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New Oscillator Topologies Using Inverting Second-Generation Current Conveyors

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Abstract

In this work, new oscillator topologies based on a recently introduced active element, namely inverting second-generation current conveyor, are presented. This recently introduced unity gain based active element is suitable for integrated circuit realization and can easily be implemented with CMOS technology. Considering this fact, basic oscillator topologies employing a single, two and three conveyors are proposed. Several oscillator circuits based on these topologies are obtained. Expressions for oscillation conditions and frequencies are derived both for ideal and non-ideal cases. Some of them are single frequency and the others are variable frequency oscillators. The oscillators employing two and three active elements use only grounded passive elements. The presented oscillators are tested with SPICE simulations to verify the theoretical results.

1. Introduction

There have been significant advances in the last three decades in linear analog integrated circuit applications since the appearance of the integrated circuit (IC) operational amplifier (op-amp). The op-amp itself is the most widely used integrated circuit among those commercially available. The applications range from analog/digital and digital/analog converters to voltage references, analog multipliers, wave shaping circuits, oscillators and function generators. However, the classical op-amp suffers from limited gain-bandwidth product problems and from low slew rate at its output. Many R-C oscillators employing op-amps have been designed and described. The limited gain-bandwidth product of the op-amp affects the oscillation condition and the oscillation frequency of the oscillator designed. They remain therefore unsatisfactory at higher frequencies [1]. Recently current-mode circuits are used instead of voltage-mode circuits for a wide variety of applications. The reason is that in voltage-mode circuits the high valued resistors with parasitic capacitances create a dominant pole at a relative low frequency, which limits the bandwidth.

In general, the node impedances in current-mode circuits are low and the voltage swings are small. Thus the time constant is reduced and also the time required for charging and discharging a parasitic capacitor is kept small. Hence the slew rate for current-mode circuits will be sufficiently high [2]. They are well suited to work at higher frequencies and thus are often used in communication circuits. Furthermore, current-mode circuits are suitable for integration with CMOS technology and thus have become more and more attractive in electronic circuit design in recent years. Previously, new current-mode active building blocks like second-generation current conveyors (CCIIs), current-feedback op-amps (CFOA) [3,4] received considerable attention due to their larger dynamic range and wider bandwidth. Moreover, different additional types of current-mode circuits, like electronically controlled current-conveyors (ECCII), differential-voltage current conveyors (DVCC), differential-difference current conveyors (DDCC), third-generation current conveyors (CCIII) and four-terminal floating nullors (FTFN), are presented in the literature [5-10]. As a result of this increasing attention, a new active element, namely inverting second-generation current conveyor (ICCII) was introduced by Awad and Soliman [11] as an adjoint block of CCII to obtain and design current-mode circuits from their voltage-mode counterparts [12, 13]. This active element can easily be implemented with CMOS technology; besides its simple realization, it offers the main advantages of the classical second-generation current conveyors [11].

Oscillators are widely used in communication, control and signal processing circuits and measurement systems. Therefore many current conveyor based oscillators are reported in the literature, which also offer the main advantages of the current-mode circuits [14-18]. The aim of this work is to contribute additional oscillator circuits to the existing ones using this new element, inverting second-generation current conveyor. It is worth noting that no oscillator structures employing ICCIIs have been described in the literature.

2. Investing Second-Generation Current Conveyor

The inverting second-generation current conveyor (ICCII) is shown in Fig. 1. The relation between terminal voltages and currents for this active element can be given with following matrix equation [11].

$$\begin{bmatrix} Iy \\ Vx \\ Iz \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} Vy \\ Ix \\ Vz \end{bmatrix} \tag{1}$$

For the above matrix representation +1 in the third row denotes positive type inverting second-generation current conveyor (ICCII+); and –1 denotes negative type inverting second-generation current conveyor (ICCII-) [11].

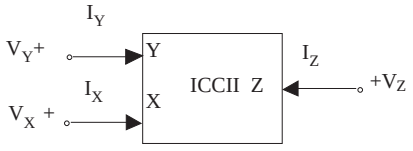

Figure 1. The circuit symbol of the inverting second-generation current conveyor (ICCII).

The matrix equation, Eq. (1), is only valid for the ideal case. In practice, however, for bipolar or CMOS implementation of the conveyor there will be voltage and current tracking errors ε_v and ε_i. The non-ideal case can be defined with the following equations:

$$\begin{aligned} v_y(t) &= -\beta\, v_x(t) \\ i_y(t) &= 0 \\ i_z(t) &= \pm\alpha\; i_x(t) \end{aligned} \tag{2}$$

where α and β are the current and voltage gains of ICCII. They can be given in terms of the tracking errors as follows:

$$\alpha = (1 - \varepsilon_i), \quad \beta = (1 - \varepsilon_v) \tag{3}$$

where ε_v and ε_i are much smaller than unity ($|\varepsilon_v| << 1,\ |\varepsilon_i| << 1$).

3. CMOS Realization

The rapid development of CMOS technology, which enables the realization of complex systems in a small chip-area, has permitted wide integration of CMOS circuits for analog functions that also include current conveyors. In Figs. 2a and 2b two different CMOS implementations of ICCII- are shown [11]. In the circuits illustrated in Fig. 2, the floating output stage introduced by Arbel and Goldminz in 1992 is used to obtain accurate current following between X and Z terminals [19], while the input stages are single output transconductors.

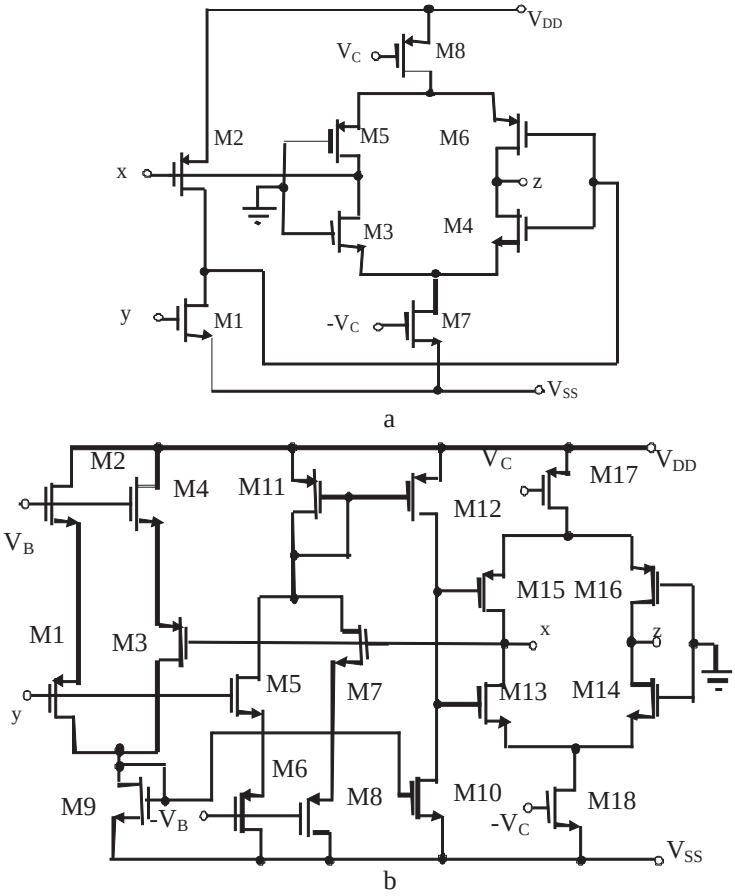

Figure 2. CMOS implementations of ICCII- [11].

The first CMOS implementation of ICCII- illustrated in Fig. 2a is very simple and the input stages are constructed with M1 and M2, but its DC offset between Y and X terminals is large. For proper operation, the aspect ratios of M1 and M2 must be chosen according to the following relation:

$$\frac{(W/L)_1}{(W/L)_2} = \frac{\mu_p}{\mu_n} \tag{4}$$

where μ_n and μ_p are the electron and hole mobilities, respectively.

In order to reduce the offset effect of the circuit in Fig. 2a and increase the voltage following range, the second CMOS circuit shown in Fig. 2b can be used [11]. The limitations of the circuit in Fig. 2a are avoided by using linear transconductors, which are constructed with four matched CMOS pairs and two current mirrors [11]. For DC offset cancellation, the difference between the two control voltages must be equal to the difference between the NMOS and the PMOS threshold voltages.

It is easily noted from Figs. 2a and 2b that CMOS simple and high performance realizations of ICCII- are possible [11]; thus we propose new oscillators employing only ICCII-s and passive elements.

4. Proposed ICCII-Based Oscillators

The oscillator topologies proposed can be considered in three categories, namely single-, two- and three-ICCII- based oscillators.

4.1. Single ICCII-based oscillators

New single ICCII- based oscillator topologies are shown in Figs. 3a-c and their characteristic equations in terms of admittances are given in Table 1. These circuits are obtained from the previously reported CCII based oscillators [14-16] by modifying them using ICCII-s.

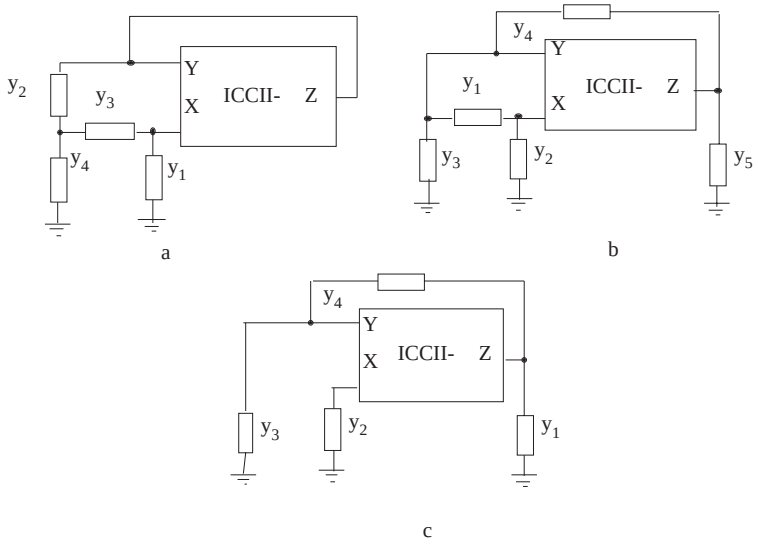

Figure 3. Proposed single ICCII-based oscillator topologies, (a) Topology 1, (b) Topology 2, (c) Topology 3.

Table 1. Characteristic equations of the presented single ICCII- based oscillators.

Topology	Characteristic equation
1	$y_1(y_2+y_3+y_4)=y_4(y_2-y_3)$
2	$y_3(y_4+y_5)+y_5(2y_1+y_4)=y_2y_4$
3	$y_1(y_3+y_4)=y_4(y_2-y_3)$

As easily seen from Table 2, two different oscillators are derived from Topology 1 by using different passive elements. The oscillators obtained with different combination of passive elements, the oscillation frequencies and the oscillation conditions are shown in Table 2.

Table 2. Oscillation frequencies and conditions of the presented single ICCII- based oscillators.

Circuit no	Admittances					Oscillation frequency (ω_0^2)	Oscillation condition
	y_1	y_2	y_3	y_4	y_5		
1	sC_1	sC_2	G_3	G_4	-	$\frac{G_3G_4}{C_1C_2}$	$C_1(G_3+G_4)=C_2G_4$
2	G_1	G_2	sC_3	sC_4	-	$\frac{G_1G_2}{C_3C_4}$	$G_1(C_3+C_4)=C_4G_2$
3	G_1	G_2	sC_3	sC_4	G_5	$\frac{2G_1G_5}{C_3C_4}$	$G_5(C_3+C_4)=C_4G_2$
4	G_1+sC_1	G_2+sC_2	sC_3	G_4	-	$\frac{G_1G_4-G_2G_4}{C_1C_3}$	$C_3G_1+C_1G_4+C_3G_4=C_2G_4$

Circuit 1 and Circuit 2 are canonic circuits; they consist of four passive elements, namely two resistors and two capacitors. It is seen in Table 2 that for Circuits 1 and 2 neither the oscillation frequency nor the oscillation condition can be adjusted without disturbing the other. Thus these oscillators are single frequency oscillators (SFOs). Furthermore, in Fig. 3a it is observed that not all the passive elements are grounded.

Circuit 3 consists of five passive elements and Circuit 4 consists of six passive elements. From Figs. 3b and 3c it is observed that also for these circuits not all-passive elements are grounded. In Circuit 3 the oscillation frequency can be adjusted independently of the oscillation condition with R_1 and the oscillation condition can be adjusted independently of the oscillation frequency with R_2. The resistor R_2 is grounded but not R_1. This circuit is very interesting because this topology is only meaningful with ICCII but not with CCII since the admittance between Y and X terminals of the conveyor is redundant for the last case. In Circuit 4 the oscillation frequency can be adjusted independently of the oscillation condition with R_2 and the oscillation condition can be adjusted independently of the oscillation frequency with C_2. Both elements are grounded and this circuit is suitable for low frequency operation. The last two circuits are variable frequency oscillators (VFO).

4.2. Oscillators employing two ICCIIs

The proposed oscillator topology employing two ICCIIs and only grounded passive elements is shown in Fig. 4. The proposed oscillator topology (Topology 4) in Fig. 4 is based on the modified well-known Sedra-Smith gyrator [20]. The characteristic equation in terms of admittances is given by

$$y_2y_4-y_1y_3=0 \tag{5}$$

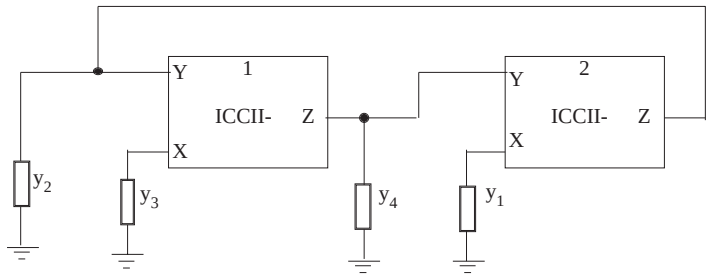

Figure 4. Proposed oscillator topology employing two ICCII-s (Topology 4).

By appropriately choosing the grounded admittances, various oscillators can be obtained. The resulting circuits are given in Table 3. Each circuit, except the last four given in Table 3, employs seven passive components, but they exhibit non-interactive control between oscillation frequency and oscillation condition. The first four circuits are suitable for low frequency oscillators. The oscillation frequency of Circuits 9-12 can be adjusted with capacitors without disturbing the oscillation condition. As seen from Table 3, Circuit 13 is obtained by removing the resistor (R_3) from Circuit 5, but the resulting circuit is now a single frequency oscillator (SFO). This operation is also performed for Circuits 6-8 and the last three SFOs are obtained.

Table 3. Oscillation frequencies and conditions of the presented oscillators employing two ICCIIs.

Circuit no	Admittances				Oscillation frequency (ω_0^2)	Oscillation condition
	y_1	y_2	y_3	y_4		
5	G_1	G_2+sC_2	G_3+sC_3	G_4+sC_4	$\frac{G_2G_4-G_1G_3}{C_2C_4}$	$C_2G_4+C_4G_2=C_3G_1$
6	G_1+sC_1	G_2	G_3+sC_3	G_4+sC_4	$\frac{G_1G_3-G_2G_4}{C_1C_3}$	$C_1G_3+C_3G_1=C_4G_2$
7	G_1+sC_1	G_2+sC_2	G_3	G_4+sC_4	$\frac{G_2G_4-G_1G_3}{C_2C_4}$	$C_2G_4+C_4G_2=C_1G_3$
8	G_1+sC_1	G_2+sC_2	G_3+sC_3	G_4	$\frac{G_1G_3-G_2G_4}{C_1C_3}$	$C_1G_3+C_3G_1=C_2G_4$
9	sC_1	G_2+sC_2	G_3+sC_3	G_4+sC_4	$\frac{G_2G_4}{C_2C_4-C_1C_3}$	$C_2G_4+C_4G_2=C_1G_3$
10	G_1+sC_1	sC_2	G_3+sC_3	G_4+sC_4	$\frac{G_1G_3}{C_1C_3-C_2C_4}$	$C_1G_3+C_3G_1=C_2G_4$
11	G_1+sC_1	G_2+sC_2	sC_3	G_4+sC_4	$\frac{G_2G_4}{C_2C_4-C_1C_3}$	$C_2G_4+C_4G_2=C_3G_1$
12	G_1+sC_1	G_2+sC_2	G_3+sC_3	sC_4	$\frac{G_1G_3}{C_1C_3-C_2C_4}$	$C_1G_3+C_3G_1=C_4G_2$
13	G_1	G_2+sC_2	sC_3	G_4+sC_4	$\frac{G_2G_4}{C_2C_4}$	$C_2G_4+C_4G_2=C_3G_1$
14	G_1+sC_1	G_2	G_3+sC_3	sC_4	$\frac{G_1G_3}{C_1C_3}$	$C_1G_3+C_3G_1=C_4G_2$
15	sC_1	G_2+sC_2	G_3	G_4+sC_4	$\frac{G_2G_4}{C_2C_4}$	$C_2G_4+G_2C_4=C_1G_3$
16	G_1+sC_1	sC_2	G_3+sC_3	G_4	$\frac{G_1G_3}{C_1C_3}$	$C_3G_1+C_1G_3=C_2G_4$

4.3. Oscillators employing three ICCIIs

New oscillator topologies employing three ICCIIs and only grounded passive elements are shown in Fig. 5. These topologies are based on the modified circuits with the ICCII-s given in ref. [21, 22]. Their characteristic equation in terms of admittances is equal for the ideal case and is given as follows:

$$y_1y_4+y_2y_5-y_3y_5=0 \tag{6}$$

Two oscillators (Cases A and B in Table 4) are obtained with a different combination of passive elements for each topology, so the total number of the oscillator circuits employing three ICCII-s is eight. The oscillation frequencies and the oscillation conditions are given in Table 4.

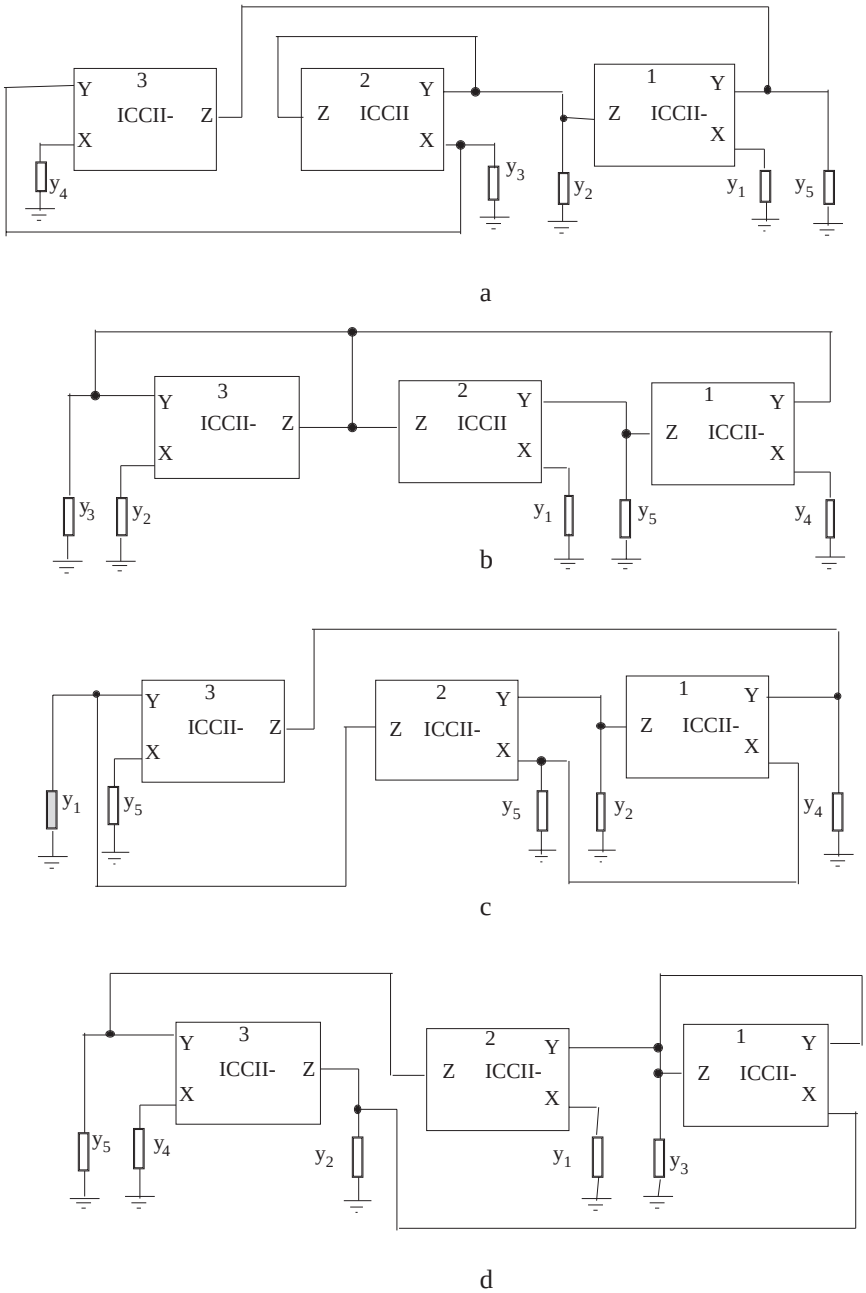

Figure 5. Proposed oscillator topologies employing three IICC-s: (a) Topology 5, (b) Topology 6, (c) Topology 7, (d) Topology 8.

Table 4. Oscillation frequencies and the oscillation conditions of oscillators employing three ICCIIs.

Case	Admittances					Oscillation frequency (ω_0^2)	Oscillation condition
	y_1	y_2	y_3	y_4	y_5		
A	G_1	G_2+sC_2	G_3	G_4	sC_5	$\frac{G_1G_4}{C_2C_5}$	$G_2 = G_3$
B	sC_1	G_2+sC_2	sC_3	sC_4	G_5	$\frac{G_2G_5}{C_1C_4}$	$C_2 = C_3$

It is obvious from Table 4 that all oscillators employ three active and six passive elements, but they offer independent control features between oscillation frequency and oscillation condition. Therefore they

can be used as variable frequency oscillators (VFO). Furthermore, a single grounded resistance can adjust their oscillation frequencies, and they are called single resistance controlled oscillators (SRCOs).

5. Oscillation for the Non-Ideal Case

The oscillation frequencies and the oscillation conditions are given for the ideal case in the previous section. Taking the non-idealities of ICCIIs given in Eqs. (2) and (3) into account, the characteristic equations are recalculated as follows:

Characteristic equations for oscillators employing single ICCII- are given in Table 5.

Table 5. Characteristic equations of the presented a single ICCII- based oscillators for the non-ideal case.

Topology	Characteristic equation
1	$\alpha\beta\, y_1(y_2+y_3+y_4)-y_2y_3(1+\beta)(1-\alpha)=y_4(y_2-\alpha\beta y_3)$
2	$y_3(y_4+y_5)+y_5[(1+\beta)y_1+y_4]+(1-\alpha)(1+\beta)y_1y_4=\alpha\beta y_2y_4$
3	$y_1(y_3+y_4)=y_4(\alpha\beta y_2-y_3)$

Characteristic equation for oscillator topology employing two ICCII-s can be given as:

$$y_2y_4-\alpha_1\beta_1\alpha_2\beta_2y_1y_3=0 \tag{7}$$

Characteristic equations for oscillator topologies employing three ICCII-s are different for the non-ideal case and are given in Table 6.

Table 6. Characteristic equations of the presented three ICCII-s based oscillators for the non-ideal case.

Topology	Characteristic equation
5	$\alpha_1\beta_1\beta_2\alpha_3\beta_3y_1y_4+y_2y_5-\alpha_2\beta_2y_3y_5=0$
6	$\alpha_1\beta_1\alpha_2\beta_2y_1y_4+\alpha_3\beta_3y_2y_5-y_3y_5=0$
7	$\alpha_1\beta_2y_1y_4+\beta_1\alpha_2\alpha_3\beta_3y_2y_5-\alpha_1\beta_1\alpha_2\beta_2\alpha_3\beta_3y_3y_5=0$
8	$\alpha_1\alpha_2\beta_2\alpha_3\beta_3y_1y_4+\alpha_1\beta_1y_2y_5-y_3y_5=0$

Oscillator frequencies and oscillation conditions for the non-ideal case of the proposed oscillator circuits can easily be found by using Tables 5-6 and Eq. (7).

6. Design Example and Simulation Results

All the presented oscillators are tested with SPICE simulations to verify the theory. Topology 8 employing three ICCII-s (Fig. 5d) is chosen as a design example. The element values are chosen as $R_1 = R_2 = R_3 = R_4 = 10\text{k}\Omega$ and $C_2 = C_5 = 400\text{pF}$, which results in an oscillation frequency of $f_o = 39.78$ kHz. The circuit was realized with the CMOS implementation of ICCII- illustrated in Fig.2b and supplied with symmetrical voltages of $\pm$ 2.5V. The biasing voltages are chosen as $V_C = \pm$ 1.2V. The MOS transistor model parameters and device dimensions used for SPICE simulations are given in Tables 7 and 8.

Table 7. 1.2 μm CMOS process model parameters used for SPICE simulations

```
.MODEL nb NMOS LEVEL=3 PHI=0.7 TOX=3.05E-8 XJ=0.2U
+TPG=1 VTO=0.95705 DELTA=1.252 LD=1.7777E-9 KP=7.9173E-5
+U0=699.3 THETA=1.2260E-01 RSH=9.091E-2 GAMMA=0.5623
+NSUB=1.221E16 NFS=6.5E11 VMAX=2.025E5 ETA=1.056E-1
+KAPPA=1.954E-01 CGDO=5.0000E-11 CGSO=5.0000E-11
+CGBO=3.266E-10 CJ=2.7366E-4 MJ=5.428E-1 CJSW=1.736E-10
+MJSW=1.000E-1 PB=9.9E-1

.MODEL pb PMOS LEVEL=3 PHI=0.7 TOX=3.05E-8 XJ=0.2U
+TPG=1 VTO=-0.8351 DELTA=2.186 LD=1.1E-9 KP=1.91485E-5
+U0=172.1 THETA=9.69E-02 RSH=1.727E-1 GAMMA=0.3423
+NSUB=4.525E15 NFS=6.5E11 VMAX=2.038E5 ETA=1.487E-1
+KAPPA=9.998 CGDO=5.0000E-11 CGSO=5.0000E-11
+ CGBO=3.411E-10 CJ=2.883E-4 MJ=4.9284E-1 CJSW=2.0216E-10
+MJSW=1.000E-1 PB=9.9E-1
```

Table 8. Dimensions for transistors of the ICCII- realization used for SPICE simulations.

	W [μm]	L [μm]
M1	30	4.8
M2	97.2	4.8
M3	60	1.2
M4	60	1.2
M5	120	1.2
M6	120	1.2
M7	94.8	3.6
M8	198	3.6

The waveform of the output voltage is shown in Fig. 6. The oscillation frequency of the actual circuit is specified as f_o = 38.76kHz. The offset voltage at the output and the deviation in the oscillation frequency is caused by the non-idealities and the parasitics of the active elements.

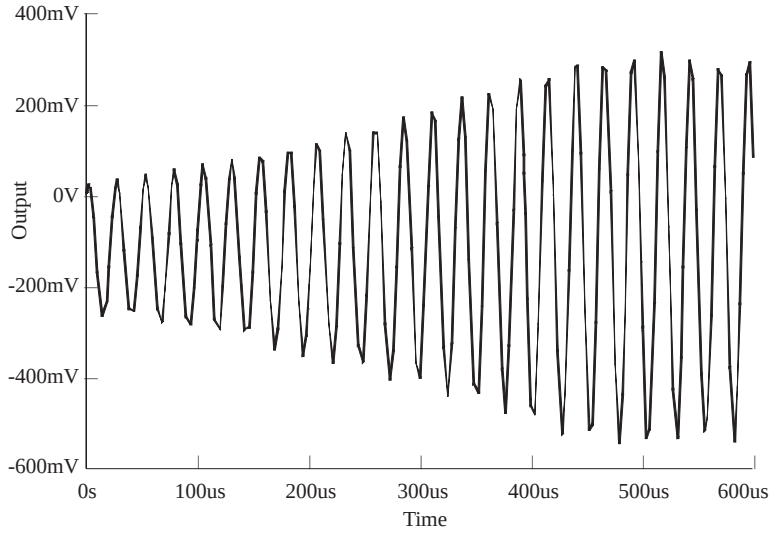

Figure 6. Growing oscillations for Topology 8 (case A).

Note that the output signal of the oscillator topologies proposed can be taken at any node of the corresponding circuit. Also note that a current output is available if the Z terminal current of the ICCII- realization circuit is mirrored to a second Z terminal. In this case, the ICCII- forms a dual output circuit, which can be considered as a further design possibility in current-mode analog design.

7. Conclusions

In this study, employing the inverting second-generation current conveyor (ICCII), new ICCII- based R-C sinusoidal oscillators are proposed. Corresponding oscillation frequencies and oscillation conditions are given in tabular form. Their characteristic equations are given also for the non-ideal case. Some of the presented oscillators are single frequency oscillators and some can be used as variable frequency oscillators. Many of them employ all grounded passive elements and ICCII-s, which can be considered as a further advantage for integration. It should be noted again that the second presented oscillator topology (circuit 3) is not realizable using CCII, which indicates that some circuit topologies are only for implementation using ICCIIs. The presented circuits represent additional topologies to conveyor-based oscillators known in the literature to date. Because of the simple circuitry of CMOS ICCII- realization, the presented oscillator circuits can easily be implemented and applied to any analog system, and therefore they provide new design possibilities for the IC designer.

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