

A New Simulator for HVdc/ac Systems-Part I

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Abstract

A simulator with optimal step time (SOST) has been designed to investigate Large HVdc/ac systems. The adequacy and robustness of the simulator will be demonstrated by showing some important applications relevant to operation, operational planning and medium-term planning.

Some of the features of our SOST simulator are optimal step time algorithm, interpolation, chatter removal, MATLAB interface, unlimited size of ac system, and Farsi command that help model complex power electronic circuits, provide fast and accurate results.

On account of its reduced calculation effort and deterministic execution time, optimal-step simulation is a prerequisite for real-time performance. However, when simulating electromagnetic-transients behavior, it introduces errors in the form of switching delays and inconsistent initial conditions. In order to eliminate these errors, the present paper describes a comparison of performance (the focus of numerical simulation) of traditionally simulation with SOST in large HVdc systems. A detailed simulation of HVdc converter behaviour has been modified to eliminate switching delays and calculate consistent initial conditions, even though switching time may not coincide with a calculation time-step and a circuit may pass through a series of simultaneous switchings. Furthermore, the SOST proposed has a simple decoupling technique to isolated parts of the circuit where the switching occurs in order to reduce the effort required for the calculation of initial conditions.

Key Words: *Large scale, HVdc/ac system, time domain analysis, dynamic behavior, power system simulation.*

1. Introduction

The stable operation of a HVdc/ac system is dependent on the balance of mechanical and electromagnetic forces keeping the generators in synchronism [1]. A disturbance in the HVdc/ac system may or may not result in the system falling out of synchronism and electrically collapsing. The assessment of such behavior is the purpose of electromechanical stability studies.

Two types of stability study are normally carried out. Subsequent recovery from a sudden large disturbance is referred to as transient stability, and the solution is obtained in the time domain. The period under investigation can vary from a fraction of a second, when first-swing stability is being determined, to over 10 s when multiple-swing stability must be examined.

The term dynamic stability is used to describe the long-term response of a HVdc/ac system to a small disturbance or badly set automatic control. In this paper steady state operations, transient stability, and dynamic stability are considered in the time domain, with the latter as an extension of the former.

The ac systems may be either synchronously interconnected or isolated. The HVdc system could indicate interconnection.

For modeling and simulation purposes, the integrated HVdc/ac system is divided into the following subsystems:

1. Frequency dependent ac system beyond the interface buses,
2. Interface buses with the shunt connected equipment,
3. Six-pulse converter units,
4. dc transmission system, and
5. HVdc controls.

The proposed hybrid algorithm utilizes electromechanical simulation as the steering program, and the electromagnetic-transients program is designated a subroutine.

A hybrid approach is also used to study the impact of ac-system dynamics, particularly those of a weak ac system on dc system transient performance [1].

Disturbance response studies, control assessment and temporary overvoltage consequences are all typical examples for which a hybrid package is suited.

In this paper, the ac system contains 2 HVdc links. Both links can be modeled independently in detail and represents the equivalent of an ac system.

The numerical simulation problem of switched circuits (in electromagnetic-transients behavior) was present in this simulator.

The main problems were the very complex nature of the switching device and its very fast behavior. They were partly solved by reducing the switch model to an ideal switch model, which may be either open-circuit or short-circuit, with instantaneous switching behavior. However, 2 main problems remain :the estimation of the exact switching time, and the calculation of the initial conditions required to resume the simulation, with the updated equation set, after a switching occurs.

In the present work both the switching delay and initial conditions problem are addressed. A double interpolation method is proposed that allows an appropriate bridging of the delay between switching time and integration step, and a method of calculating the initial conditions following every discontinuity or switching operation is suggested.

2. Steady State Simulation of HVdc/HVAc Systems

The basic concept, shown in Figure 1 is not restricted to HVdc/HVAc applications only. The transfers of voltage and current across the ac/dc converter are completely specified by the switching instants of the bridge valves, being both the firing and end of commutation instants.

In this simulator we used the converter models required for different power-system studies in the steady state, and these range from fundamental frequency power flow to unbalanced operation assessment in order of increasing modeling complexity [1].

The converter, whether rectifying or inverting, is represented by the circuit in Figure 2.

With reference to Figure 2 the converter model uses 26 variables, i.e. $E_1, E_2, E_3, \theta_1, \theta_2, \theta_3, I_1, I_2, I_3, \omega_1, \omega_2, \omega_3, u_{12}, u_{13}, u_{23}, C_1, C_2, C_3, \alpha_1, \alpha_2, \alpha_3, a_1, a_2, a_3, I_d$ and V_d .

Therefore, 26 equations have to be found involving these variables [1].

Thus, for each network-loading component an injected current is calculated by solving the relevant differential algebraic equations.

The nodal voltage is then obtained from the current injections and matrix admittance. However, as the network voltages affect the loading components, an iterative process is often required.

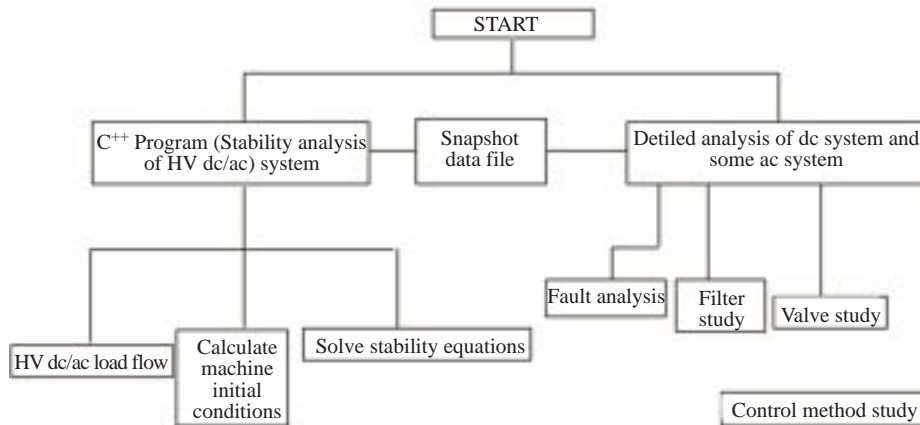


Figure 1. Description of hybrid algorithm.

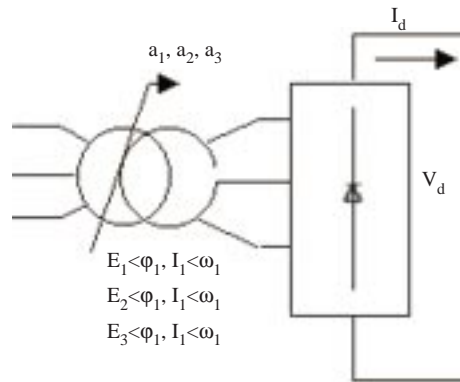


Figure 2. Basic converter unit [2].

3. Transient Simulation

SOST presents a general and efficient method for the transient simulation of HVdc converters based on network topological concepts, which provides an efficient solution to the problem of modeling. The inherently nonlinear characteristics and time-varying topology of static power converters are caused by the switching action of the valves [3].

4. Optimal Step Time Algorithm

The SOST algorithm imposes no restriction on the integration step length and the instances of network topological changes or parameter value changes are determined accurately by changing the simulation step size.

The time for switching ‘ON’ a converter valve and fault application are easily determined before the event. The time of zero current in converter valves and fault branches are detected after they occur and linear interpolation is used to derive the switching instant. SOST employs the following different method for iterative implicit integration:

- Dormand-Prince,
- Runge-Kutta,
- Bogacki-Shampine,
- Heun,
- Euler,
- Stiff/NDF, and
- Stiff/Mod.Rosenbroek.

The basic structure of a optimal step time algorithm is given in Figure 3.

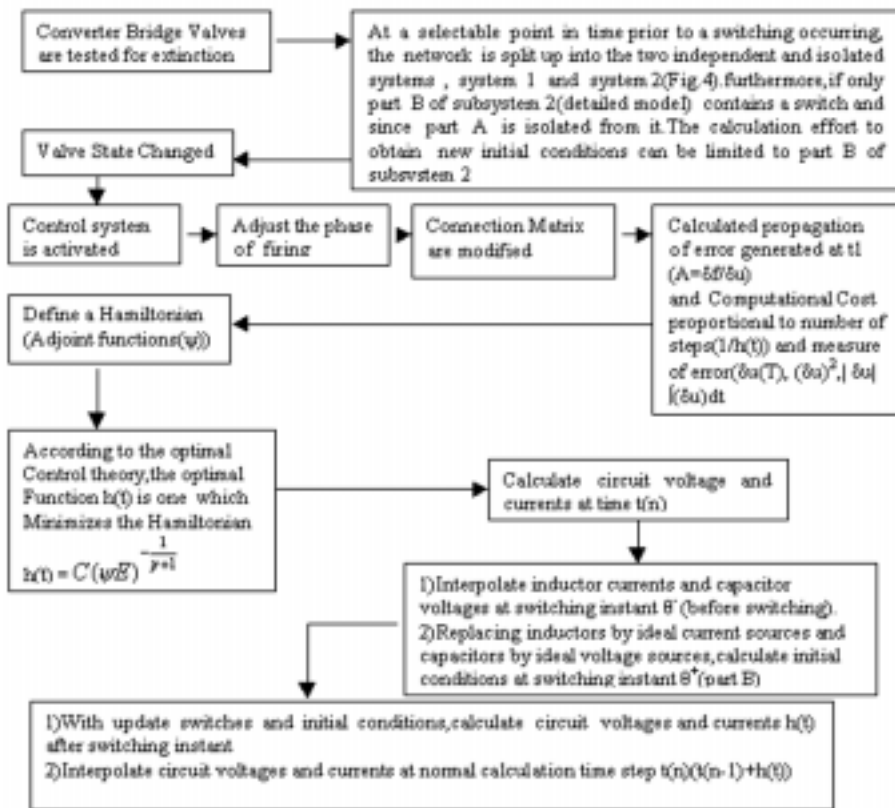


Figure 3. Optimal step time algorithm.

The dynamic location of a discontinuity will force the step length to change between the maximum and minimum step size. In the case of HVdc systems, which are stiff, the use of optimal step-size algorithm will generally lead to an optimal simulation times.

5. The Modeling Algorithm

The hybrid-algorithm interface shown in Figure 4 contains the 5 possible states summarized in Table 1.

The default state is 0 for the first time that the algorithm is called.

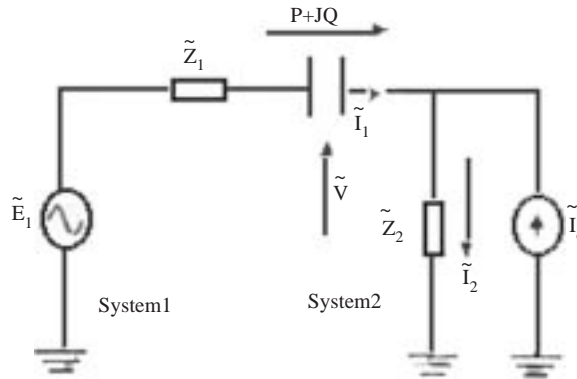


Figure 4. Variable (P,Q,V,I) extracted and converted.

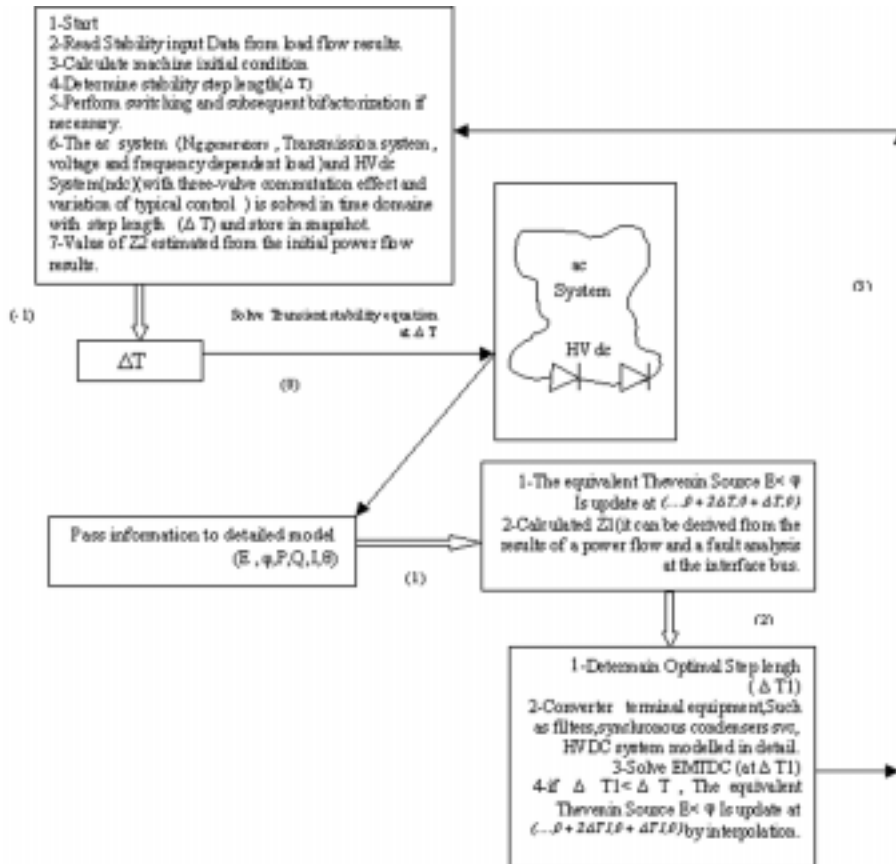


Figure 5. The state conditions.

This occurs once transient simulation has reached steady-state electromechanical equilibrium and is ready for interfacing prior to a system disturbance.

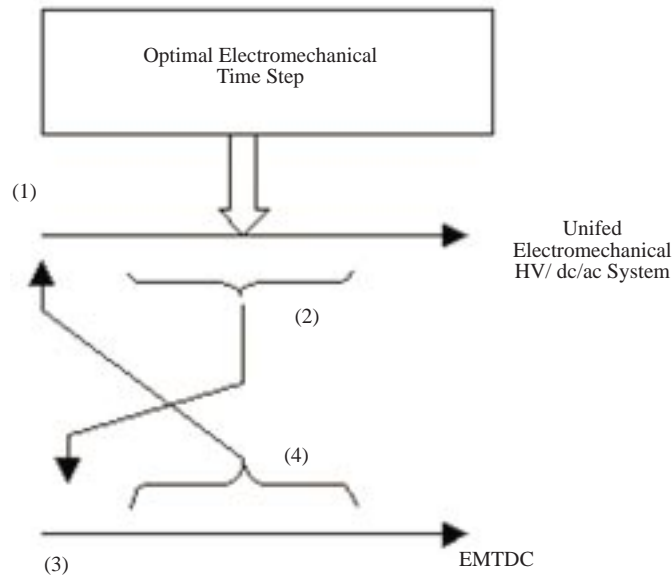


Figure 6. The interaction protocol.

EMTDC is called for a full fundamental period ahead of transient simulation and P, Q, V, I (Figure 4) are extracted and converted to positive sequences.

The state is now set to 1. Transient simulation is run for one half of the fundamental period and the variables (P, Q, V, I (Figure 5)) at its interface location are compared with those of EMTDC. If the data in both files is correctly set then the transient network is the split into systems 1 and 2, and Norton equivalent circuits are set up in each system.

Table 1. Interfacing states.

State	Event
-1	Isolate transient network ready to interface with EMTDC
0	Initial time through interfacing routine
1	Normal interaction between transient and EMTDC
2	Run EMTDC For full period
3	Transient model catching up with EMTDC after a system-network change

The state conditions and interaction protocol around a disturbance are shown in Figure 6.

At the fault time, the interface variables are passed from the transient model to system 1 equivalent in EMTDC in the usual manner as shown by arrow marked 1 in Figure 6a. EMTDC is then run for a full fundamental-period length past the fault application (arrow 2) and the information obtained over this period is passed back to the transient model (arrow 3).

The fault is now also applied to the transient model which is then solved for a period unit until it has again reached EMTDC position in time (arrow 4).

5.1. The HVac/HVdc test system and results

The configuration of the HVdc/HVdc system modeled is shown in Figure 7 The system consists of 2 HVdc links and a 169 bus ac system.

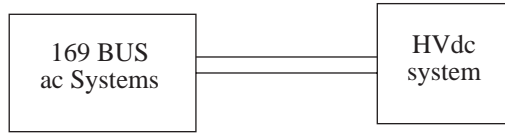


Figure 7. Configuration of the test system[4].

The complete description of the ac/dc system Data can be found in the paper [4].

5.2. Stability analysis

This Section Shows the eigenvalues and root locus when the HVdc system is operating with a very weak ac system at the inverter end (the rectifier control modes are direct current feedback and inverter control strategies are constant gamma mode).

Reduction of the SCR (keeping power factor constant) at the inverter ac system mostly affects the lower frequency and the system is very sensitive (Figure 8).

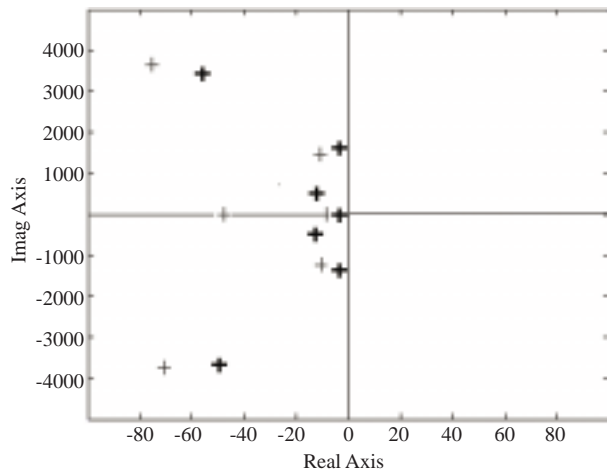


Figure 8a. Root locus with direct current feedback + eigenvalues of uncontrolled system ($s_{cri} = 1.5$) + eigenvalues of original system.

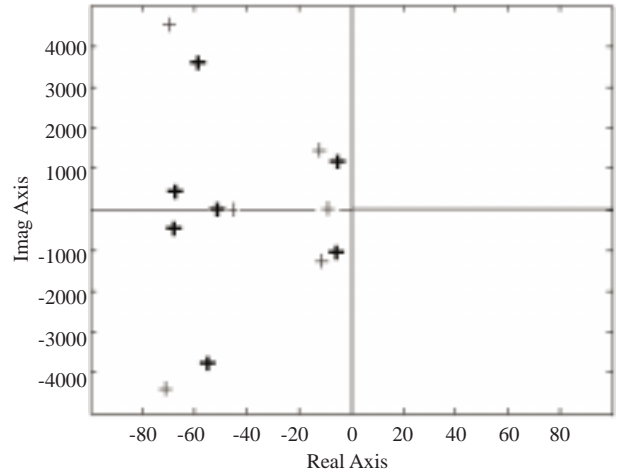


Figure 8b. Root locus with direct current feedback + eigenvalues of uncontrolled system ($s_{cri} = 3$) + eigenvalues of original system.

As can be seen from Tabel 2 the damping of dominant oscillatory mode was even improved with reduced SCR at rectifier side.

5.3. Operational planning

This application concerns the suitability assessment of the test system EHV grid to supply large load.

1. Frequency changes produced by step and ramped variations of the active and reactive power profiles absorbed from (or delivered to) the grid by a large load. This effect is almost independent of the particular site chosen.

2. Voltage changes produced by step and ramped variation of reactive power are absorbed from the grid by the large load, this is a typical site-dependent effect.
3. Further disturbances are relevant to the voltage harmonics content, as well as the inverse voltage sequence produced by the unbalancing of the large load. Both these aspects have been examined with tools other than the SOST simulator and, therefore, they are neglected in this paper.

During AVR action, which is very important to compensate the voltage drop in the area affected by the large load operation, the simulations demonstrated that the variations of the reactive large load causes a voltage drop of KV (15%) at the large load BUS, reduced by AVR action to (8%) in less than 2 s.

Table 2. System Eigenvalues for Reduced SCR [5,6]

	Original System	Rec.SCR = 3 Inv.SCR = 1.5	Rec.SCR = 1.5, Inv.SCR = 3
1	-48.23	$-10 \pm 105j$	$-72.3-310j$
2	$-6.43 \pm 1190j$	$-5.83 \pm 1200j$	$-7.78 \pm 1090j$
3	$-76.7 \pm 3680j$	$-43.6 \pm 3580j$	$-59 \pm 3600j$
4	-5.76	-5.34	-5.98

5.4. Medium-term planning

Stability assessment of the system is analyzed using the SOST simulator. In this case, the system is driven to an unstable equilibrium point (Uep).

Thus the simulator first computes the bifurcation diagram (nose curves) using the generation and load distribution factor defined in the BUS data and then it computes the system time trajectory starting at the computed Uep (Figure 9). default dynamic P and Q load model is changed with the help of the options

- changes default P time constant of 0.1.
- changes default Q time constant of 0.01.
- defines percentage of load to be modeled as resistance (10%) and reactance (10%) and, finally, calculates the ac/dc energy function Hessian.

6. Differences Between Sost and Other Simulators

6.1. Fault study (EMTDC)

A realistic comparison of the HVdc converter behavior provided by the 2 alternative algorithms (SOST, EMTDC) can be achieved with reference to the system illustrated in Figure 7. It consists of a monopolar dc. link with a single bridge at each end (bus 69 and 71 at test system) provided with the basic control functions. A 3-phase short circuit is applied to rectifier terminals at time 0.6 s and cleared 3 cycles later. The rectifier dc currents, displayed for the 2 solutions in Figure 9, show a very similar variation for the SOST and EMTDC solutions, except for the region between $t = 0.803$ s and $t = 0.914$ s (the ac voltage drops to

zero (0.6 s), the rectifier is blocked and the converter dc current collapses. The dc- line voltage is effected by inductive and capacitive components of the line. When the fault is cleared (at $t = 0.66$ s), a dynamic over voltage is set up until the full power to link is restored.

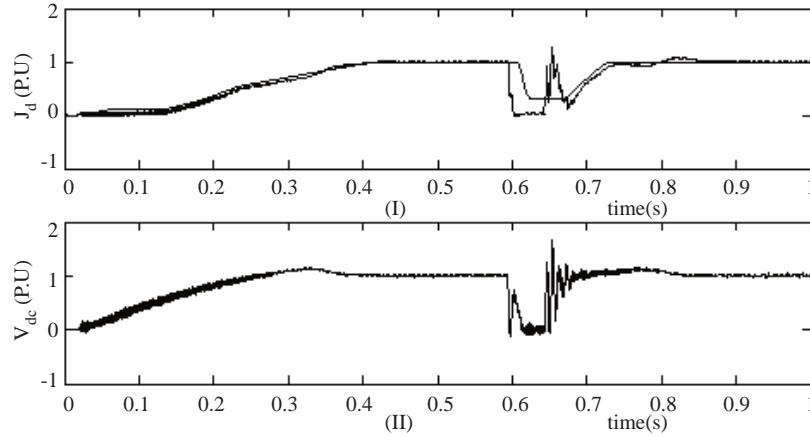


Figure 9. The three-phases fault at the rectifier terminal, I- The Dc-Side Current (input), II- The DC-Side Voltage (input).

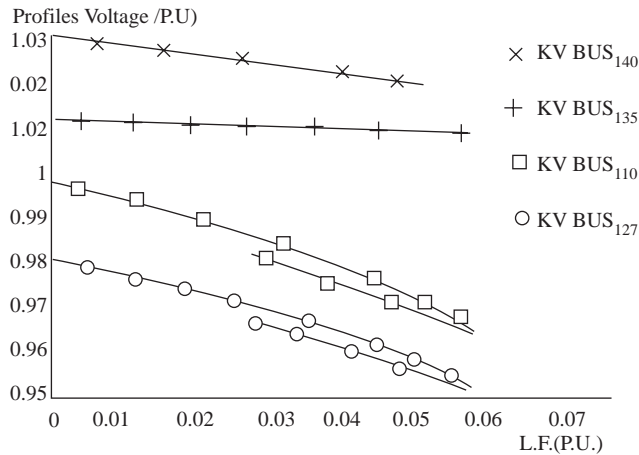


Figure 10. Nose curves (140, 136, 110, 127).

The rectifier is unblocked at $t = 0.7$ s and few ms later the inverter takes over conduction from its bypass valves. Following an initial current inrush into the dc-line capacitance, the power setting is ramped up. At 0.87s the inverter is restarted and the link current dips, the current drop being more pronounced, and maintained for a longer period, in the EMTDC solution. At the end of power ramp, the ac current has returned to its nominal value and after a small oscillatory settling of the controllers so do the dc voltage and current. Figure 11a compares their results for line-to-ground (L-G) fault simulation. For instance, with reference to Figure 11b, valve 5 attempts to conduct at about 0.515 s in the EMTDC simulation, whereas it does not conduct at all in SOST. Thus, some small deviations are observed in the dc current and ac voltage waveforms illustrated in Figure 11a. An important algorithmic difference between SOST and EMTDC is the use of the subsystem concept by the latter. In EMTDC, commutation voltages at the t^{th} interval are derived from those calculated in the previous interval ($t-\Delta t$) by an approximate phase advance prediction. This is achieved by equation (1).

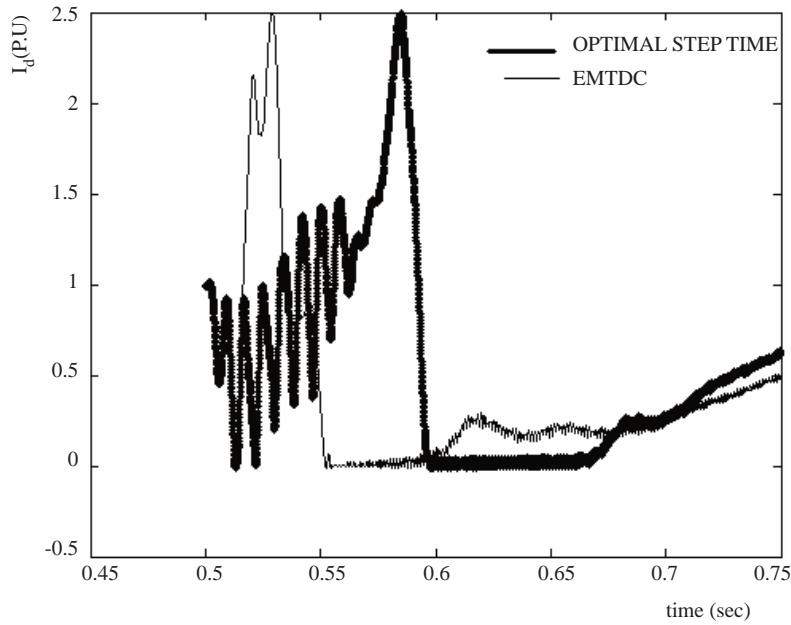


Figure 11a. Line-to-Ground fault current SOST, EMTDC.

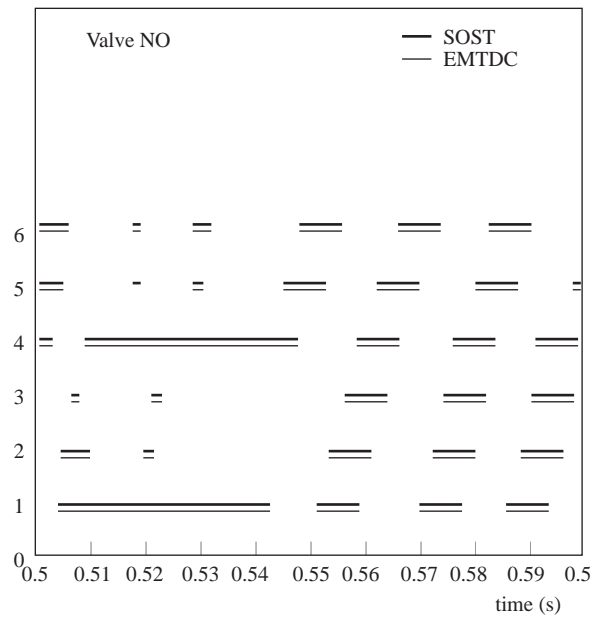


Figure 11b. Comparing valve conduction (Commutation failures predicted by both program is eight).

$$V_t = (1 - \omega^2 \Delta t^2) V_{a(t-\Delta t)} + \frac{\omega \Delta t}{\sqrt{3}} \{ V_{c(t-\Delta t)} - V_{b(t-\Delta t)} \} \quad (1)$$

However, this equation is based on the assumption that the voltages are perfectly balanced and therefore their use is only accurate under balanced steady-state or symmetrical-faults conditions. Thus, neglecting the considerable negative sequence voltage content during L-G fault simulations can cause some error in the derivation of the commutation voltages, which alters the valves commutation interval and voltage crossings, which alters the valve extinction angles. This may account for the small differences in the valve conduction patterns between the EMTDC and SOST results observed during the asymmetric disturbances. [7]

6.2. Power flow study (sequential method)

Power flow study in SOST is based on a unified method. The overall convergence rate of the ac/dc algorithms depends on the successful interaction of the 2 distinct parts.

The ac system equations are solved using the well-behaved constant tangent fast decoupled algorithm, whereas the dc system equations are solved using the more powerful, but somewhat more erratic, full Newton-Raphson approach.

The powerful convergence of the full Newton-Raphson process for dc equations can cause overall convergence difficulties.

If the first dc iteration occurs before the reactive power voltage update, then the dc variables are converged to be compatible with the incorrect terminal voltage.

This introduces an unnecessary discontinuity which may lead to convergence difficulties in the sequential method (Table 3 compares the 2 method).

To illustrate the nature of the iteration (for more detailed and quantitative comparison study), the convergence pattern of the converter reactive power demand and the ac system terminal voltage of the rectifier is shown in Table 3c.

Table 3a. Number of iterations for test system (strong ac system)-(A: reactive power control, P: active power control)

m-rectifier, n-inverter	SOST (Unified)	Sequential P,Q,dc
A mPdm γ nVdn	20	22
A mPdmanVdn	42	50

Table 3b. Number of iterations for test system (weak ac system) (γ, α : extinction, firing angle control).

m-rectifier, n- inverter, a: tap	SOST (Unified)	Sequential P, Q,dc
Am Pdm γ nVdn	22	22
Am P manVdn	45	50
Am P dm anVdn	>50	50

Table 3c. Convergence pattern (weak ac system).

	SOST	Sequential
TerminalVotage (p.u.)	0.94, 0.93, 0.937, ..., 0.939	0.91, 0.94, 0.92, 0.939, 0.923, ..., 0.930
Reactive Power (MVAR)	28, 22.5, 22,21.5, ..., 21.8	28, 18, 23.7, 20, 22, ..., 21

7. Conclusion

This algorithm utilizes the general properties and structure of HVac/HVdc systems to achieve the following:

1. Minimization of the computations involved in the construction of the state equations of the system at each switching instant.

2. Direct construction of the model of the integrated system from the models of its components which makes the system modeling process easily programmable and increases the flexibility of the simulation [8].
3. Division of study and integrated ac/HVdc system into its dc systems, steady state simulation , fault analysis detailed study. This facilitates the use of parallel processing techniques if higher simulation speeds are required for certain applications.
4. The results show that using a frequency-dependent equivalent is also entirely adequate for presenting the correct effects of waveform distortion to the converter terminal.
5. Minor disturbance has been used to validate the SOST response (response is practically identical to that of the electromechanical-stability algorithm).
6. Major disturbance, a line-to-ground fault at the rectifier-converter terminal, exemplifies the differences between the 2 types of solution.

The electromechanical solution show the slower dynamic response of the ac system ,and the electromagnetic solution displays the fast dynamics of the rapidly switched converter.

In SOST these responses are combined, thus giving a more realistic overall picture of the entire system's performance (generator, controller response varying the ac-system voltage at the converter terminal).[9]

7. Major disturbance, a 3-phase short circuit at the rectifier-converter terminal, exemplifies the main difference between them occurring in the period between fault removal, where the fixed-voltage source of EMTDC model predicts a higher voltage (SOST have a variable-voltage source).
8. Power flow study in SOST is based on a unified method. The results show that in cases where the ac system is weak, the sequential algorithm is susceptible to convergence problems. Thus, in general the unified method is recommended due to its greater reliability. In cases where the ac system is strong ,the unified algorithm may be programmed to give fast and reliable convergence.

References

- [1] J. Arrillaga, B. Smith, "ac/dc Power System Analysis", Power Energy Series 27, IEE, 1998.
- [2] J. Arrillaga, N.R. Watson, G.N. Bathurst, "Unified Newton Framework for the Steady State Simulation of Networks with Multiple ac-dc Converters", IEEE papers 85 PCC, Osaka, 2002.
- [3] S. Miliadis, TH. Argitis, Z. Harias, "Transient Simulation On Of Integrated ac/HVdc Systems Part I, II", IEEE Transactions on Power Systems Vol. 3, No. 1, February , 1988.
- [4] Common Format for Exchange of Solved Load Flow Data, IEEE Trans .Power Apparatus and Systems, Vol. 92, No. 6, Nov/Dec 1973, 1916-1925. Working Group report.
- [5] J. Arrillaga, " High Voltage Direct Current Transmission", Peter Peregrinnus Ltd., London, UK, 1983.
- [6] D. Jovicic, N. Pahalawattha, "Stability analysis of HVdc Control Loops", IEEE Proc-Gen. Trans. Distr., Vol. 146, No. 2, March ,1999.
- [7] H.W. Dommel, "Digital Computer Solution Of Electromagnetic Transients In Single And Multiphase Network", IEEE Trans. on Power Apparatus and Systems, Vol. PAS- 88. No. 4, April 1964, 388-399.

- [8] R. Saeks, R. Decalo, “ Interconnected Dynamic System”, Marcel Dekker, 1980.
- [9] D.A. Woodford, A.M. Gol, R. Menzies, “Digital Simulation Of dc Links And ac Machines”, IEEE Transactions on Power Apparatus and Systems, Vol, PAS-102, 1616-1623, June 1983, 1616-1623.