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A new CMOS Differential OTRA Design for the Low Voltage Power Supplies in the Sub-Micron Technologies

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Abstract

In this study, a new CMOS differential OTRA topology is proposed. This topology can operate with a very low voltage power supply as ± 0.6V. In this design, CMOS 0.13 μm STMicroelectronics technology transistor models are used for the simulations. The designed CMOS OTRA has a transresistance gain (Rm) of 7478 V/I with a 28.1 MHz bandwidth (-3 dB) and a transresistance unity-gain bandwidth of 2 GHz. To demonstrate the performance of the OTRA, designed low pass, high pass and band pass filters employing a single CMOS differential OTRA and passive elements are tested with SPICE simulation program to verify the theoretical results.

Key Words: *OTRA, transimpedance amplifier, low voltage power supply, current-mode circuit, sub-micron technology, filter design.*

1. Introduction

The growing demand for mobile communications has led to high level of chip integration and directed research towards the field of high frequency applications. In the new designed circuit topologies for high frequencies, current-mode approach is preferred rather than the traditional voltage-mode structures. OTRA (Operational Transresistance Amplifier), which is commercially available under the name of Norton amplifier has been attracted attention by its advantages in the current-mode circuit design [1, 2]. Low input and output impedances, a bandwidth independent of the device gain can be considered the main advantageous properties of the OTRA. These commercial realizations don't provide a true virtual ground at the input terminals and they allow the input current to flow in one direction only. In order to remove these disadvantages of the OTRA, some topologies are proposed in the literature [3-8]. But these solutions are both complex structures and do not operate properly at low power supplies like 1.2V if they are realized with sub-micron technologies.

In todays technology, circuits which use power supplies as 1V, and fabricated in the CMOS 0.09 μm

technology can be designed and the process improvement works on the CMOS 65 nm technology with a power supply of 0.9V are still going on. The first silicon products in the CMOS 65 nm technology are expected to be announced in the year 2005. Also CMOS 45 nm technology will be available in the year 2007 with a power supply of 0.6V.

So for the future design concept the main interest is designing circuitries with low power supplies. This demand leads designing a high performance CMOS differential OTRA for the current-mode analog systems design. For these reasons, using the STMicroelectronics CMOS 0.13 μm technology, a differential OTRA is designed for 1.2V power supply. This new CMOS differential OTRA topology is characterized by the CADENCE simulation tool and the characteristic results showing its high performance are given.

Low pass and band pass filters with single CMOS differential OTRA structures are tested with simulations to verify the theoretical results.

2. Proposed CMOS Differential OTRA

The Differential Operational Transresistance Amplifier (OTRA) is a four terminal analog building block, besides the power terminals, with a describing matrix in the form given by

$$\begin{bmatrix} V_1 \\ V_2 \\ V_{OA} \\ V_{OB} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ R_m & -R_m & 0 & 0 \\ -R_m & R_m & 0 & 0 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_{OA} \\ I_{OB} \end{bmatrix} \tag{1}$$

Circuit symbol of the differential OTRA is illustrated in Figure 1.

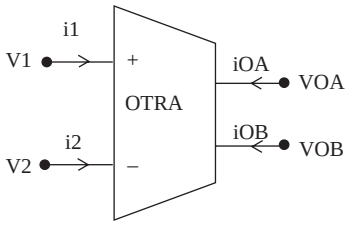

Figure 1. Circuit symbol of the differential OTRA.

Both the input and output terminals are characterized by low impedances. The input terminals are virtually grounded, leading to circuits that are insensitive to the stray capacitance as reported in [4].

For ideal operation, the transresistance gain, R_m approaches infinity forcing the input currents to be equal. Thus the OTRA must be used in a negative feedback configuration in a way that is similar to conventional op amps. OTRA has similar transmission properties to the current-feedback op-amp, but with two low-impedance inputs and two low-impedance outputs for the differential OTRA. Since the input terminals of these circuits are virtually grounded, they are suitable for cascade connection.

2.1. Operational Principles of the Proposed CMOS Differential OTRA

The proposed CMOS differential OTRA is illustrated in Figure 2. This circuitry also includes the four power-down transistors which generates the enabled power-supplies named as "bes" and "top". OTRA is active when the "EN" input is at the VSS voltage level. When the "EN" input is at the VDD voltage level,

all the system is in the power-down mode and the output "VOA" and "VOB" behave as high impedance outputs. Mbes and Mtop transistors need to have high width values in order to have about the same power supply values for the "bes" and "top" power nodes as VDD and VSS. Mbescap and Mtopcap are MOS capacitances, which filter the power supply to ground, and avoid nodes "bes" and "top" from being floating nodes in the power down mode.

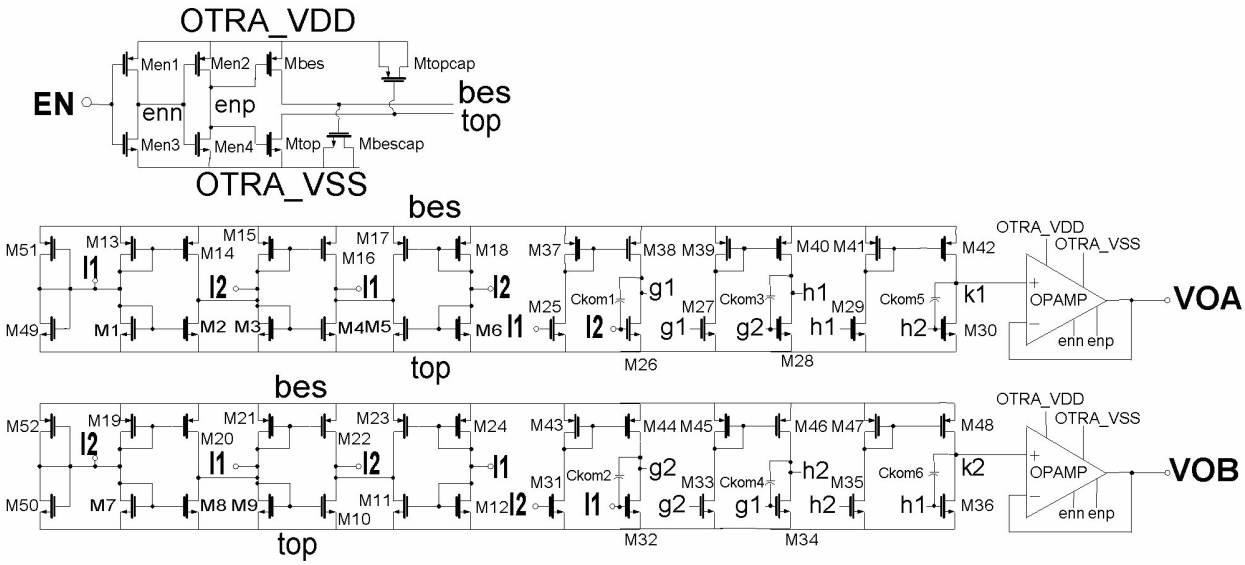

Figure 2. Proposed CMOS differential OTRA topology.

This basic input cell consists of four transistors which is illustrated in Figure 3. These four transistors generate two Class AB current mirror connection [8]. In the static state I1 and I2 are biased automatically to the half of the power supply. For this design the initial value for I1 and I2 is 0V as virtually grounded (in $\pm$ 0.6V power supply operation). The input currents are directly connected to the I1 and I2 nodes. So the input currents directly flow through the drains of the transistors. If one basic cell is used, the OTRA input will not be symmetrical. Because, for the given basic cell, the input I1 is formed by the use of two diode connected NMOS (M9) and PMOS (M21) transistors, but at the input I2 there are no diode connections. For that reason, a second basic cell is placed into the design, by replacing the input pins, that input I2 is applied to the two diode connected input part of the basic cell and input I1 is applied to the other input as given in Figure 2 (the transistors M3, M4, M15 and M16 in the top-middle level).

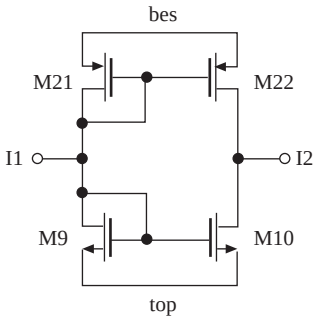

Figure 3. Basic cell of the input part in the proposed differential OTRA.

Afterwards in order to decrease the process variation effects and to have a stronger input part, four basic cells are also connected to this block as illustrated in Figure 2. Totally both inputs I1 and I2 are formed

with three diode-connected NMOS, three diode-connected PMOS, and one not-diode-connected NMOS and one not-diode-connected PMOS transistors. The inputs I1 and I2 are also connected to the differential amplifier in the gain stage. This negative feedback is helping to decrease the input impedance in I1 and I2 nodes. Also one-pair of diode-connected NMOS and PMOS transistors which have large width values are connected both to the inputs I1 and I2 in order to decrease the input impedance of the I1 and I2 nodes which are the input nodes for the OTRA. This connection also can be thought as an inverter whose output is connected to its own input. The only disadvantage of this connection is using more current from the power supply.

The basic cell of the gain part is composed of four transistors, namely M25, M26, M37 and M38 as illustrated in Figure 4. This differential amplifier is not a classical amplifier with a fixed current source biasing the NMOS transistors M25 and M26. This amplifier can operate independent of any fixed current. This cell is converting the two input differential signals to one single ended signal.

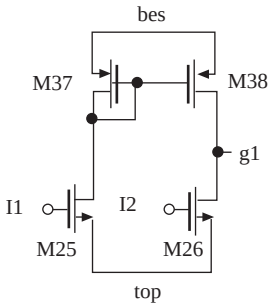

Figure 4. Basic cell of the gain stage in the proposed differential OTRA

In order to have a symmetrical output at g1 and g2 nodes, two basic cells are used, which have the same idea in the input part of the OTRA. For the second basic cell which composed with the transistors M31, M32, M43 and M44 illustrated in Figure 2, the input pins are reversed. So both I1 and I2 inputs are directly connected to one diode-connected PMOS (M37 and M43) and one not-diode-connected PMOS (M44 and M38).

The first gain outputs which are "g1" and "g2" in names, are connected to the second same structured gain stage like the first gain stage. The outputs of the second gain stage which are "h1" and "h2" in names, are connected to the third, same structured gain stage as the first gain stage. The outputs of the third gain stage which are "k1" and "k2" in names are the non-buffered dual outputs of differential OTRA.

The non-buffered dual outputs are buffered with the unity-gain configuration, illustrated in Figure 2, by using the OPAMP which is illustrated in Figure 5. The VOA is the same functional output as the VO in the classical single output OTRA, VOB is the dual output of VOA, which is just differ from the VOA output in the phase level.

2.2. Operational Principles of the Proposed CMOS OPAMP

For the rail-to-rail input voltage operations, a new CMOS OPAMP has been designed and it is illustrated in Figure 5. In this opamp, input differential amplifiers are used both in NMOS and PMOS combinations as in the OPAMP proposed in 1997 [9]. The rail-to-rail input stage, composed with the transistors named from M1 to M6 are illustrated in Figure 5.

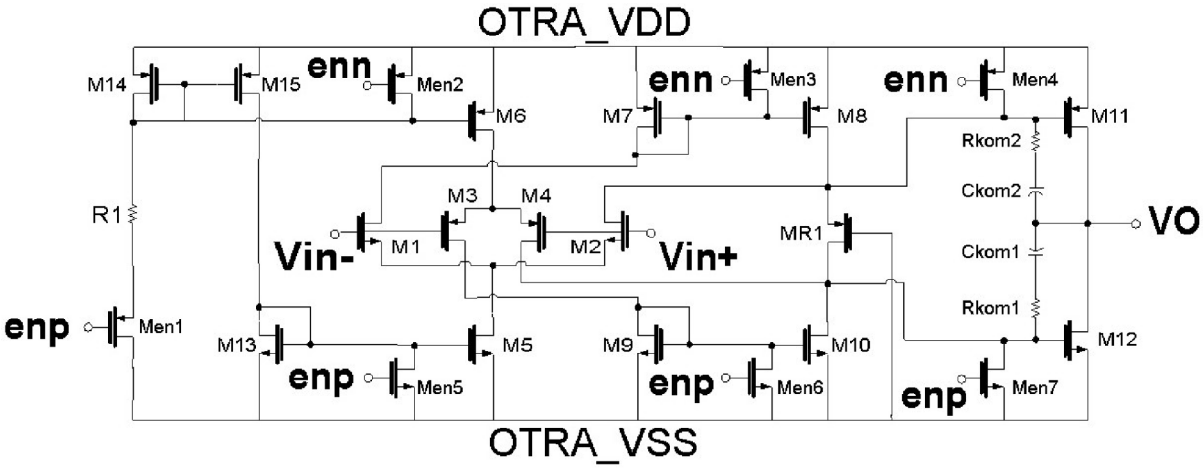

Figure 5. New proposed CMOS OPAMP used in the OTRA as a unity gain output buffer.

For low input common-mode voltages, only the PMOS pair (M3-M4) is active, for high input common-mode voltages only the NMOS pair (M1-M2) is active. For middle-level input common mode voltage values, both pairs are "ON", but each with reduced contribution. The outputs of these amplifiers are applied to the current mirrors M7-M8 and M9-M10. Between M8 and M10 a PMOS transistor named MR1 is connected. This transistor behaves as a resistor in order to achieve the necessary bias voltage for the output stage to operate in Class AB. The voltage on the resistor behaved the transistor MR1 directly applied to the large output transistors M11 and M12. The output impedance of the OPAMP is very low because of the large output transistors. Also 200 fF compensation capacitances and 500 Ω resistors are connected to the output transistors.

The biasing current stage of the OPAMP is generated with an internal resistor and simple current mirrors.

3. Characterization of the CMOS Differential OTRA and OPAMP

In this part, the characterization results of the proposed CMOS differential OTRA and OPAMP will be given in details.

3.1. Characterization of the CMOS Differential OTRA

The proposed CMOS differential OTRA, is simulated using CADENCE simulation program, and the STMicroelectronics CMOS 0.13 μm technology *spectre* models (version 8.0.4). The transistor dimensions and element values for CMOS differential OTRA and CMOS OPAMP are listed in Tables 1 and 2. Power supplies are chosen as $\pm$ 0.6V, and the operating temperature is taken as 27 °C . The load capacitances used in the simulations are 5 pF.

The typical dc simulation results are shown in Figures 6 and 7. According to these results the maximum output voltages are reached with at least 200 μA of input difference current. The maximum output voltage in the dc analysis is 0.474mV, and the minimum output voltage is -0.474mV with 200μA input current. Another typical dc test simulation result is shown in Figure 8. According to these results, it is shown that this OTRA can operate within the limits of -2 mA and 2 mA. If one of the input node is biased with more 2 mA, it is also possible to operate. But the 2mA input current limit will be much more than enough for a classical operation.

Table 1. Transistor dimensions (W/L) and other devices values in the proposed CMOS OTRA.

Transistor names	**W / L**
M1, M2, M3, M4, M5, M6, M7, M8, M9, M10, M11, M12	3.4 μm / 0.15 μm
M13, M14, M15, M16, M17, M18, M19, M20, M21, M22, M23, M24	8.16 μm / 0.15 μm
M25, M26, M27, M28, M29, M30, M31, M32, M33, M34, M35, M36	0.85 μm / 0.15 μm
M37, M38, M39, M40, M41, M42, M43, M44, M45, M46, M47, M48	2.04 μm / 0.15 μm
M49, M50	108.8 μm / 0.15 μm
M51, M52	380.8 μm / 0.15 μm
Men1, Men2	28.8 μm / 0.13 μm
Men3, Men4	13.6 μm / 0.13 μm
Mbes	561 μm / 0.15 μm
Mtop	140 μm / 0.15 μm
Mbescap, Mtopcap	67.84 μm / 5.28 μm
Other devices	**Value**
Ckom1, Ckom2, Ckom3, Ckom4, Ckom5, Ckom6	10 fF

Table 2. Transistor dimensions (W/L) and other devices values in the proposed OPAMP.

Transistor names	**W / L**
M1, M2	8.5 μm / 0.3 μm
M3, M4	41 μm / 0.3 μm
M5	13.6 μm / 0.4 μm
M6	32.64 μm / 0.4 μm
M7, M8	12.24 μm / 0.3 μm
M9, M10	5.1 μm / 0.3 μm
M11	440 μm / 0.3 μm
M12	170 μm / 0.3 μm
M13	3.4 μm / 0.3 μm
M14, M15	8.16 μm / 0.3 μm
MR1	2 μm / 4 μm
Men1	43.2 μm / 0.13 μm
Men2, Men3, Men4	0.4 μm / 0.13 μm
Men5, Men6, Men7	3.4 μm / 0.13 μm
Other devices	**Value**
Ckom1, Ckom2	200 fF
Rkom1, Rkom2	500 Ω
R1	6 KΩ

The normalized transresistance gain is shown in Figure 9. The transresistance gain is 7478 V/I. The -3 dB frequency of the transresistance gain is at 28.1 MHz. It is a good range for the CMOS 0.13 μm technology. Also the unity gain-bandwidth is 2 GHz. This bandwidth region gives the oppurtunity of designing high bandwidth filters and inductance simulators.

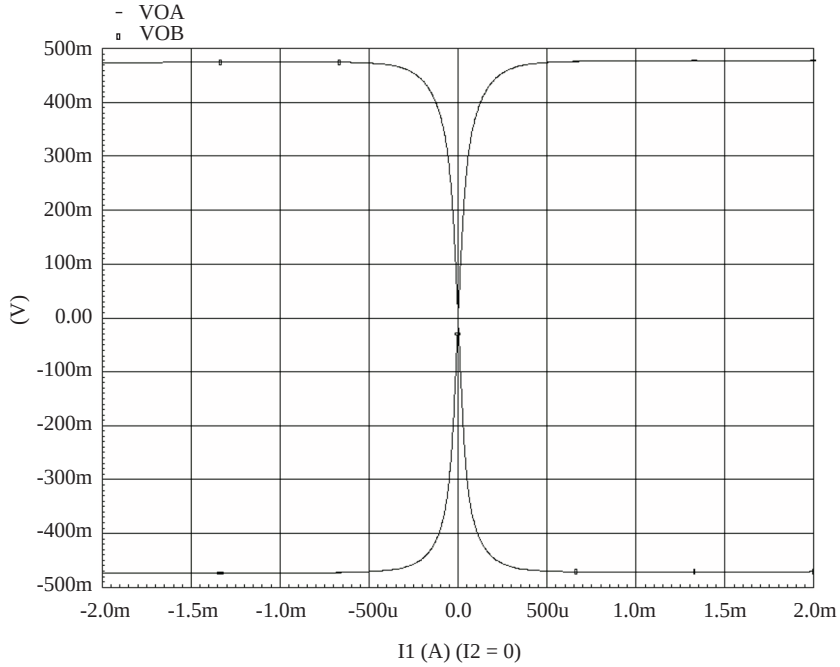

Figure 6. Typical dc simulation result of CMOS differential OTRA.

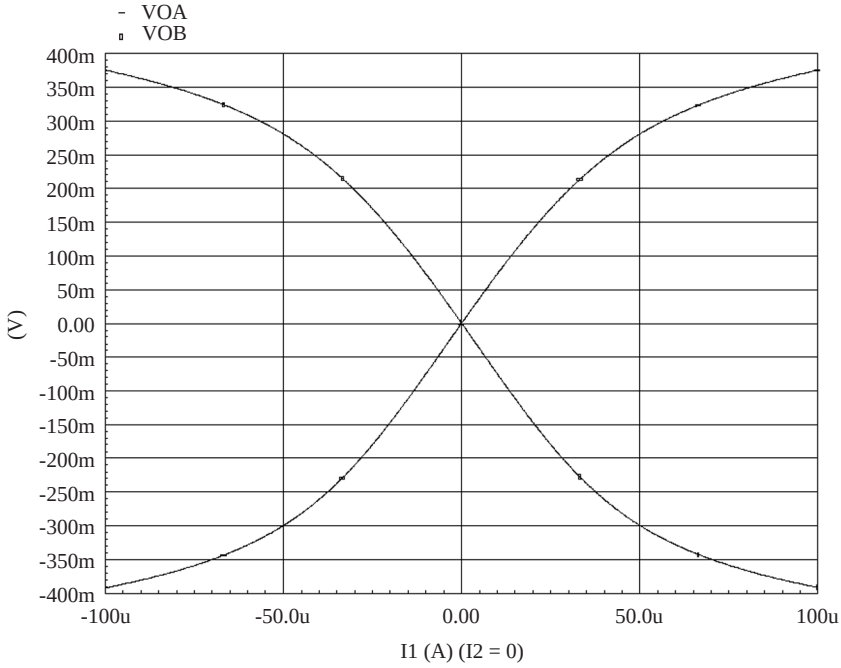

Figure 7. Zoomed typical dc simulation result of CMOS differential OTRA.

The performance characteristics of the CMOS differential OTRA is given at the Table 3.

3.2. Characterization of the CMOS OPAMP

The proposed OPAMP, is simulated using CADENCE simulation program, and the STMicroelectronics CMOS 0.13 μm technology *spectre* models (version 8.0.4). The transistor dimensions and element values for

CMOS OPAMP are listed in Table 2. Power supplies are chosen as $\pm$ 0.6V, and the operating temperature is taken as 27 °C. The load capacitance used in the simulations is 5 pF, and the load resistor is 1 MΩ.

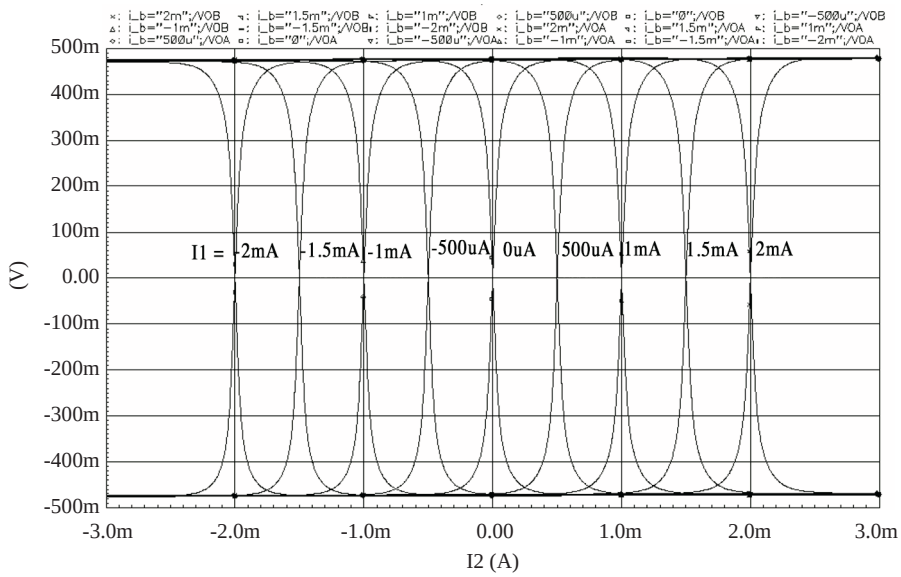

Figure 8. Typical dc simulation of CMOS differential OTRA with different I1 input currents.

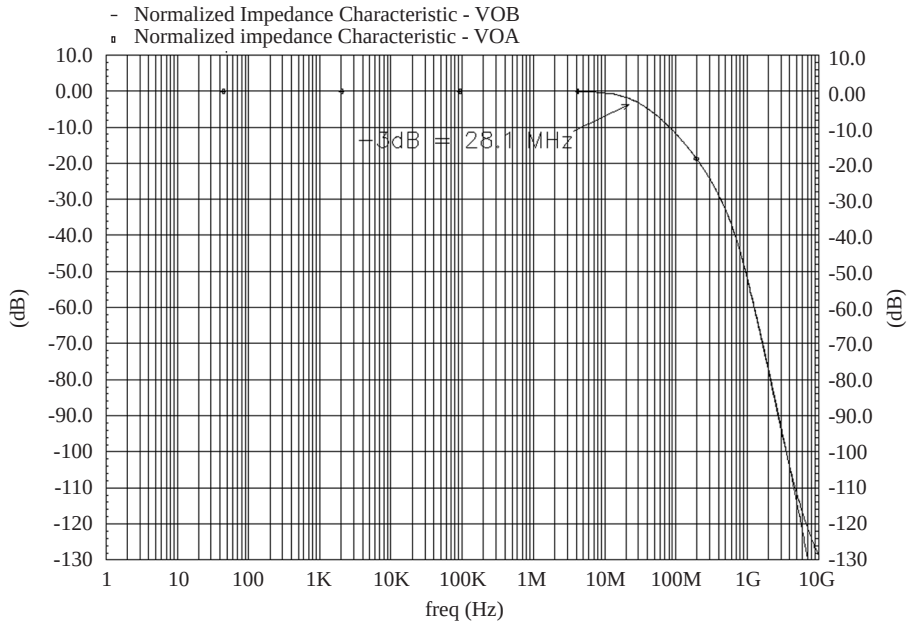

Figure 9. Typical ac simulation result, transresistance gain of the CMOS differential OTRA in a normalized axis.

The gain and the phase simulation results of the compensated OPAMP in the open-loop are shown in Figures 10 and 11, respectively. According to these results the phase margin of the OPAMP is 50.6°C, and the gain margin of the OPAMP is 14.4 dB.

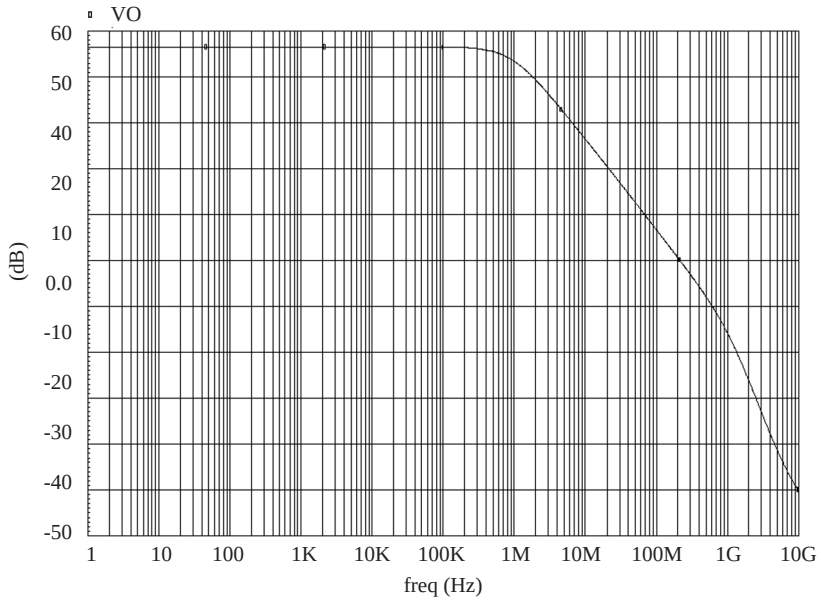

Figure 10. Typical ac simulation result, gain of the compensated OPAMP in the open-loop.

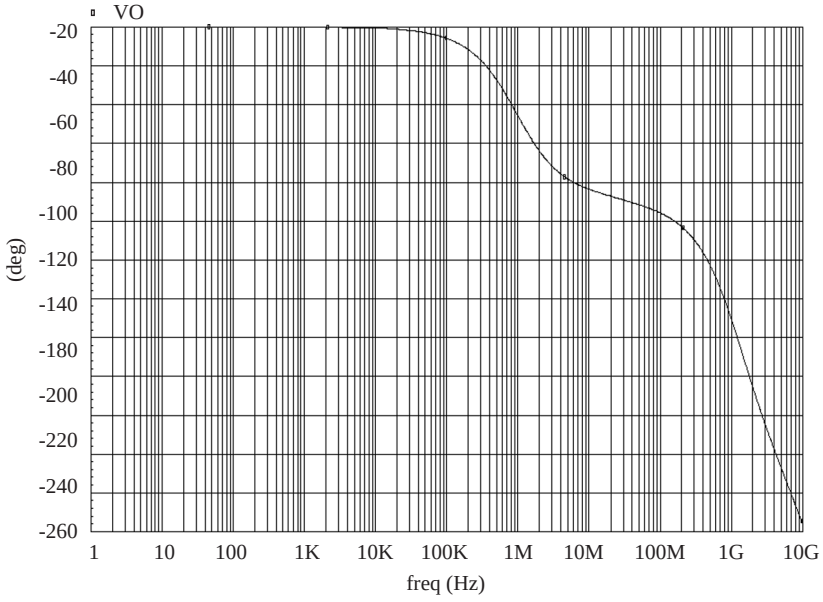

Figure 11. Typical ac simulation result, phase of the compensated OPAMP in the open-loop.

The input-output dc relation is given in the unity gain configuration is given in the Figure 12. The voltage difference error between the ideal and the simulation result is lower than 1mV in the $\pm$ 440mV voltage levels.

The ac simulation results of the unity-gain OPAMP is given in Figure 13. The cut-off frequency (-3 dB) of the unity-gain OPAMP is 1.088 GHz. A 25 MHz sinus signal is applied to the unity-gain OPAMP, the output is given in Figure 14. The tracking error between the input and output signals are 2mV.

The performance characteristics of the CMOS OPAMP is given at the Table 4.

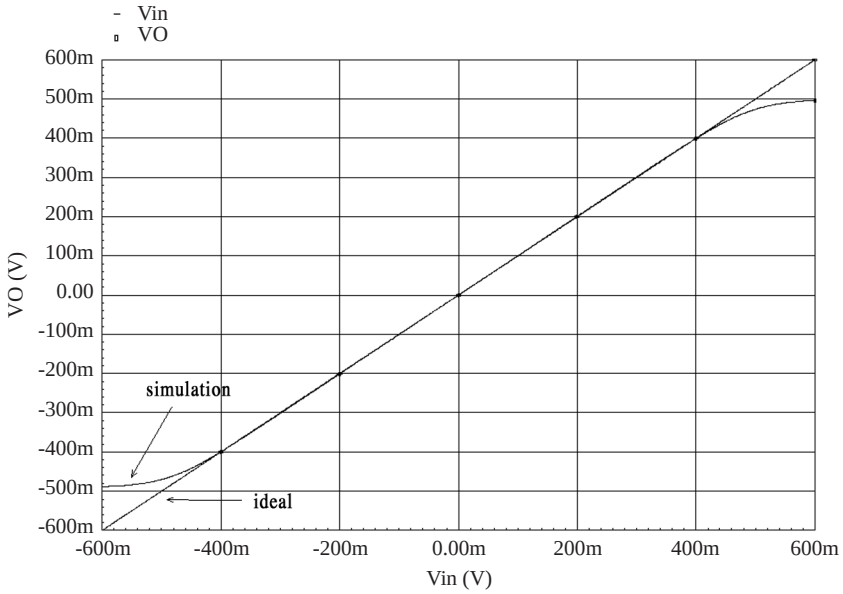

Figure 12. Typical dc input-output relation of OPAMP, in unity-gain configuration.

Table 3. Performance of the proposed CMOS differential OTRA.

Power supply	±0.6 V
Maximum output voltage	0.474 V
Minimum output voltage	-0.474 V
Input resistance	$R\_I_1 = R\_I_2 = 9.3\ \Omega$
Output resistance	0.6 Ω
Input offset current	42 nA
Transresistance gain (Rm) (DC)	7478 V/I
Transresistance gain bandwidth (-3dB)	28.1 MHz
Transresistance unity gain-bandwidth	2 GHz
Power consumption	34 mA, 40.8 mW
Expected silicon area	60 μm × 50 μm

Table 4. Performance of the proposed CMOS OPAMP.

Power supply	±0.6 V
Maximum output voltage	0.490 V
Minimum output voltage	-0.485 V
Output resistance	0.6 Ω
Input offset voltage	2.3 μV
Gain Margin	14.4 dB
Phase Margin	50.6°C
Unity gain-bandwidth	1.088 GHz
Power consumption	5.3 mA, 6.36 mW

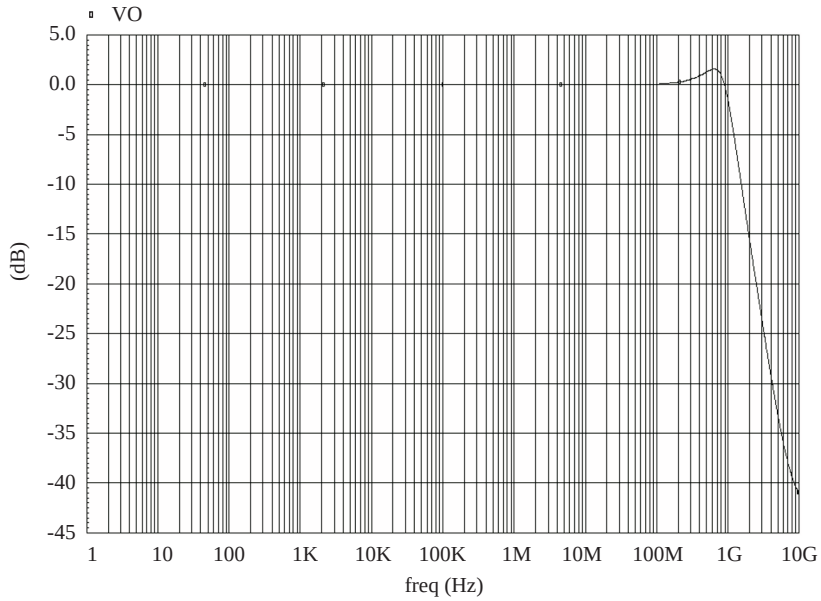

Figure 13. Typical ac simulation result, gain of the unity-gain OPAMP.

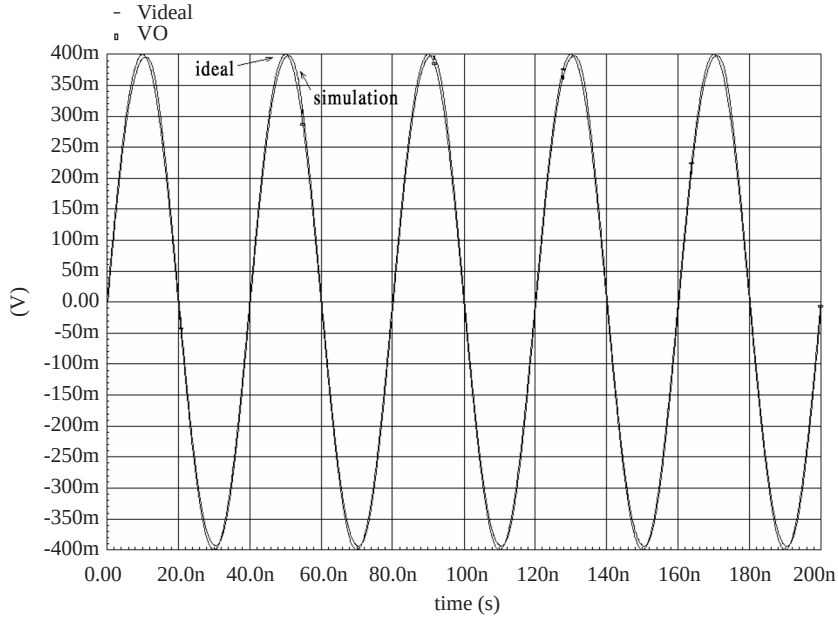

Figure 14. Output of the unity-gain OPAMP for the 25MHz input sinus signal.

4. Design Examples and Simulation Results

The performance of the CMOS differential OTRA proposed is demonstrated on a design example of single input dual output filter structure.

The filter topology illustrated in Figure 15 performs band pass at the output node V_{01} and low pass responses at the output node V_{02}. The transfer function of the two output nodes are given by (2) and (3).

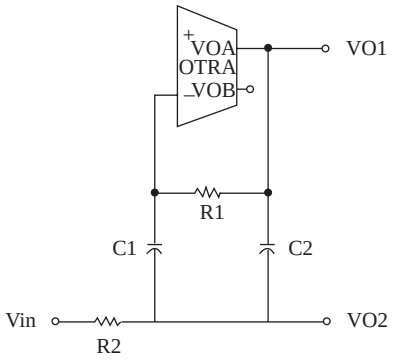

Figure 15. The band pass and low pass filters with OTRA.

Transfer function for the band pass output in the node V_{01},

$$H_1(s) = -\frac{C_1 G_2 s}{G_1 G_2 + C_1 G_1 s + C_2 G_1 s + C_1 C_2 s^2} \tag{2}$$

Transfer function for the low pass output in the node V_{02},

$$H_2(s) = \frac{G_1 G_2}{G_1 G_2 + C_1 G_1 s + C_2 G_1 s + C_1 C_2 s^2} \tag{3}$$

When the passive element values are chosen as $C_1 = C_2$ and $G_2 = 2.G_1$, the following transfer functions are calculated for the band pass (H_1) and the low pass (H_2) characteristics,

$$H_1(s) = -\frac{2C_1 G_2 s}{G_2^2 + 2C_1 G_2 s + 2C_1^2 s^2} \tag{4}$$

$$H_2(s) = \frac{G_2^2}{G_2^2 + 2C_1 G_2 s + 2C_1^2 s^2} \tag{5}$$

The cut-off frequency for both band pass and low pass filters is given by (6).

$$f_{1(-3dB)} = f_{2(-3dB)} = \frac{1}{2\pi\sqrt{2}C_1 R_2} \tag{6}$$

The quality factor of this filter is $Q = \sqrt{2}/2$

A second filter topology can be obtained by the RC and CR transformation in Figure 15 which performs band pass at the output node V_{01} and high pass responses at the output node V_{02}. The cut-off frequency of this filter is also given by equation (6).

The CMOS OTRA filter, is simulated using CADENCE simulation program, and the STMicroelectronics CMOS 0.13 μm technology *spectre* models (version 8.0.4). The transistor dimensions and element values for CMOS differential OTRA and CMOS OPAMP are listed in Tables 1 and 2. Power supplies are chosen as $\pm$ 0.6V, and the operating temperature is taken as 27 °C.

For the band-pass and the low pass filters illustrated in Figure 15, $C_1 = C_2 = 20$ pF, $R_1 = 500\ \Omega$, $R_2 = 250\ \Omega$ are chosen. The dc transresistance gain (Rm) of the proposed CMOS OTRA is 7478 V/I.

The theoretical cut-off frequency of the band pass and low pass filters is $f_{-3dB(\text{teo})} = 22.508$ MHz, and for the OTRA, the simulated cut-off frequency for the band pass filter is $f_{-3dB(\text{sim})} = 22.39$ MHz, the difference because of the non-idealities of the OTRA is % 0.52. The simulated gain of the filter is 0.863 (–0.91 dB). For the OTRA, the simulated cut-off frequency for the low pass filter is $f_{-3dB(\text{sim})} = 21.54$ MHz, the difference because of the non-idealities of the OTRA is % 4.3. The simulated gain of the filter is 1 (0 dB). The performance of the ideal and the simulated band pass and low pass filters for OTRA are shown in Figure 16.

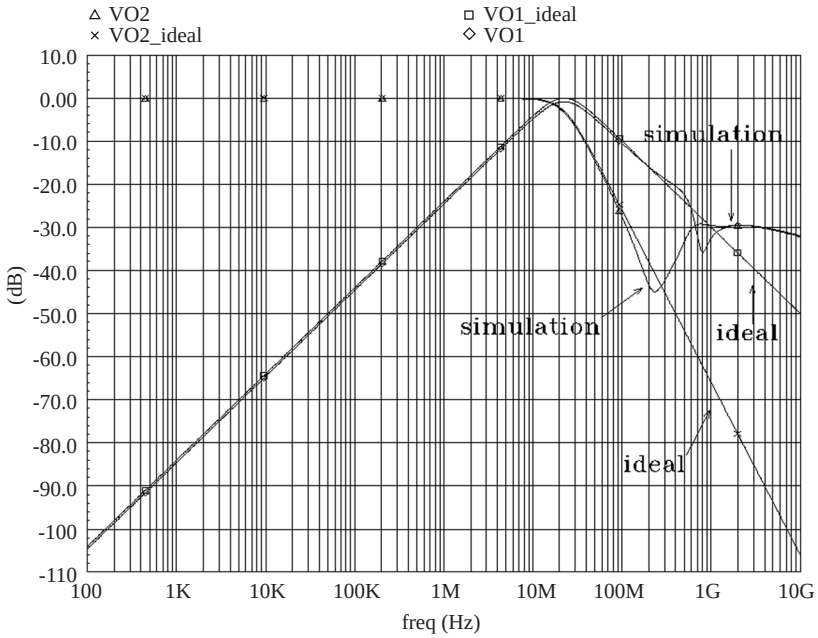

Figure 16. Band pass and low pass filter characterizations of the ideal and the simulated CMOS OTRA with a typical ac simulation.

For another low pass filter with smaller capacitance values, illustrated in Figure 15, $C_1 = C_2 = 2.5$ pF, $R_1 = 4\ \text{K}\Omega$, $R_2 = 2\ \text{K}\Omega$ are chosen.

The theoretical cut-off frequency of the band pass and low pass filters is $f_{-3dB(\text{teo})} = 22.508$ MHz, and for the OTRA, the simulated cut-off frequency for the low pass filter is $f_{-3dB(\text{sim})} = 18.65$ MHz, the difference because of the non-idealities of the OTRA is % 17.14. The simulated gain of the filter is 1 (0 dB). The performance of the ideal and the simulated band pass and low pass filters for OTRA are shown in Figure 17.

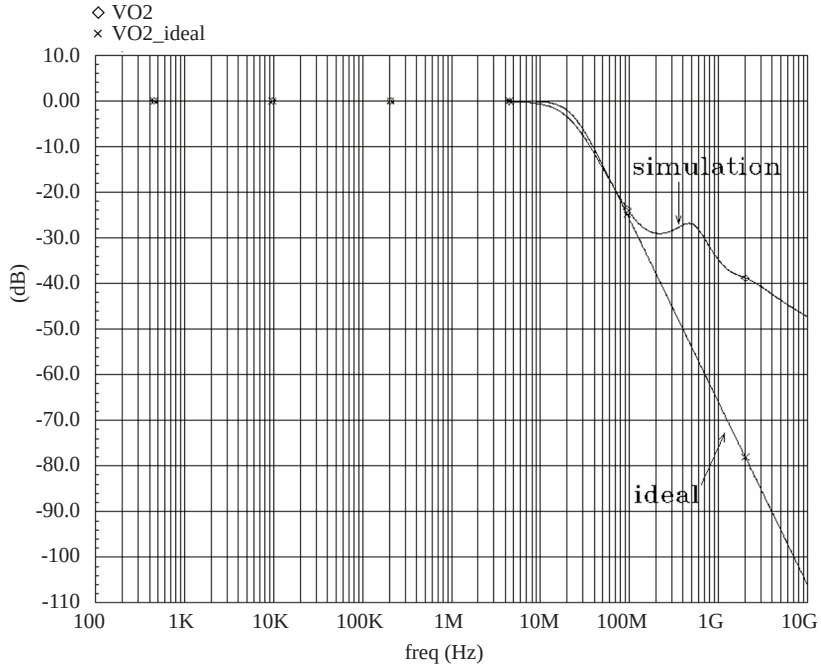

Figure 17. Low pass filter characterizations of the ideal and the simulated CMOS OTRA with a typical ac simulation.

5. Conclusion

In this study, a new CMOS differential OTRA for the low power supplies like 1.2V is proposed. This current-mode active element is suitable for high frequency applications, including filter, inductance simulator applications. Characterization simulations of the differential OTRA is done with the CADENCE tool and 28.1 MHz transresistance gain bandwidth is achieved.

Low pass and band pass filters with single CMOS differential OTRA structures are tested with simulations to verify the theoretical results. The results are very close to the theoretical ones.

This CMOS differential OTRA structure is also very suitable for the high frequency (up to 3.2 GHz) differential signalling receiver I/O circuitry in the *SONET / SDH* (Synchronous Optical Network / Synchronous Digital Hierarchy) or *XAUI* (10 Gigabit Attachment Unit Interface – 10 Gigabit Ethernet) chipsets. Both LVDS (Low voltage differential signalling) and CML (Current-mode logic) receivers can be easily designed by removing the large input diode-connected transistors and by replacing the buffers connected to the output with the inverter based buffer chains. These input and output structures in OTRA, which are removed for the receiver I/O circuitry, have the function of lowering the input and the output resistances to very low values.

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