Turk J Elec Engin, VOL.14, NO.3 2006, © TÜBİTAK

Statistical Model of Hot-Carrier Degradation and Lifetime Prediction for P-MOS Transistors

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Abstract

Along with advances in microelectronics, and computer and space technologies, device dimensions are becoming smaller; as a result, hot-carrier effect, lifetime prediction, and reliability become more important concepts for MOS transistors.

In this paper, the degradation in the drain current and threshold voltage of P-MOS transistors are observed by operating the devices under voltage stress conditions. Using the observation results, the effect of hot-carriers was investigated statistically and a new statistical method for modeling was proposed as an alternative to those given in the literature. The linear regression method is used to estimate the power, Weibull, and logarithmic parameters, and the correlation coefficient is used to confirm the results. The observed and estimated values of the degradation are compared. SPICE simulation of a CMOS inverter was performed to demonstrate how the proposed method can be applied to a circuit example.

Key Words: *Hot-carrier, P-MOS transistor, lifetime prediction, statistical methods, MOS models.*

1. Introduction

The down-scaling of device dimensions in MOS technology will improve performance and packing density for VLSI circuits, but will negatively affect the quality of the circuits. Basically, integrated circuits are classified according to the electrical function they perform. The concept of quality is used to express how well the required function is performed.

Several works have been conducted on hot-carrier effect, which is one of the most important factors that influence the reliability of MOS structures [1-23].

The reliability of a system is defined as the probability that it will perform its required function under stated conditions for a stated period of time. In most reliability studies on the modeling of the hot-carrier effect available in the literature, models based on physical properties have been proposed [1-8, 23]; however, difficulties in preparation of physical models, losing the actuality within the advances in the technology, and excessively long simulation times seem to be disadvantages of these models.

To overcome these disadvantages of physical models, a statistical method that is based on the observation results, independent of the technology, and that exhibits a short simulation time and high accuracy has been introduced in this work. Starting with experimental results of Siemens AG., Munich, Germany [23], the effect of hot-carriers on the drain current and threshold voltage of P-MOS transistors was statistically investigated and a statistical model was proposed as an alternative to those available in the literature. The time-dependent statements of degradation were obtained by using 3 different statistical methods. Coefficients were optimized with these methods and functions were generated. These functions gave variations of drain current with time and channel length. The proposed method is based on the measurement results, is independent of the technology, and can be easily applied to P-MOS transistors with different dimensions.

2. P-MOS Degradation

P-MOS degradation occurs only if electrons are trapped in the gate oxide due to the impact ionization of hot-holes [1-9]. This is known as the drain avalanche hot carrier mechanism and is shown in Figure 1. When the P-MOS transistor is operating in the saturation region, holes move from the source to the drain and are accelerated by the high electric field at the drain end of the channel. If a hole has energy of at least 1.5 eV, then it can be concluded with impact ionization. After impact ionization, the rise of the new hole moves to the drain, as do the other holes, and it increases the drain current (I_D) a small amount. Most of the new electrons, after impact ionization, move to the substrate, forming the substrate current (I_B). Nevertheless, some of these electrons, if they have an energy at least of 3.1 eV and the right direction, they surmount the $Si\text{-}SiO_2$ potential barrier and are injected into the gate oxide. The electric field strength direction in the gate oxide above the depletion region causes the electron to accelerate to the gate. Most of the electrons in the gate oxide reach the gate from the gate current (I_G), which corresponds greatly with the drain current (I_D). Yet, the existing traps in the oxide can capture some of the electrons, and these captured electrons behave like fixed negative charges. Electrons that are injected into the gate oxide can damage the $Si\text{-}SiO_2$ interface. These interface defects are partially filled by the holes in the non-saturation operation. Therefore, this degradation effect on a MOSFET will be ignored. The fixed negative charges of the captured electrons cause an increase in the drain current in all regions of operation; however, the largest degradation will be in the saturation operation. For short channel MOSFETs, the threshold voltage (V_{th}) will also change to lower values.

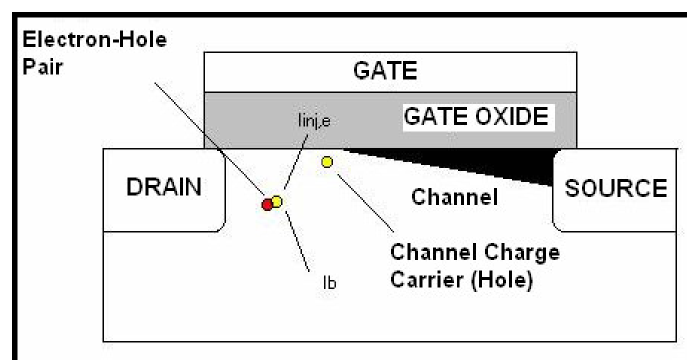

Figure 1. Hot-carrier formation mechanism of P-MOS transistors.

3. Statistical Methods

This study was performed for 3 different transistors produced with the same technology, but with different channel lengths. Process parameters of the transistors are given as: t_{ox} = 20 nm and x_j = 400 nm; the dimensions are W = 10 μm and L = 1.5 μm, 2 μm, and 3 μm. Stress voltage was applied to the transistors for 16 h. Statistical methods were applied and investigated using variations of the drain currents and threshold voltages with time, which were obtained as a result of applied stress voltages (V_D = 0.5 V, V_D = 2.5 V, V_G = 1.5 V, V_G = 2 V, and V_G = 2.5 V).

The investigated methods were:

- power method: F(t) = a.t^b
- Weibull method: F(t) = 1-exp [- $(t/a)^b$]
- logarithmic method: F(t) = a + b ln(t)

where for all methods
t = time
a = scale parameter
b = shape parameter.

Calculations were based on the linear regression method for all 3 approaches and the least squares method was used [14-17]. Exponential and logarithmic parameters, and power distribution with the least squares method are given by the following equations. Calculations were performed using the MATLAB program.

Exponential Distribution with the Least Squares Method

$$y = Ae^{Bx} \tag{1}$$

$$a = \frac{\sum_{i=1}^{n} \ln y_i \sum_{i=1}^{n} X_i^2 - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} x_i \ln y_i}{n\sum_{i=1}^{n} x_i^2 - (\sum_{i=1}^{n} x_i)^2} \tag{2}$$

$$b = \frac{n\sum_{i=1}^{n} x_i \ln y_i - \sum_{i=1}^{n} x_i \sum_{i=1}^{n} \ln y_i}{n\sum_{i=1}^{n} x_i^2 - (\sum_{i=1}^{n} x_i)^2} \tag{3}$$

$B \equiv b$ and $A \equiv \exp(a)$.

Logarithmic Distribution with the Least Squares Method

$$y = a + b\ln x \tag{4}$$

$$b = \frac{n\sum_{i=1}^{n} (y_i \ln x_i) - \sum_{i=1}^{n} y_i \sum_{i=1}^{n} \ln x_i}{n\sum_{i=1}^{n} (\ln x_i)^2 - (\sum_{i=1}^{n} \ln x_i)^2} \tag{5}$$

$$a = \frac{\sum_{i=1}^{n} y_i - b\sum_{i=1}^{n} (\ln x_i)}{n} \tag{6}$$

Power Distribution with the Least Squares Method

$$y = Ax^B \tag{7}$$

$$b = \frac{n\sum_{i=1}^{n}(\ln x_i \ln y_i) - \sum_{i=1}^{n}(\ln x)\sum_{i=1}^{n}(\ln y_i)}{n\sum_{i=1}^{n}(\ln x_i)^2 - (\sum_{i=1}^{n}\ln x_i)^2} \tag{8}$$

$$a = \frac{\sum_{i=1}^{n}(\ln y_i) - b\sum_{i=1}^{n}(\ln x_i)}{n} \tag{9}$$

$B \equiv b$ and $A \equiv e^a$.

4. Numerical Results

Experimental results for P-MOS transistors at different stress conditions are summarized in the 3-dimensional plots of $I_D = I_D(L,t)$ in Figure 2.

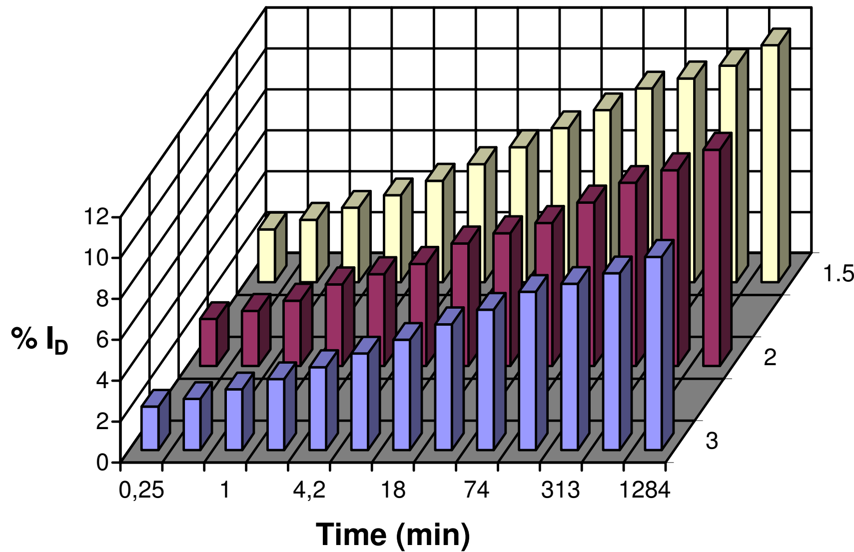

Figure 2. Experimentally determined dependence of the drain current on channel length and stress time.

As can be observed from Figure 2, drain current increases with stress time, and I_D decreases with channel length. On the other hand, based on a previous study [24], it can be easily observed that the drain current and the threshold voltage of N-MOS transistors decrease with time. For $L = 1.5\ \mu$m, the change in the drain current is approximately 4% for P-MOS, while it is 0.8% for N-MOS. It seems that P-MOS transistors are more affected by hot-carriers. The power, logarithmic, and Weibull parameters were calculated using experimental data and the linear regression method, including Equations (1-9). The functions obtained by using the investigated methods that gave the percent changes in drain currents and threshold voltages are given in Table 1.

Coefficients were optimized with these methods and functions were generated. These functions gave variation of drain current with time and channel length. The function coefficients for different operating conditions obtained by the 3 methods can be seen in Table 2.

Table 1. Obtained functions of the investigated methods.

Investigation method	Obtained function
Power	$\% \ I_D(t,L) = k. \ L^{m}.t^{n}$
Logarithmic	$\% \ I_D(t,L) = k \ . \ L^m + n. \ \ln(t)$
Weibull	$\% \ I_D(t,L) = 1\text{-}\exp(-(t/k.L^m)^n$

Table 2. Obtained function coefficients of P-MOS transistors for different methods.

	Power	Logarithmic	Weibull
$I_D(V_D = 0.5$ V)	k = 3.158 m = -1.175 n = 0.1216	k = 3.036 m = 1.199 n = 0.583	k = 270 m = 3.62 n = 0.174
$I_D(V_D = 2.5$ V)	k = 1.372 m = -1.818 n = 0.156	k = 1.261 m = 1.115 n = 0.370	k = 40052 m = 4.7 n = 0.181
$I_D(V_G = 1.5$ V)	k = 3.264 m = -1.982 n = 0.156	k = 3.005 m = 1.982 n = 0.8833	k = 16400 m = 2.95 n = 0.26
$I_D(V_G = 2$ V)	k = 1.662 m = -1.677 n = 0.156	k = 1.531 m = 1.719 n = 0.4498	k = 13160 m = 5.547 n = 0.36
$I_D(V_G = 2.5$ V)	k = 1.513 m = -1.758 n = 0.156	k = 1.393 m = 1.741 n = 0.4094	k = 26340 m = 3.44 n = 0.48

Results calculated from the equations in Table 1 are compared with experimental results. It has been observed that the logarithmic method seems to be the best statistical method that characterizes the measurement results. The characterization results using the logarithmic method are given with experimental results in Figures 3-5.

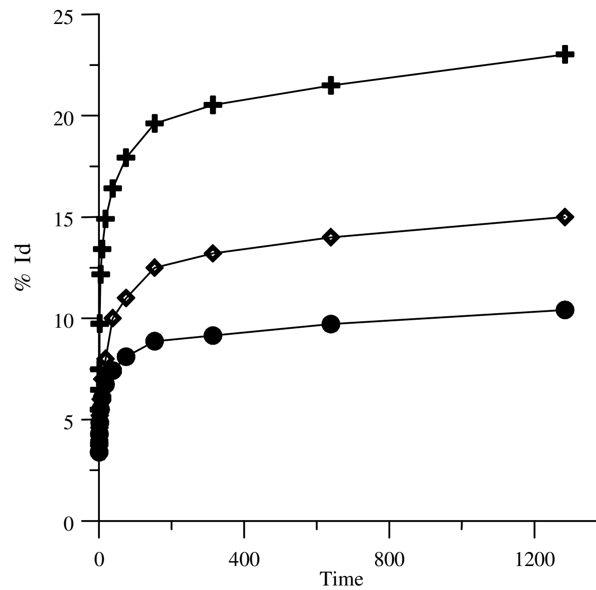

Figure 3. Measured L = 1.5(+) , 2 (◇), and 3(•) μm, and calculated (—) I_D % variations with the logarithmic method for different channel lengths ($V_D = 0.5$ V).

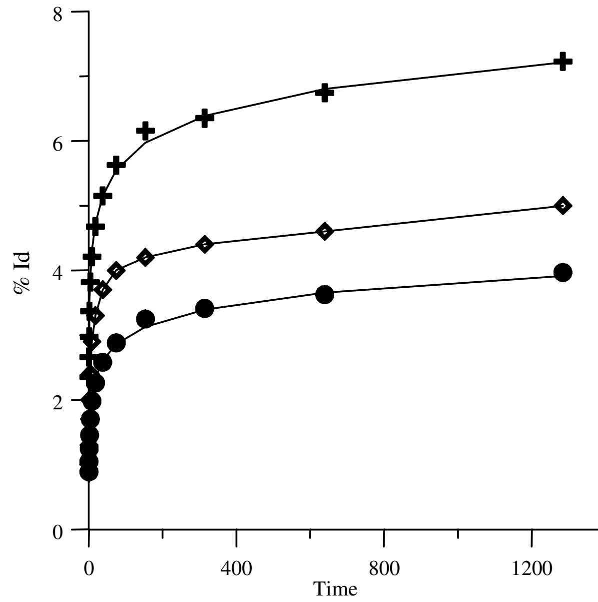

Figure 4. Measured L = 1.5(+) , 2 (◇), and 3(•) μm ,and calculated (—) I_D % variations with the logarithmic method for different channel lengths (V_D = 2.5 V).

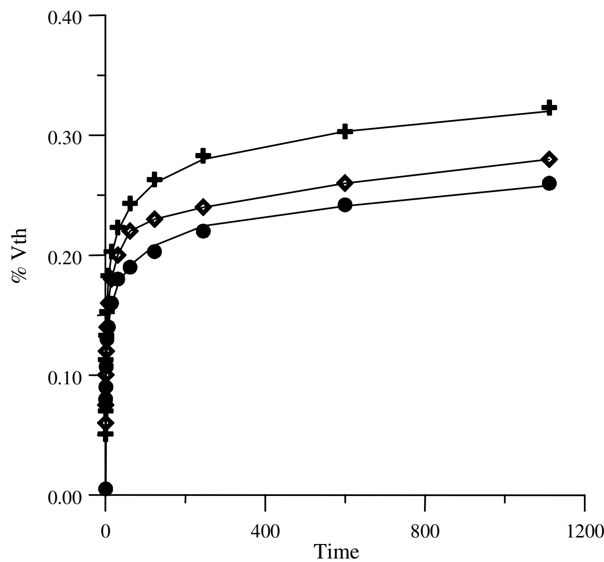

Figure 5. Measured L = 1.5(+), 2 (◇), and 3(•) μm, and calculated (—) V_{TH} % variations with the logarithmic method for different channel lengths (V_D = 2.5 V).

It seems from the figures that there is good agreement between the experimental results and the calculated values. To show the similarity between the measured and calculated values, correlation coefficients were calculated and very high correlation coefficients were obtained. The results obtained can be seen in Table 3. Moreover, error calculations were achieved with the RMS method and the results are given in Table 4. It can easily be observed that the error values are very low. With respect to the graphics, the table of correlation coefficients, and the table of RMS errors, the methods are classified from the best to worst as the logarithmic, power, and Weibull methods, respectively.

Table 3. Obtained correlation coefficients for P-MOS.

	Logarithmic	Power	Weibull
Id (Sub-threshold)	0.998482	0.990399	0.997737
Id (Inversion)	0.997117	0.988502	0.992571
Vth	0.998128	0.952594	0.9587

Table 4. Obtained RMS errors for P-MOS.

	Logarithmic	Power	Weibull
Id (Sub-threshold)	0.03111	0.07891	0.04356
Id (Inversion)	0.02728	0.05528	0.04657
Vth	0.01377	0.08093	0.08590

5. Proposed P-MOS Model

It is clearly seen that the drain current and the threshold voltage of the P-MOS transistor increase with time. An appropriate model was designed to represent the hot-carrier effect of the transistors in this work. With the help of the obtained time-dependent functions, a solution was formed for the increasing value of the drain current by the connection of a dependent current source between the drain and source of the P-MOS transistor, which was formed for increasing the value of the threshold voltage by the connection of a dependent voltage source to the gate. The proposed model for the P-MOS can be seen in Figure 6.

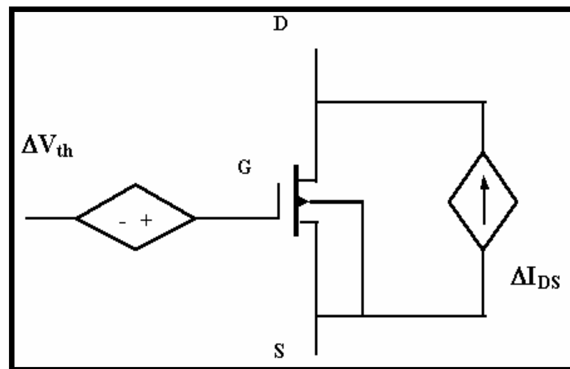

Figure 6. Model to represent time-dependent variation of drain current and threshold voltage caused by the hot-carrier effect.

6. Application Example

In this section, SPICE simulation of a CMOS inverter was performed to demonstrate how the proposed method can be applied to a circuit example and to show the practicality of the method. BSIM3 MOSFET model parameters, which are often used in simulations nowadays, were used.

By using the simple CMOS structure of Figure 7, circuit simulations were performed. Supply voltage of the circuit was chosen as $V_{DD} = 5$ V, dimensions for the NMOS were W = 10 μ and L = 3 μ, and dimensions for PMOS transistors are W = 10 μ and L = 1.5 μ.

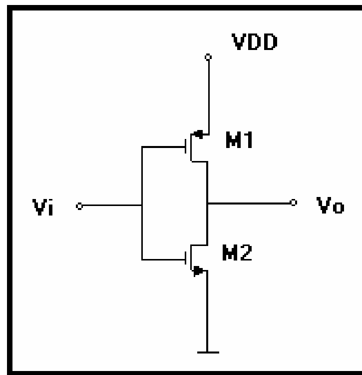

Figure 7. CMOS inverter circuit.

SPICE simulation results for the change in the DC transistor characteristics of the circuit, before stress and after stress, are seen in Figure 8.

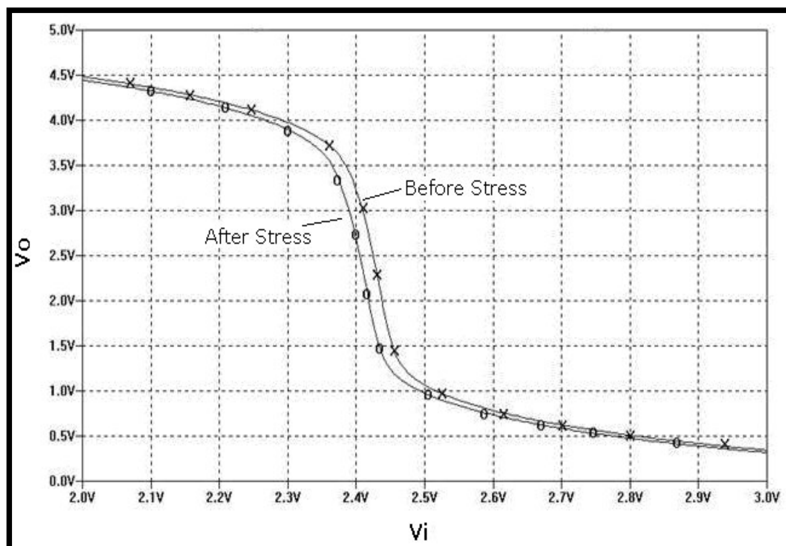

Figure 8. Voltage transfer characteristics before and after stress of the CMOS inverter.

In CMOS inverters, the change of the current and threshold voltage of the transistors have an important effect on the value of the inverting voltage of the circuit. Inverting voltage of the inverter was $V_I = 2.41$ V and $V_O = 2.81$ V before the stress. It was observed that the value of the inverting point of the voltage transition characteristic shifted to $V_I = 2.41$ V and $V_O = 2.51$ V after a stress of 18 h. The transfer characteristic of the inverter, without considering the degradation effect caused by the PMOS transistor, is given in Figure 9, and assumes that the characteristic is influenced only by the NMOS transistor. Before stress and after stress values of the inverter for $V_I = 2.41$ V were Vo = 2.81 V and Vo = 2.75 V, respectively. As seen, the output characteristic of the circuit depends mostly on the change of the drain current of the PMOS. The change in the inverting voltage value with time can be seen in Figure 10.

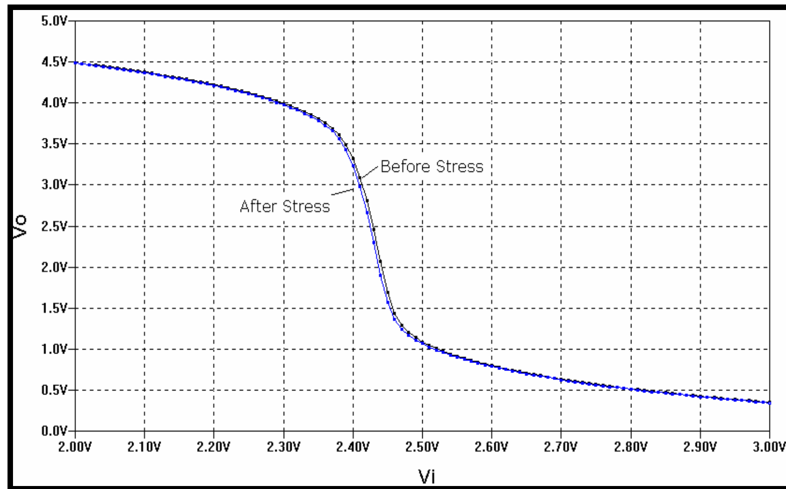

Figure 9. Voltage transition characteristic without the PMOS effect of the CMOS inverter before and after stress.

7. Lifetime Prediction

In order to allow a prediction of device lifetime in real life, stress levels from results obtained under actual stress conditions must be used. With such results, empirical models for hot carrier degradation and several extrapolation laws to calculate the lifetime have been developed. However, the proposed model combines a hot carrier degradation model and lifetime prediction model into a single model [18-22]. Lifetime predictions for MOS transistors have been performed using the criteria given in the literature [18].

They can reach 10% of the lifetime criteria [18] for hot-carriers in DC stress applications in 10 years or less. One year in static conditions is equivalent to 10 years in real operating conditions, in an analog application.

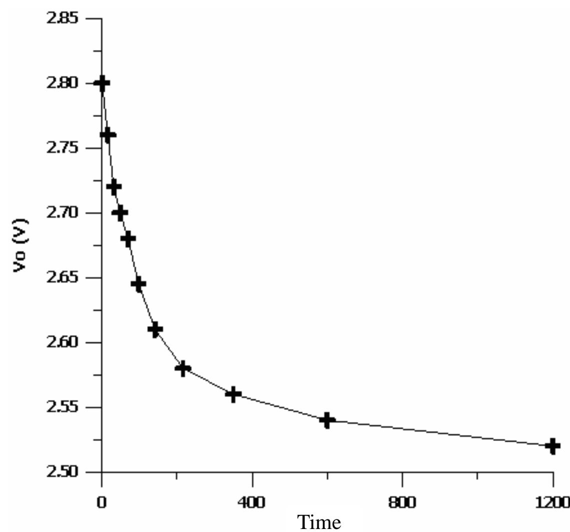

Figure 10. Change in the inverting voltage of the CMOS inverter with time.

Lifetime prediction calculations for MOS transistors were performed with respect to the logarithmic method using the functions of the proposed methods and 10% drain current criteria, which are given in the

literature [18]. Lifetime prediction results obtained by calculations for different operating conditions can be seen in Table 5. Similarly, a function for the change in the output characteristic of the CMOS inverter with lifetime prediction was obtained and it was calculated to be 1.52×10^3 min.

Table 5. Calculated lifetime prediction of P-MOS transistors for different channel lengths.

	P-MOS Predicted lifetime (min)	
Channel length (μm)	Sub-threshold region	Inversion region
L = 1.5	2.16×10^3	4.76×10^6
L = 2	6.83×10^3	2.10×10^7
L = 3	4.00×10^4	6.10×10^8

8. Conclusion

The effect of hot-carriers on the drain current and threshold voltage of PMOS transistors was investigated statistically and an alternative method was proposed to those available in the literature.

Three different statistical methods for PMOSs were investigated for modeling the hot-carrier degradation of transistors. In all the investigated methods, the change in hot-carriers has been expressed by using 2 variable functions, and these coefficients can be determined independently of the technology of the transistor and its operating conditions. Considering the correlation coefficients of the investigated methods, we observe that the logarithmic method is the nearest method to 1 with 0.998, and, considering the RMS errors, we see that the logarithmic method has the least error with 0.03. From these results we can say that the logarithmic method is the best method for the explanation of the change in the data.

To express the variations in drain current and threshold voltage, models have been proposed for PMOS transistors by using the functions belonging to the investigated methods. By using these proposed methods, the effect of hot-carrier degradation on the CMOS inverter circuit was investigated. Hot-carrier degradation's effect on the performance of the circuit was discussed again by using SPICE simulations with the proposed models. At the end of this work, a lifetime prediction calculation was performed using the proposed functions.

The proposed model has some advantages: it can be modeled more practically than the physical model and the simulation time is shorter than the physical model.

The proposed method is based on the measurement results and it is independent of the technology; it can easily be applied to PMOS transistors that have different dimensions. By using this proposed method, percentage changes in drain current, which occur as a result of degradation at any time (t) and threshold voltage, can be found and used for the lifetime prediction of the transistor, and/or any other circuit can be approximately predicted.

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