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New approach FPGA-based implementation of discontinuous SVPWM

Tole SUTIKNO[1,2], **Auzani JIDIN**[1,3], **Nik Rumzi Nik IDRIS**[1]
[1] *Department of Energy Conversion, Faculty of Electrical Engineering*
Universiti Teknologi Malaysia (UTM), Johor-MALAYSIA
[2] *Department of Electrical Engineering, Faculty of Industrial Technology*
Universitas Ahmad Dahlan (UAD), Yogyakarta-INDONESIA
[3] *Department of Power Electronics and Drives, Faculty of Electrical Engineering*
Universiti Teknikal Malaysia Melaka (UTeM), Melaka-MALAYSIA
e-mail: thsutikno@ieee.org, auzani@ieee.org, nikrumzi@ieee.org

Abstract

The discontinuous space vector pulse-width modulation (DSVPWM) is a well-known technique offering lower switching losses than continuous SVPWM. At the same, average switching frequency, or a switching frequency 1.5 times higher than utilized in continuous SVPWM, the discontinuous SVPWM results in lower current harmonic distortions than that obtained in continuous SVPWM at high modulation indices. This paper is concerned with the design and realization of new FPGA approach based a 5-segment discontinuous SVPWM operated at 40 kHz switching frequency. It will be shown that the implementation of the discontinuous SVPWM utilized in FPGA, to execute some complex tasks, is simplified through this new straightforward approach. For example, the judging of sectors, the computation of on-duration or firing pulses to control the switching of power switching devices can be executed much simpler with the proposed arithmetic logics or digital calculation in FPGA. In this way, the sampling frequency and hence switching frequency be increased. The SVPWM scheme has been implemented successfully based on APEX20KE Altera FPGA considering hardware resource saving. The validity of the proposed scheme has been tested experimentally to drive a 1.5 kW induction machine with low current harmonic distortions.

Key Words: *Discontinuous SVPWM, hardware resource saving, FPGA*

1. Introduction

The important requirements of any modulation technique are to obtain higher power output and efficiency for a wide range of inverter output voltage control. The Space Vector Pulse Width Modulation (SVPWM) method has gained popularity to be employed in many industrial and electric drive applications. Compared to Sinusoidal Pulse Width Modulation (SPWM), the SVPWM is more flexible and can be easily implemented using digital signal processor (DSP) or field programmable gate array (FPGA) controller boards. This flexibility is present

because SVPWM requires only a single-voltage reference rather than three voltage reference needed in SPWM, and the output inverter voltage in the SVPWM can be gradually controlled from PWM to a six-step mode. Moreover, SVPWM can achieve better current total harmonic distortion factor [1–4].

In common engineering practice, the SVPWM algorithm is implemented utilizing digital signal processors (DSP), which are superior in their ability to handle calculations involving trigonometric or complex algorithms. The DSP control procedure is performed sequentially, exploiting mathematically oriented resources. This may result in a slower cycling period if complex algorithms are involved. Thus, a purely software-based technique is not an ideal solution. Employing Field Programmable Gate Arrays (FPGA) in implementing SVPWM strategies provides advantages such as rapid prototyping, simpler hardware and software design, high speed computation and hence fast switching frequency. In contrast, FPGA performs entire procedures with concurrent operation (parallel processing via hardware) using reconfigurable hardware. For its powerful computation ability and flexibility, the FPGA may be the best solution to achieve excellent performance in ac drive systems. Currently, the FPGA has gained popularity and is widely used in many electric drive systems and in implementations of the SVPWM algorithm [2, 5–8].

It has been reported that continuous SVPWM suffers drawbacks such as computational burden, inferior performance at high modulation indices and high inverter switching losses. Hence to reduce the switching losses and improve performance in high modulation index regions, several discontinuous SVPWM methods have been proposed [9–12]. In this paper, the implementation of discontinuous SVPWM technique used for three-phase inverter utilizing FPGA is presented. The complex discontinuous SVPWM algorithm is simplified based on the basic ideas reported in [4] and [12]. Our effort is to verify the simplified method and propose some new techniques in defining the sector of space voltage vector and calculation the on-duration of PWM signals. It will be shown that the simple approach to design discontinuous SVPWM results in high speed in computing the overall algorithm and hence produce high switching frequency and low current harmonic distortions in the induction motor drive system. The validity of the proposed control method is verified by the experimental results of an induction motor drive system.

2. The principles of SVPWM

The SVPWM was originally developed as a vector approach to pulse-width modulation (PWM) for three-phase inverter [1]. It is a more sophisticated technique for generating sinusoidal wave that provides a higher voltage to the motor with lower total harmonic distortion. It confines space vector to be applied according to the region where the output voltage vector is located. It is based on the fact that there are only two independent variables in a 3-phase voltage system. We can use orthogonal coordinates to represent the 3-phase voltage in the phasor diagram. A three-phase-voltage vector can be expressed as:

$$V_{\text{ref}} = \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{A_0} \\ v_{B_0} \\ v_{C_0} \end{bmatrix} \tag{1}$$

In the SVPWM scheme, the 3-phase output voltage is represented by a reference vector which rotates at an angular speed of $\omega = 2\pi f$. The task of Space Vector Modulation (SVM) is to use the combinations of switching states to approximate the reference vector, V_{ref}. To approximate the locus of V_{ref}, the eight possible switching

states of the inverter are represented as 2 null vectors and 6 active vectors. These latter vectors ($\mathbf{V}_1 \sim \mathbf{V}_6$) can be used to frame the vector plane, as illustrated in Figure 1. The rotating reference vector can be approximated in each switching cycle by switching between the two adjacent active vectors and the zero vectors. In order to maintain the effective switching frequency at a minimal value, the sequence of the toggling between these vectors is organized in such way that only one leg is affected in every step.

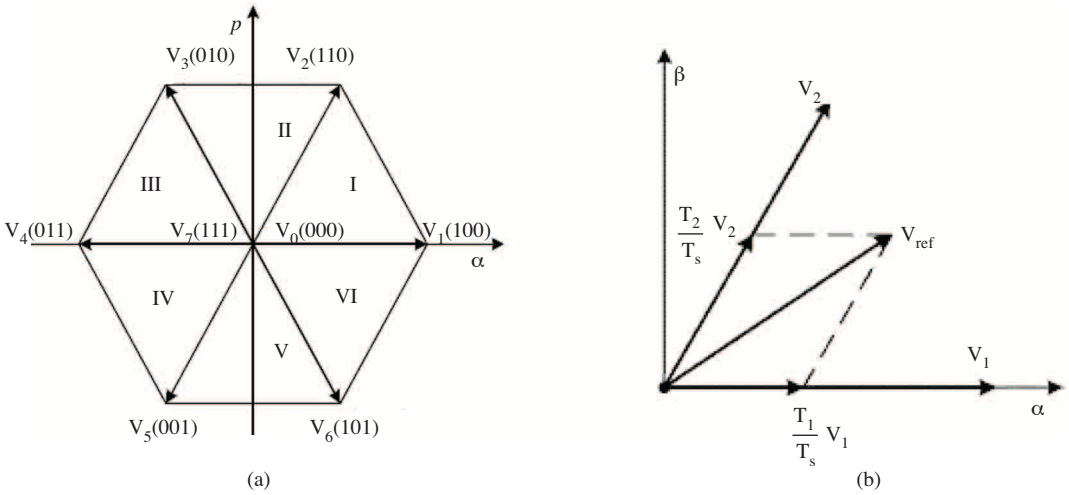


Figure 1. Vector plane frame with (a) space voltage vectors, and (b) the decomposition of $\mathbf{V}_{\text{ref}}$ in terms of $\mathbf{V}_k$ and $\mathbf{V}_{k+1}$ (e.g., in sector I).

Table 1. Criterion for sector identification as used in Reference [6].

Sector	Vector Angle	V_α, V_β conditions
I	(0°, 60°)	$0 \le V_\beta \le \sqrt{3}V_\alpha$
II	(60°, 120°)	$V_\beta \ge \sqrt{3}V_\alpha$ and $V_\alpha \ge 0$, or $V_\beta \ge -\sqrt{3}V_\alpha$ and $V_\alpha < 0$
III	(120°, 180°)	$0 \le V_\beta \le -\sqrt{3}V_\alpha$
IV	(180°, 240°)	$\sqrt{3}V_\alpha < V_\beta \le 0$
V	(240°, 300°)	$V_\beta \ge \sqrt{3}V_\alpha$ and $V_\alpha \ge 0$, or $V_\beta \ge -\sqrt{3}V_\alpha$ and $V_\alpha < 0$
VI	(300°, 360°)	$-\sqrt{3}V_\alpha \le V_\beta < 0$

2.1. Sector identification

The sector determination and application time of an active vector for all SVM strategies are the same. From Figure 1(a), it is obvious that the sector number is determined by the angle of the reference vector. Identification of sector k can be, generally, in $\alpha\beta$ coordinates by using the appropriate boundary condition as per Table 1.

2.2. Determination of the duration of active vectors

For digital control application, the reference inputs are sampled in a regular sampling interval to determine the switching duration of the active vectors. That is, any reference vector inside the hexagon can be obtained two adjacent active vectors (V_k, V_{k+1}). Then, V_{ref} can be expressed as functions of V_k and V_{k+1} by the following

equation:

$$V_{\text{ref}} = \frac{T_k}{T} V_k + \frac{T_{k+1}}{T} V_{k+1}, \tag{2}$$

where T_k and T_{k+1} are the dwell time of V_k and V_{k+1} during each sampling period, respectively, and k is the sector number denoting the reference location. For example in sector I, k=1, vector V_1 activates lasting for T_1, and V_2 activates lasting for T_2 during T. The principle is similar in all sector of the six sectors, therefore Figure 1(b) highlights the relation for sector I only.

Considering that magnitude of non zero space satisfies $||\mathbf{V}_k|| = 2V_{dc}/3$, the dwelling time can be evaluated by the following equations:

$$\begin{cases} T_k = \frac{\sqrt{3}}{V_{dc}} T \left(\sin(\frac{\pi}{3}k) V_\alpha - \cos(\frac{\pi}{3}k) V_\beta \right) \\ T_{k+1} = \frac{\sqrt{3}}{V_{dc}} T \left(-\sin(\frac{\pi}{3}(k-1)) V_\alpha + \cos(\frac{\pi}{3}(k-1)) V_\beta \right) \\ T_0 = T - T_k - T_{k+1} \end{cases} \tag{3}$$

Here, V_{dc} is the dc-link voltage of the inverter, and T_0 is the switching duration of a zero vector in each sampling period. Suppose the reference is keeping a circular trajectory, the $T_0 > 0$, the output voltage is a regular sinusoidal in linear modulation. As in equation (3), it is theoretically simple but it is obvious that this algorithm requires complicated computations involving trigonometric functions.

2.3. Switching sequence (switching pattern)

This SVPWM strategy aims to minimize harmonic distortion in the current by selecting the appropriate switching vectors and determining of their corresponding dwelling widths. The flux produced by the reference voltage vector in a SVPWM switching period is a combination of each individual flux resulted by corresponding voltage vector.

Table 2. Comparison of SVPWM patterns.

No	Pattern SVPWM (based on sector I)	Number of segments	Number of commutation in one sampling period	Total harmonics distortion (THD)	To implement in FPGA (hardware platform)
1	V_0-V_1-V_2-V_7-V_2-V_1-V_0	7	6	low	quiet-difficult
2	V_7-V_2-V_1-V_0-V_1-V_2-V_7	7	6	low	quiet-difficult
3	V_1-V_2-V_7-V_2-V_1	5	4	almost low	easy
4	V_0-V_1-V_2-V_1-V_0	5	4	almost low	easy
5	V_0-V_1-V_2-V_7	4	3	almost significant	not-easy
6	V_0-V_2-V_1-V_7	4	3	almost significant	not-easy
7	V_1-V_2-V_7 and V_2-V_1-V_7 alternately	3	2 and 3 alternately	higher significant	not-easy

There are many switching patterns that can be used to implement SVPWM. The choice of the null vector determines the SVPWM scheme. There are some options: the null vector $\boldsymbol{V}_0$ only, the null vector $\boldsymbol{V}_7$ only, or a combination of null vectors. The equivalent PWM waveforms, which produce the same average flux, may consist of various combinations of the basic vectors. Referring to [5, 11–13], there are at least seven switching patterns. The characteristic of each those schemes above can be resumed as shown in Table 2. It is shown

that SVPWM third and fourth patterns are easier to implement FPGA compared to others patterns. Moreover, those patterns have lower switching loss compared to 7-segment continuous SVPWM with almost low harmonics distortion.

3. A new approach to implementing 5-segment discontinuous SVPWM algorithm

Different from how SVPWM has been implemented by other previous researchers, this section presents a symmetrical 5-segment discontinuous switching sequence with a new method of sector determination and a new method of SVPWM generation based on calculation of active vector duration to avoid complicated computations with trigonometric functions, as mentioned in equation (3).

3.1. Proposed SVPWM switching Pattern (5-segment discontinuous switching pulses)

There has been reported many discontinuous SVPWM patterns [5, 9–11, 13]. However, not all those patterns have lower switching losses. A simpler algorithm, with low switching losses, can be easily implemented via FPGA. In this paper, a novel symmetric 5-segment discontinuous SVPWM design is considered, with reference to the basic idea from [4] and [12], in which is proposed there is always one channel that stays constant for the entire PWM period. The state sequence in this pattern is X-Y-Z-Y-X, where Z=1 in sector I, III and V, and Z=0 in the remaining sector. So the amount of switching time for this pattern is less than the continuous pattern. The obvious result of this is reduced switching losses.

A similar pattern has been successfully implemented via DSP by Yu [12]. That method has lower switching losses, a simpler algorithm and ease of implementation. Unfortunately, the implementation of a SVPWM algorithm based on DSP is limited to sampling rate and switching frequency, a limitation that can be expected because the DSP is a software-platform based device.

Therefore, this paper proposes using a FPGA, which is a hardware-platform based device, to improve sampling rate and switching frequency in the implementation of SVPWM.

3.2. Proposed identification of the sector

Several methods have been introduced to decide the sector in which the reference space voltage vector lies. Zhi-pu [14] compared the reference space vector's angle with 0°, 60°, 120°, 180°, 240°, and 300° to obtain the sector number in which $\mathbf{V}_{ref}$ lies. Others, Yu [15], Jiang [7] and Xing [16], have analyzed the relationship between V_α and V_β to determine the sector. They have calculated the projections V_a, V_b and V_c of V_α and V_β in (a,b,c) plane by using the inverse Clark transformation:

$$\begin{cases} V_a = V_\beta \\ V_b = \frac{\sqrt{3}V_\alpha - V_\beta}{2} \\ V_c = \frac{-\sqrt{3}V_\alpha - V_\beta}{2}. \end{cases} \tag{4}$$

Then, based on equation (4), they calculate $N = \text{sign}(V_a) + 2\ \text{sign}(V_b) + 4\ \text{sign}(V_c)$. Map N to the actual sector of the output voltage reference by referring to the following relationship:

N	1	2	3	4	5	6
sector	2	6	1	4	3	5

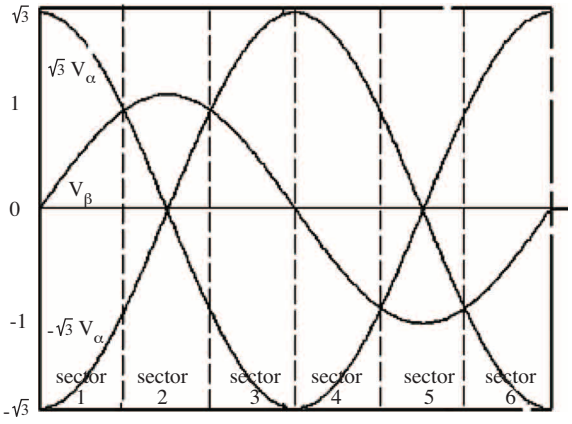


Figure 2. Plot of V_β, $\sqrt{3}V_\alpha$, $-\sqrt{3}V_\alpha$ waveforms as a function of time.

Table 3. The proposed, simpler identification of the sectors. 1 denotes *satisfy*, 0 denotes *not* satisfy.

Sector	Vector Angle	$V_\beta > 0$	$V_\beta > \sqrt{3}V_\alpha$	$V_\beta > -\sqrt{3}V_\alpha$
I	(0°, 60°)	1	0	1
II	(60°, 120°)	1	1	1
III	(120°, 180°)	1	1	0
IV	(180°, 240°)	0	1	0
V	(240°, 300°)	0	0	0
VI	(300°, 360°)	0	0	1

In [17], Zeliang adopted intermediate vectors $X_\alpha = \frac{3}{2}V_\alpha$ and $X_\beta = \sqrt{3}V_\beta$, as decomposition of continuous SVPWM, which will properly counteract the redundant calculations to identify sector location; but it imported complicated matrix calculations. Hence, through analyzing SVPWM, as mentioned above, the present work has created a simpler method to determine the sectors of voltage vectors based on comparison between V_β, $\sqrt{3}V_\alpha$, $-\sqrt{3}V_\alpha$ and 0, as shown in Figure 2. With the comparison, we can more simply determine the voltage-vector sectors compared to [7, 14–17]. Table 2 clarifies sector identification via truth table.

3.3. The proposed calculation of the duration of active vectors

In this work, based on the analysis performed in [12], a new set of equations to calculate the duration of active vectors for each sector has been rearranged in order to construct an easier implementation based on FPGA. The equations associated with each sector are shown in Table 3.

3.4. Proposed method to generate SVPWM switching pulses

The discontinuous, 5-segment discontinuous SVPWM employs symmetrical switching pulses as does the 7-segment continuous SVPWM. Therefore, a similar method to generate continuous SVPWM switching pulses

can be adopted in the proposed SVPWM. To simplify the implementation based on FPGA, a graphical method has been devised to generate the SVPWM switching pulses as illustrated in Figure 3.

Table 4. The switching time of the active vector for each sector.

Sector	T_a	T_b	$T_a + T_b$
I	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
II	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
III	$\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
IV	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} + \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$
V	$\frac{3T}{4}\left(-\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$
VI	$-\frac{3T}{4}\frac{2V_\beta}{\sqrt{3}V_{dc}}$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$	$\frac{3T}{4}\left(\frac{V_\alpha}{V_{dc}} - \frac{V_\beta}{\sqrt{3}V_{dc}}\right)$

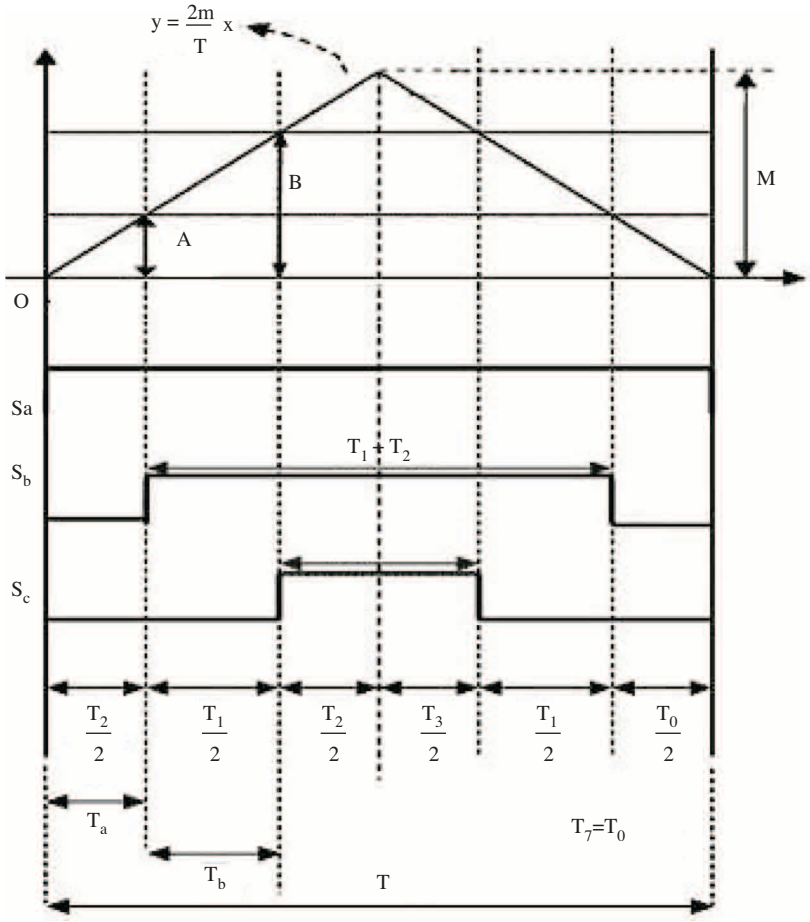


Figure 3. Proposed method to generate SVPWM switching pulses.

Considering the relation $y = \frac{2m}{T}x$ in Figure 3, the PWM generation for odd sector positions were implemented via comparison between *triangle* and T_a, and between *triangle* and $T_a + T_b$; other switching

pulses was set equal to 1. For even sector positions, PWM generation was implemented via complement of comparison between *triangle* and T_a, and complement of comparison between *triangle* and $T_a + T_b$; other switching pulses were set equal to 0.

For example, in sector I, if $x = T_a = \frac{T_0}{2}$, then $y = \frac{2m}{T}\left(\frac{T_0}{2}\right)$; and if $x = T_b = \frac{T_1}{2}$, then $y = \frac{2m}{T}\left(\frac{T_1}{2}\right)$. For simpler circuit design, in this paper the term $\frac{2m}{T}$ is set equal to 1; so if $x = \frac{T_0}{2} = T_a$, then $y = \frac{T_0}{2} = T_a$; and if $x = \frac{T_1}{2}$, then $y = \frac{T_1}{2} = T_b$. Obviously, if $x = \frac{T_0}{2} + \frac{T_1}{2} = T_a + T_b$ then $y = \frac{T_0}{2} + \frac{T_1}{2} = T_a + T_b$. Therefore, the generation of PWM for channels S_b and S_c in sector I can be obtained comparing the triangle with T_a, and comparing triangle and $T_a + T_b$, respectively, with channel S_a is set equal to 1. The generation of PWM in other sectors can be obtained in a similar way.

4. FPGA implementation of a proposed novel SVPWM

In the previous section, the principle of SVPWM was analyzed. In this section, implementation of the proposed SVPWM based on FPGA is presented. An overall schematic of the proposed SVPWM design is shown in Figure 4. The overall block is divided into 5 sub-modules: *ajust_freq*, *Vbeta_Valfa*, *find_sector*, *SVM_generator* and the *deadtime_system* module.

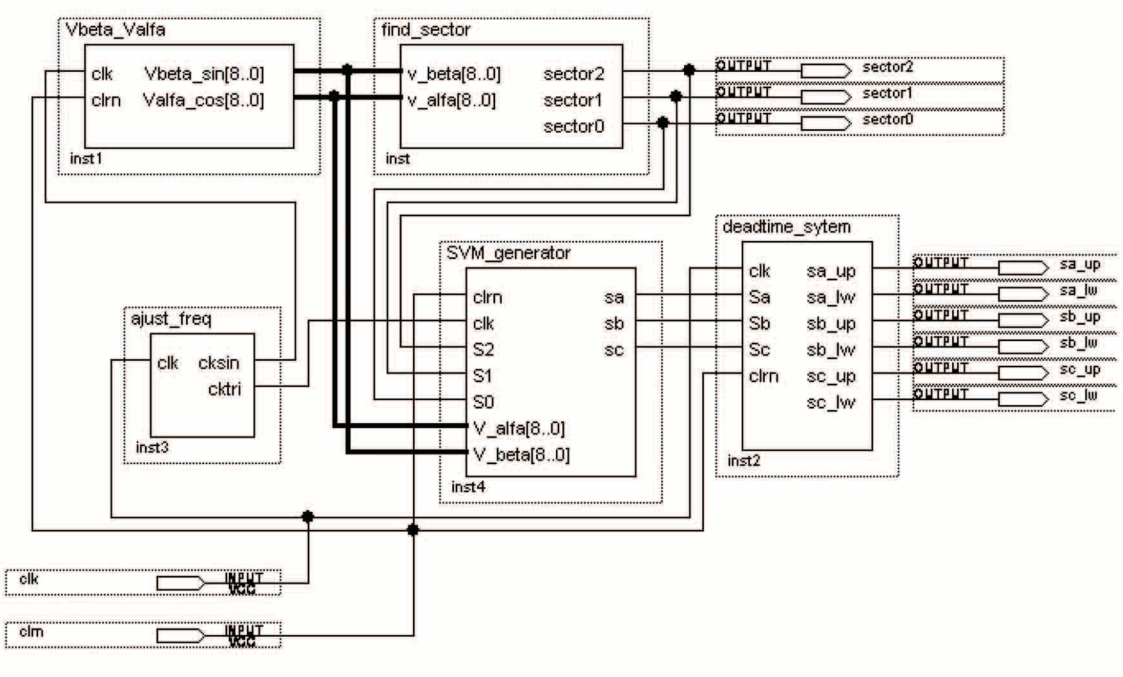


Figure 4. An overall schematic of the proposed SVPWM design.

4.1. Adjustable frequency module

In this module, the clock source is designed to connect to the L6 pin on the Altera APEX 20KE FPGA board. It is a 33.33 MHz dedicated clock generator. This module provides clocking source for carrier and the reference signal generator. In this work, the carrier signal frequency is set to 40 kHz and reference signal frequency is set

to 50 Hz. To get the desired carrier and reference signal frequency, the clock frequency is divided. For example, to generate a 40 kHz carrier signal sampled 32 times, the source clock generator (L6) is divided by 26 (33.33 MHz : 26 : 32 = 40 kHz). The reference signal clocking is produced in a similar way.

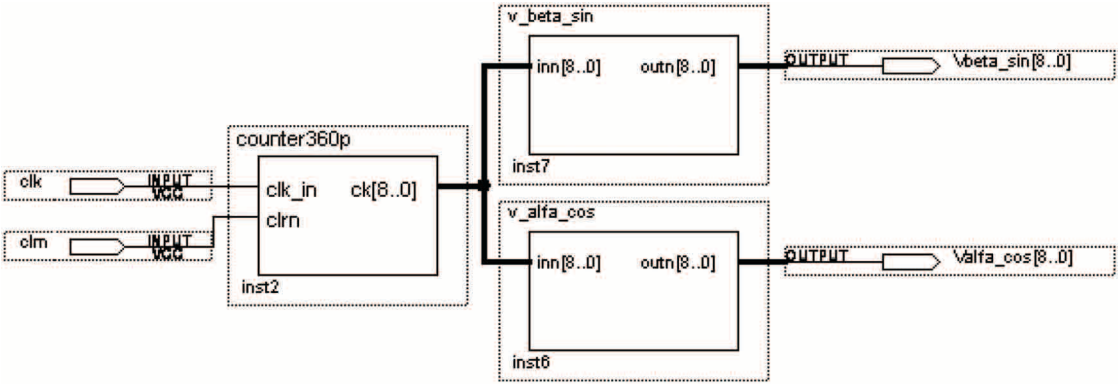


Figure 5. Modules V_α and V_β.

4.2. V_α and V_β module

In this work, V_α and V_β are generated through a sine and cosine look-up table (LUT) function with memory mapping 360 entries. The lower, base, and higher numbers of sine and cosine function are 96, 224 and 352 respectively (in 9 unsigned bits). The design of modules V_α and V_β are shown in Figure 5. Because in this design uses 360 memory mapping addresses, then a counter mod-360 is used to count LUTs mentioned above. As a note, in advanced close-loop control V_α and V_β are obtained the ABC to $\alpha\beta$ transformation of voltage sensing.

4.3. Sector identification module

The Sector Identification module is used to determine sector based on Table 2. The design of sector identification is shown in Figure 6.

The sub-modules denoted "*x_pos_akar*" and "*x_neg_akar*" were used to multiple between V_α by $\sqrt{3}$ and V_α by $-\sqrt{3}$, respectively; then, those results were compared with V_β through sub-module "*comp9a*," written in VHDL code, and V_β was compared to zero through sub-module "*compa*," as shown in Figure 6. The simplification of truth table for comparison results, as shown in Table 5, were used to determine sector number in sub-module "*csector*."

Table 5. Conversion of comparison result between $V_\beta, \sqrt{3}V_\alpha, -\sqrt{3}V_\alpha$ and 0 to sector number.

Sector	Vector Angle	Input	Ouput ($S_2S_1S_0$)
I	(0°, 60°)	101	001
II	(60°, 120°)	111	010
III	(120°, 180°)	110	011
IV	(180°, 240°)	010	100
V	(240°, 300°)	000	101
VI	(300°, 360°)	001	110

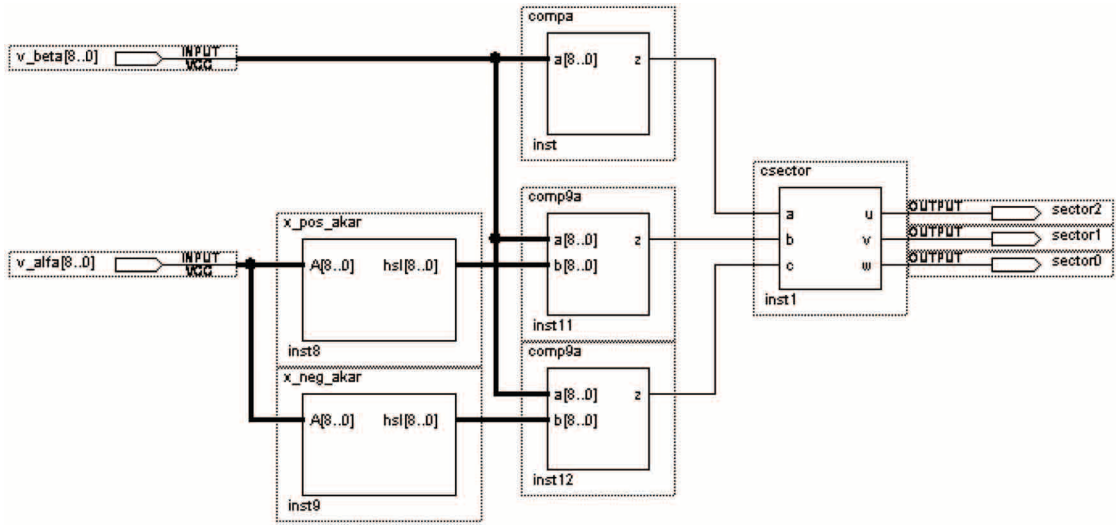


Figure 6. Sector identification module.

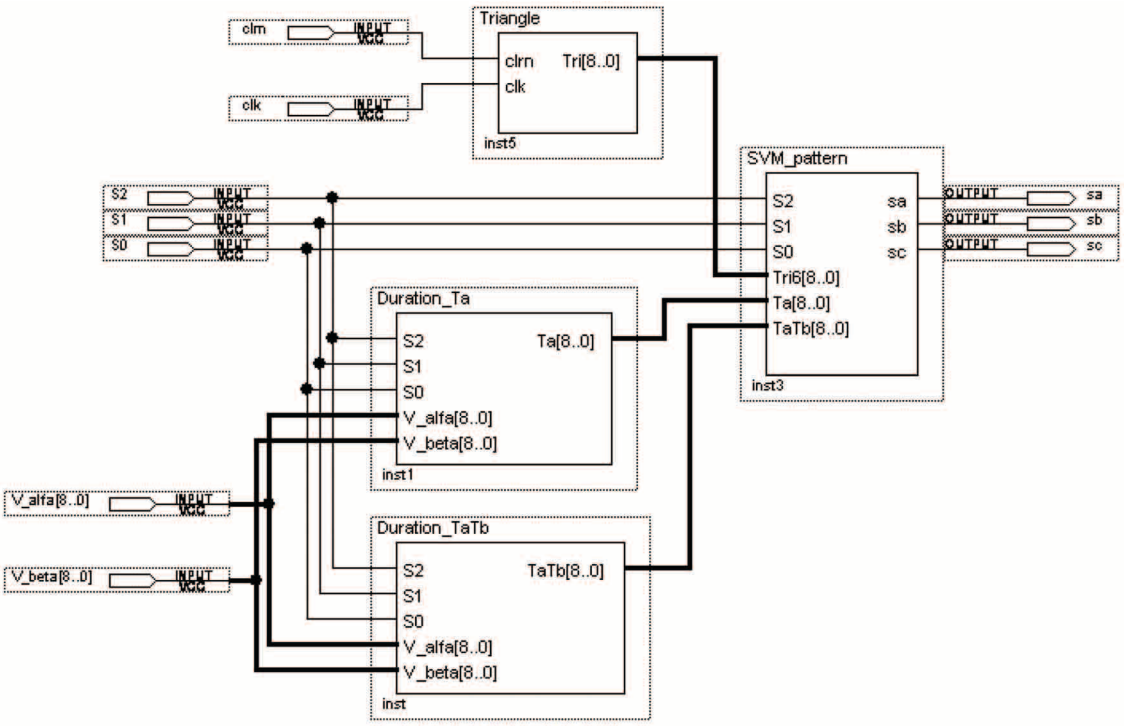


Figure 7. Three phase SVPWM signal generator module.

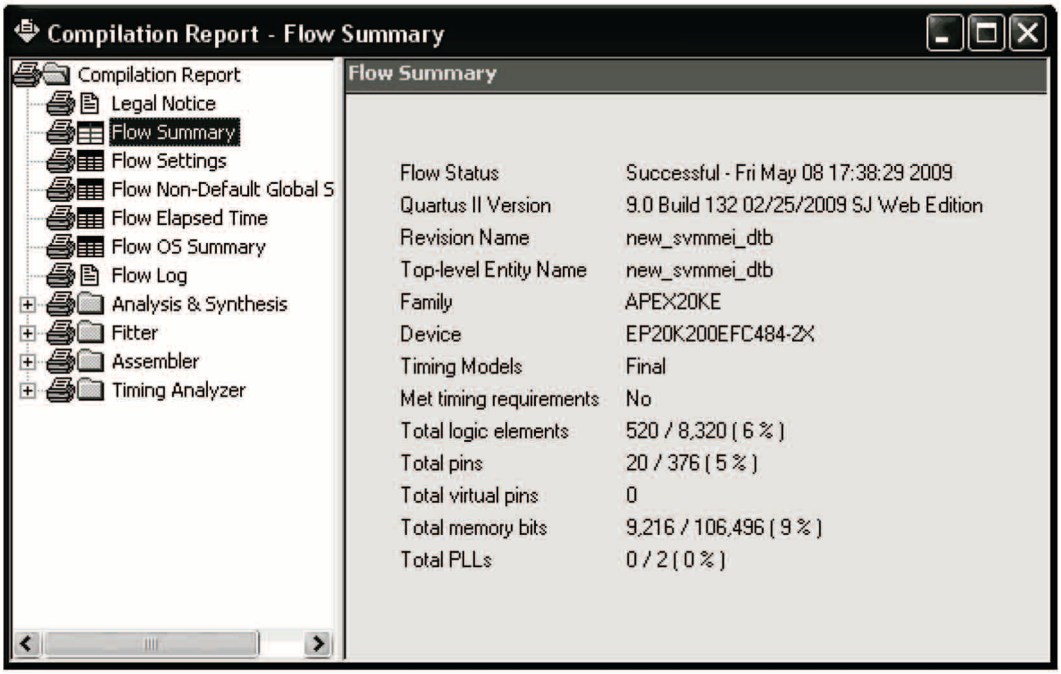
4.4. Three-phase SVPWM signal generator module

The overall schematic for the three-phase SVPWM signal generator module is shown in Figure 7. This module can be divided into 4 sub-modules, named *Triangle*, *Duration_Ta*, *Duration_TaTb*, and *Space Vector Modulation (SVM) pattern* sub-module. Sub-module *Triangle* was used to a generate triangle carrier signal. In this work, triangle signal generator was sampled at 32 Hz and 9 unsigned bits were used to encode data, with values

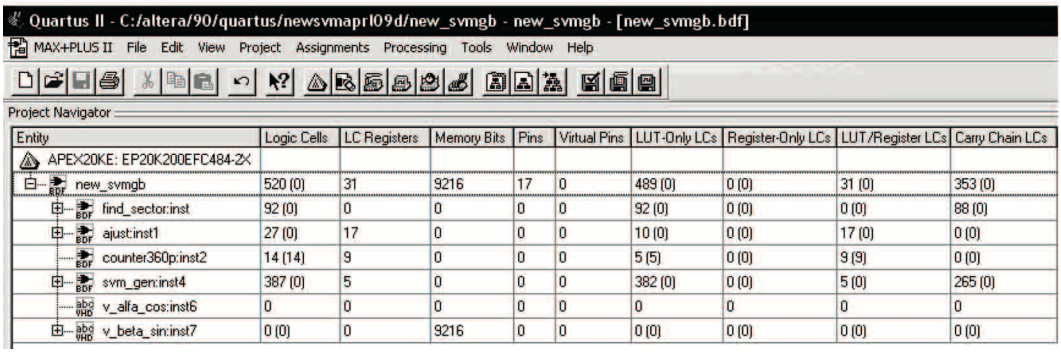
between 224 and 352. Sub-modules *Duration_Ta* and *Duration_TaTb* were created based on digital solution of the second and fourth columns in Table 3, respectively. Sub-module *SVM pattern* was used to generate the set of SVPWM pulses; refer to Section 3.4 and Figure 3.

5. Simulation and experiment results

The software to design, perform compilation, verification and develop hardware based on the APEX 20KE FPGA was developed under the Alterus Quartus II, Version 9.0, Web Edition.



(a) Compilation report



Entity	Logic Cells	LC Registers	Memory Bits	Pins	Virtual Pins	LUT-Only LCs	Register-Only LCs	LUT/Register LCs	Carry Chain LCs
APEX20KE: EP20K200EFC484-2X									
new_svmgb	520 (0)	31	9216	17	0	489 (0)	0 (0)	31 (0)	353 (0)
find_sector:inst	92 (0)	0	0	0	0	92 (0)	0 (0)	0 (0)	88 (0)
ajust:inst1	27 (0)	17	0	0	0	10 (0)	0 (0)	17 (0)	0 (0)
counter360p:inst2	14 (14)	9	0	0	0	5 (5)	0 (0)	9 (9)	0 (0)
svm_gen:inst4	387 (0)	5	0	0	0	382 (0)	0 (0)	5 (0)	265 (0)
v_alfa_cos:inst6	0	0	0	0	0	0	0	0	0
v_beta_sin:inst7	0 (0)	0	9216	0	0	0 (0)	0 (0)	0 (0)	0 (0)

(b) The using of FPGA resource in detail

Figure 8. Screen images from Quartus II showing (a) a compilation report; (b) details characterizing use of the FPGA in detail.

5.1. Simulation

In this work, we set $V_{dc}/T = 1$, switching frequency to 40 kHz, and reference frequency to 50 Hz. The Quartus II compilation report for the proposed SVPWM generator is shown in Figure 8(a), and further detail for each module shown in Figure 8(b). It can be seen that the design requires 520 logic elements and 9,216 memory bits. When compared with other previous methods, the proposed method required the minimum hardware resources, as shown in Figure 9.

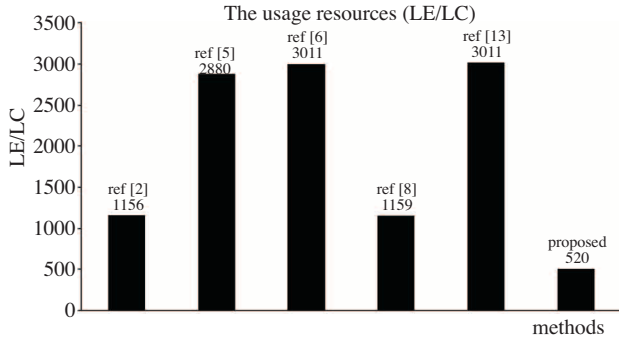


Figure 9. The comparison of required hardware resources.

The simulation result in sector I and II of the proposed SVPWM is shown in Figure 10. This simulation result has proved that the proposed design runs as desired as in [10, 12].

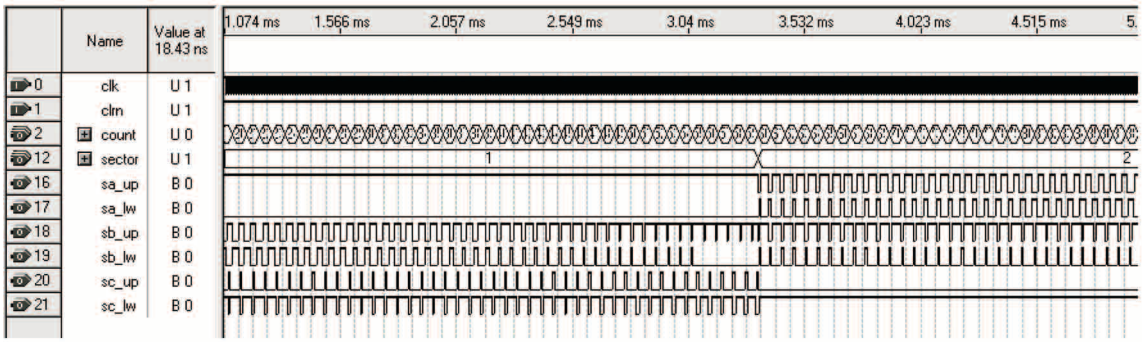
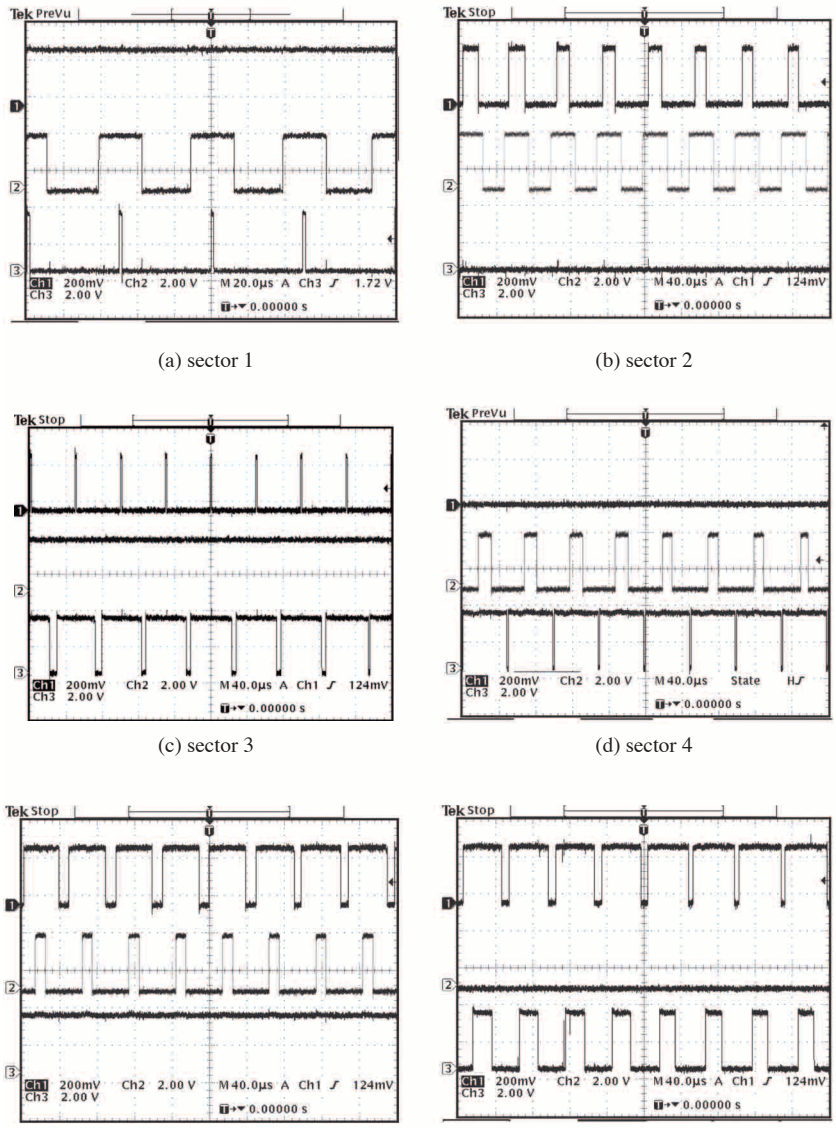


Figure 10. Simulation results of the proposed SVPWM generator.

5.2. Experiment

The previous section has shown that the proposed SVPWM generator runs properly at simulation level. Next is to validate the design at hardware level. In this work, the proposed SVPWM generator design, with carrier frequency 40 kHz, was successfully programmed into the Altera APEX 20KE FPGA. The shape of switching state pulses in each sector and the 2 μs dead-time are shown in Figures 11 and 12 respectively. These results show that the design runs as desired and as in [10, 12].

If compared to [12], the proposed SVPWM has higher switching frequency, 40 kHz, compared to 20 kHz. Moreover, time from design to prototype verification is faster.



(a) sector 1 (b) sector 2

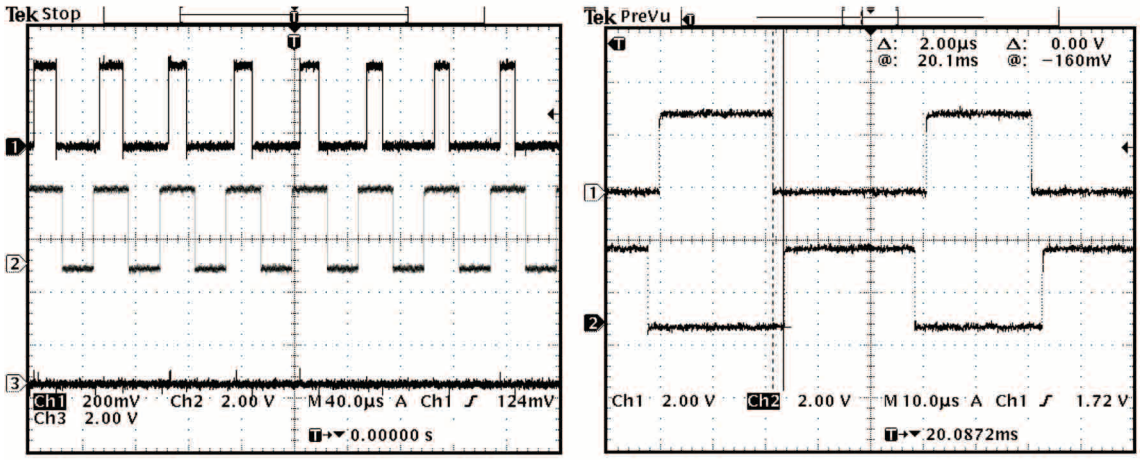
(c) sector 3 (d) sector 4

(e) sector 5 (f) sector 6

Figure 11. Shape of switching state pulses in each sector.

To investigate harmonic distortion, we measured frequency spectrum. Figure 13 (a) and (b) show line-to-line voltage and spectrum frequency of proposed SVPWM generator, respectively, at carrier frequency 40 kHz. The first, second and third channels shown Figure 13 (a) and (b) are measures of S_a, S_b, and S_c switching states, respectively. The fourth channel shows $(\mathrm{S}_a + \mathrm{S}_b)$ line-to-line switching state and its frequency spectrum.

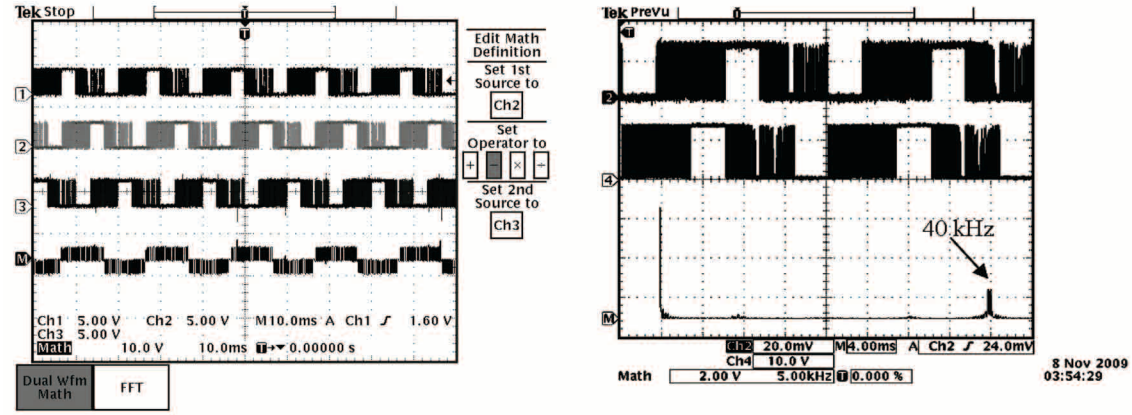
Figure 13(b) shows that the harmonic distortion below 40 kHz is significant, and proves that the proposed SVPWM generator has been successfully implemented based on FPGA, with 40 kHz switching frequency and low THD.



(a) The shape of swiching state pulses in sector 2

(b) The zoomed dead time of S_a swiching state in sector 2

Figure 12. The shape of dead-time pulses for the proposed SVPWM generator in sector 2. Image (b) is zoom of the image in (a).



(a) The swithcing state and its line-to-line

(b) The signal gating and its frequency spectrum

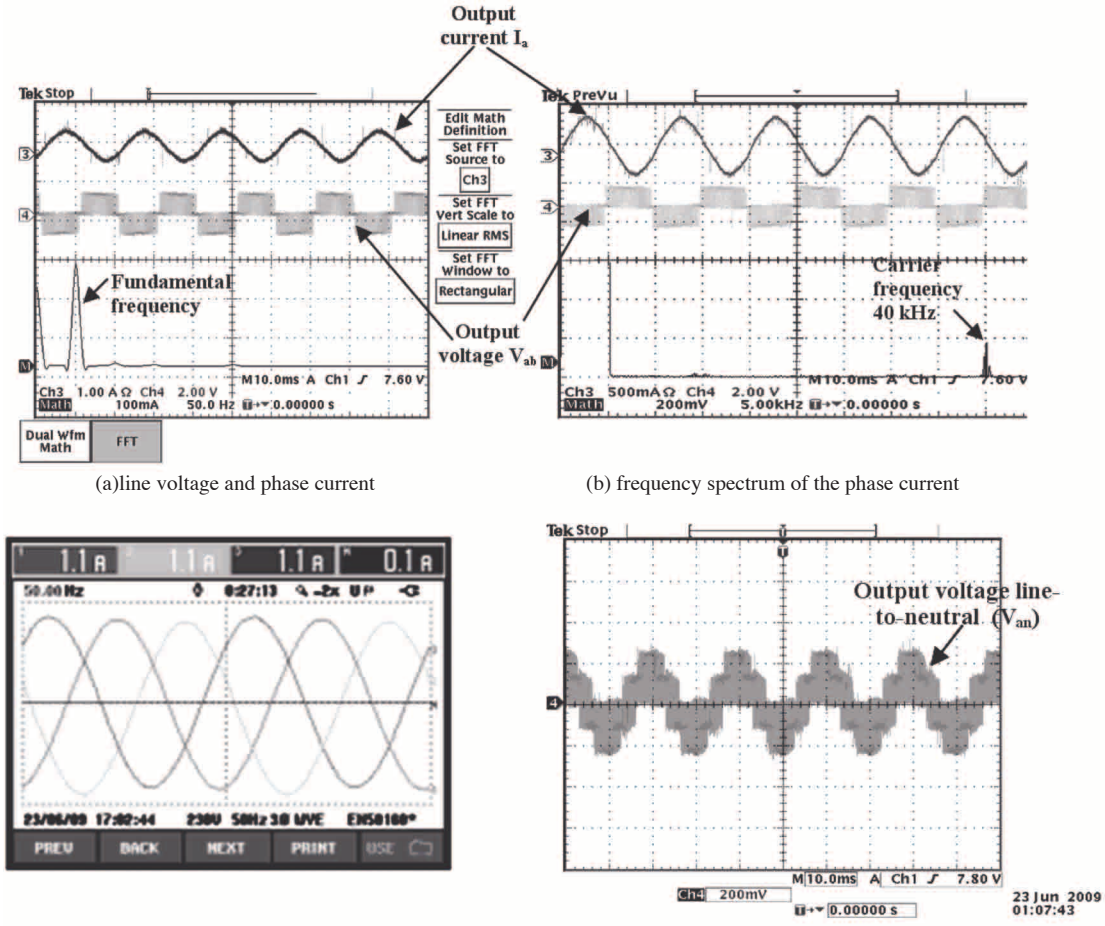
Figure 13. The hardware implementation of the proposed SVPWM generator. at carrier frequency 40 kHz.

We have also tested the proposed FPGA based SVPWM generator design using a three-phase voltage source inverter connected to a 1.5 kW load. The results are shown in Figure 14(a)Ğ(d). The figure shows the phase and line voltages, the phase current and the frequency spectrum of the phase current. The practical results from the test-rig were in as expected and showed that the proposed SVPWM generator design has successfully driven a 1.5 kW induction machine, with low current ripple.

6. Conclusion

This paper has presented the realization of a novel 5-segment discontinuous FPGA-based SVPWM at 40 kHz switching frequency, built on the simple judging of sectors, a re-arranged method for calculation of the firing time, and a simple method to generate SVPWM pulses (without complicated computations involving trigonometric

functions). The SVPWM scheme has been implemented successfully based on the Altera APEX 20KE FPGA. It also has been tested successfully to drive a 1.5 kW induction machine, exhibiting low current ripple.



(a)line voltage and phase current

(b) frequency spectrum of the phase current

(c) 3-phase currents

(d) line to neutral voltage

Figure 14. The performance of proposed SVPWM generator design based on FPGA.

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