An approach based on particle swarm computation to study the nanoscale DG MOSFET-based circuits

Faycal DJEFFAL[1], **Toufik BENDIB**[1], **Redha BENZID**[2],
Abdelhamid BENHAYA[1]
[1]*LEA, Department of Electronics, University of Batna, 05000, ALGERIA*
e-mail: faycaldzdz@hotmail.com
[2]*Department of Electronics, University of M'sila-ALGERIA*

Abstract

The analytical modeling of nanoscale Double-Gate MOSFETs (DG) requires generally several necessary simplifying assumptions to lead to compact expressions of current-voltage characteristics for nanoscale CMOS circuits design. Further, progress in the development, design and optimization of nanoscale devices necessarily require new theory and modeling tools in order to improve the accuracy and the computational time of circuits' simulators. In this paper, we propose a new particle swarm strategy to study the nanoscale CMOS circuits. The latter is based on the 2-D numerical Non-Equilibrium Green's Function (NEGF) simulation and a new extended long channel DG MOSFET compact model. Good agreement between our results and numerical simulations has been found. The developed model can also be incorporated into the nano-CMOS circuits' simulators to study CMOS-based devices without impact on the computational time and data storage.
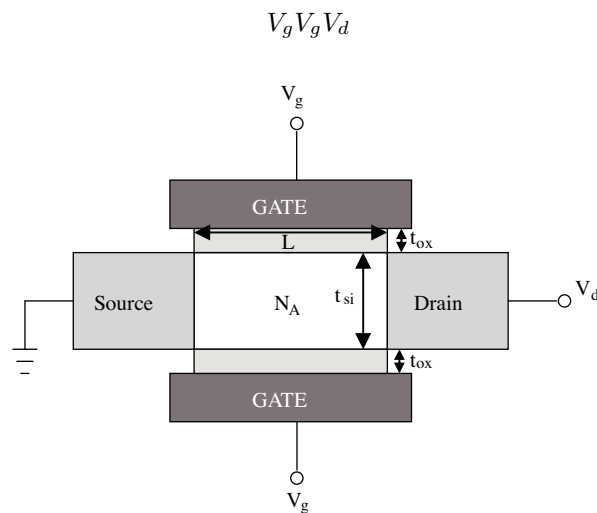
Key Words: *Particle Swarm, DG MOSFET, Optimization, nanoscale, compact model*

1. Introduction

The importance of multi-gate MOS transistors, particularly Double Gate MOSFETs (DG), is rising in nanoscale CMOS circuits design. This is mainly due to the superior control of short channel effects (SCEs) because of the reduced influence of the drain voltage on the channel charge. The advantages advocated for DG MOSFET, shown in Figure 1 include: ideal subthreshold slope; light doping of the channel reducing the mobility degradation due to the elimination of impurity scattering; good control of short channel effects; ideal subthreshold swing due to the elimination of substrate doping; etc [1–4]. Previous works which studied the DG MOSFETs include the fabrication procedures, numerical and analytical modeling [1–6]. To extract information accurately about the current-voltage (I-V) characteristics require the solution of Schrödinger and Poisson equations based on the non-equilibrium Green's function (NEGF) formalism, assuming quantum effects are to be fully accounted [7]. But from the nanoscale CMOS circuits design point of view even 2-D solution of numerical NEGF is an

overkill approach in term of both complexity and computational cost [7]. For analytical devices modeling, in general, it is difficult or almost impossible to obtain closed analytical models form for nanoscale DG MOSFETs, where this approach requires several approximations during the model development [3, 6, 8]. Thus, models are obtained by a simplification of the full physical model (quantum effects, short-channel-effects, etc.). One preferable approach is the evolutionary-based model, which could provide practical solutions for a nanoscale CMOS circuits design. We can call this the "intelligent simulator" approach.

In this work, we present the applicability of particle swarm optimization (PSO) approach to develop a compact drain current model for the nanoscale DG MOSFETs design. The database used for the optimization of our compact model is built on the basis of a numerical model of a I-V characteristics of the nanoscale DG MOSFET developed using the 2-D numerical non-equilibrium Green's function (NEGF) [4, 7]. The proposed approach can be used as an interface between device modeling step and circuits simulators like SPICE, Cadence, etc., in order to obtain a simple and accurate PSO-based nanoscale CMOS circuits' simulators.

Figure 1. Schematic sketch of symmetrical DG MOSFET structure investigated in this study with channel doping $N_A = 10^{16}$ cm^{-3}, silicon thickness $t_{si} = 3$ nm and oxide thickness $t_{ox} = 1.5$ nm.

2. Particle swarm computation

The particle swarm optimization is an evolutionary computation technique inspired by social behavior of a flock of birds and insect swarms. Originally proposed by Kennedy and Eberhart [9, 10], it has recently been introduced to study the complex and nonlinear systems and has found useful applications in engineering fields [9, 10, 11]. The basic principle of PSO algorithm is formed on the assumption that potential solutions will be flown through hyperspace with acceleration towards more optimum solutions. Each particle adjusts its flying according to the flying experiences of both itself and its companions. In the original concept of the PSO, particles fly through the search space influenced by two factors: one is the individual's best position ever found (p_{best}); the other is the group's best position (g_{best}). The most significant of PSO algorithm is its relatively simple coding and hence low computational cost. Due to its simple mechanism and high performance for global optimization, PSO can be applied to study the nanoscale DG MOSFETs.

The objective in the design of optimal I-V characteristics is to find the configuration of model parameters for the analytical compact device model that satisfies the features of the numerical or measured I-V characteristics. The relationship between modeling input parameters and computed results can be given by $I_{ds} = h(V_{gs}, V_{vs}, \vec{C})$, where V_{gs}, V_{ds} are input bias voltage represent the gate-source voltage and the drain-source voltage, respectively, and vector $\vec{C}$ is the vector of construction parameters for compact model, which will be optimized to fit the numerical results (derived via NEGF) using the PSO-based approach.

We used the NEGF formalism to form a database to optimize our PSO-based compact analytical model for nanoscale DG MOSFETs, and this offers several advantages over conventional computing methods (e.g., numerical and long channel analytical models).

The first step of our approach consists of a compact model for long channel DG MOSFETs proposed in [12]:

$$I_{ds} = \left(\frac{\mu_{eff}}{L}\right)\left[\frac{q_s^2 - q_d^2}{2n_1} + (q_s - q_d)\right], \tag{1a}$$

where q_s and q_d are the normalized charge at the source and the drain respectively; $n_1 = 1 + \text{sub}_1 \cdot \left(\frac{C_{si}}{C_{si}+C_{ox}}\right)$ represents the ideality factor; C_{si} and C_{ox} represent the silicon and oxide capacitance, respectively; and μ_{eff} represents the effective mobility given in [13] as

$$\mu_{eff} = \left(\frac{\mu_T}{[1 + \mu_T E/v_{sat}]^{mob_6}}\right)^{\frac{1}{mob_6}} \tag{1b}$$

with

$$\mu_T = mob_1 + \left(\frac{mob_1 \cdot (T/300)^{mob_3} - mob_2}{1 + (N_A/mob_5)^{mob_4}}\right) \text{ and } v_{sat} = mob_7\sqrt{\tanh\left(\frac{mob_8}{T}\right)}.$$

The analytical expression of the normalized charge within the channel is given in [12] as

$$q_I = sub_2 \cdot n_1 \cdot \ln\left(1 + \exp\left(sub_3 \cdot V_{gs} - \left(\frac{V_{to}}{n_1}\right) - V_{ch}\right)\right). \tag{1c}$$

The parameter Vt_0 represents the threshold voltage given in [10] and is

$$V_{to} = th_1 V_{fb} + th_2\left(\frac{C_{eq}}{C_{ox}}\right)V_{fb} + th_3\left(\frac{C_{eq}}{C_{ox}}\right)2\phi_B + th_4\left(1 + \left(\frac{C_{eq}}{C_{si}}\right)\right)\left(\frac{qN_At_{si}}{C_{ox}}\right), \tag{1d}$$

where $C_{eq} = \frac{C_{si}.C_{ox}}{C_{si}+C_{ox}}$, and ϕ_B, V_{fb} are the barrier and the flat band voltage respectively. By replacing V_{ch} by the S/D voltage, q_s and q_d can be evaluated. Using expressions (1a) to (1d) and an adjustment carried out on $(1+V_{ds})$ term , a new extended drain current compact model for DG MOSFET can be defined as

$$I_{ds} = \left(\frac{\mu_{eff}}{L}\right)\left[\frac{q_s^2 - q_d^2}{2n_1} + (q_s - q_d)\right](1 + mob_9 \cdot V_{ds}). \tag{2}$$

The coefficients sub_i $(i = 1:3)$, th_i $(i = 1:4)$ and mob_i $(i = 1:9)$ represent the adjustment parameters; these will be optimized in order to develop our short channel compact model to study the scaling capability of the DG

MOSFETs. Model parameters are divided into three groups: threshold group (th_i $(i = 1 : 4)$), subthreshold group (sub_i $(i = 1 : 3)$) and the mobility group (mob_i $(i = 1 : 9)$). Unfortunately, these three groups of parameters can't be extracted independently to determine the I-V characteristics. Instead, the parameters extraction has to be performed, in principle, with all parameters simultaneously for all bias conditions.

In our study, the jth particle is characterized by three attributes: (1) the particle position vector $x_j = (sub_{PSO\_i}\,(i = 1 : 3), th_{PSO\_i}\,(i = 1 : 4), mob_{PSO\_i}\,(i = 1 : 9))$, which contains the design variables of the optimization problem; (??) the particle position change (velocity) vector v_j; and (3) the personal (local) best position achieved by the particle so far p_{best_j}. The modified velocity and position of each particle can be calculated using the current velocity and the distance from the $p_{\text{best}_{j,g}}$ to g_{best_g} as shown in the following formulas [9, 10]:

$$v_{j,g}^{(t+1)} = w \cdot v_{j,g}^{(t)} + c_1 \cdot r_1 \cdot (p_{\text{best}_{j,g}} - x_{j,g}^{(t)}) + c_2 \cdot r_2 \cdot (g_{\text{best}_{j,g}} - x_{j,g}^{(t)}) \tag{3a}$$

$$x_{j,g}^{(t+1)} = x_{j,g}^{(t)} + v_{j,g}^{(t+1)}, \text{with} j = 1, 2, \ldots, n \text{and} g = 1, 2, \ldots, m \tag{3b}$$

where n represents the number of particles in the swarm; t is the number of generations; w is the inertia weight factor; c_1 and c_2 represent the cognitive and social acceleration factors, respectively; m is the number of compounds for the vectors v_j and x_j (in our case, m=16); r_1, r_2 are random numbers uniformly distributed over the range (0, 1); $x_{j,g}^{(t)}$ represents the g_{th} component of the position of particle j at generation t; p_{best_j} represents the local best of particle j; g_{best_j} is the global best of the group; and $v_{j,g}^{(t)}$ represents the g_{th} component of the velocity of particle j at generation t. In the present study, a mean squared error of the drain current for the j_{th} particle is taken as the fitness function
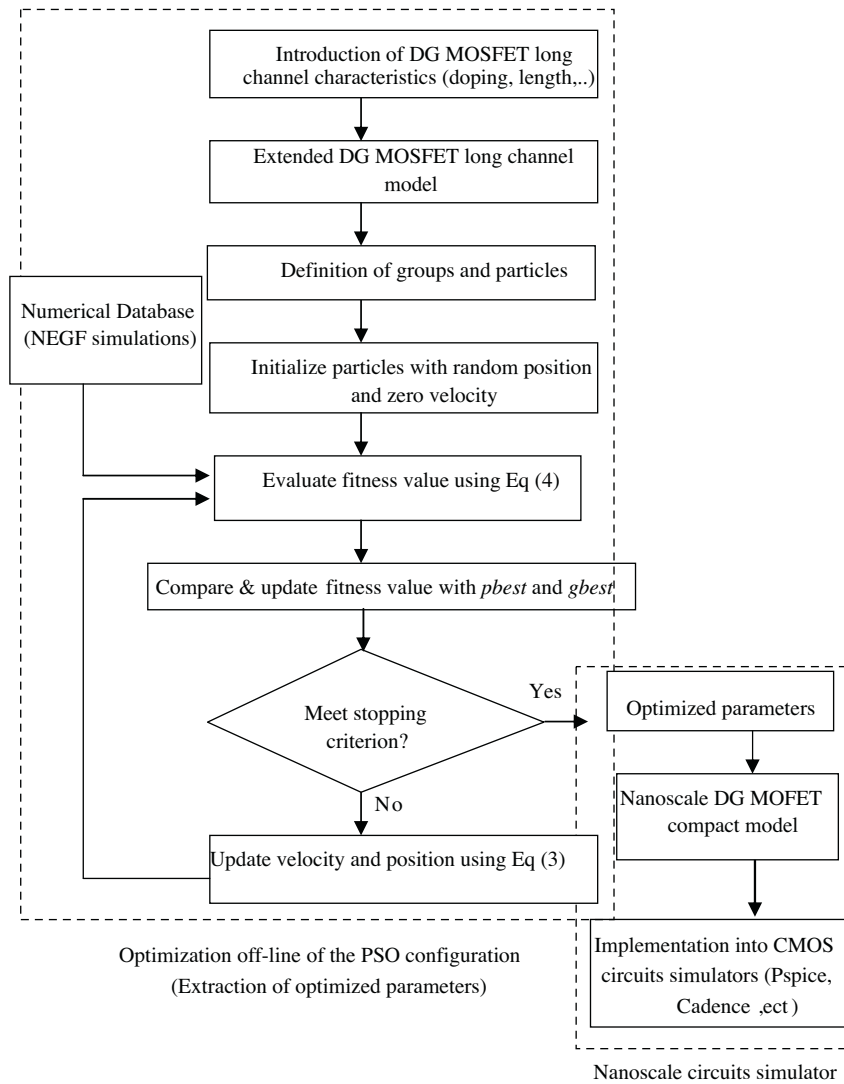
$$f = \frac{1}{M} \sum_{V_{GS}} \sum_{V_{DS}} \left[\frac{I_{DS,NUM} - I_{DS,PSO}}{I_{DS,NUM}} \right]^2, \tag{4}$$

where f is the fitness value; $I_{DS,PSO}$ is the predicted drain current based on PSO computation; $I_{DS,NUM}$ represents the target function (numerical results based on 2-D numerical non-equilibrium Green's function ,NEGF, simulation); and M represents the number of samples (database size). It is aimed to minimize this fitness function in order to improve the accuracy of the compact drain current model for nanoscale DG MOSFETs. The flowchart of our approach used in this study is detailed in Figure 2.

3. Results and discussions

For the purpose of optimization of (4), routines and programs for PSO computation were developed using MATLAB 6.5 and all simulations are carried out on a computer with a 2.8 GHz Pentium IV and 500 MB RAM. The optimization process was based on a population of 20 particles, and a maximum number of generations equal to 8000; in each iteration, the Position of each particle is updated using its velocity vector (parameters updated) and the optimization error was recorded. The three steps of velocity update, position update, and fitness calculations are repeated until a desired configuration of the particles and their movement towards g_{best} (best particle). The parameters of PSO were varied and the error was recorded. So, they allowed us to obtain an optimal configuration of the particles positions and their movement towards g_{best}.

Table 1 shows the PSO parameters used in this study. For this optimized PSO configuration, the obtained fitness function is equal to 0.001 and almost all cases have been correctly studied.

Figure 2. Flowchart of our PSO-based computation approach.

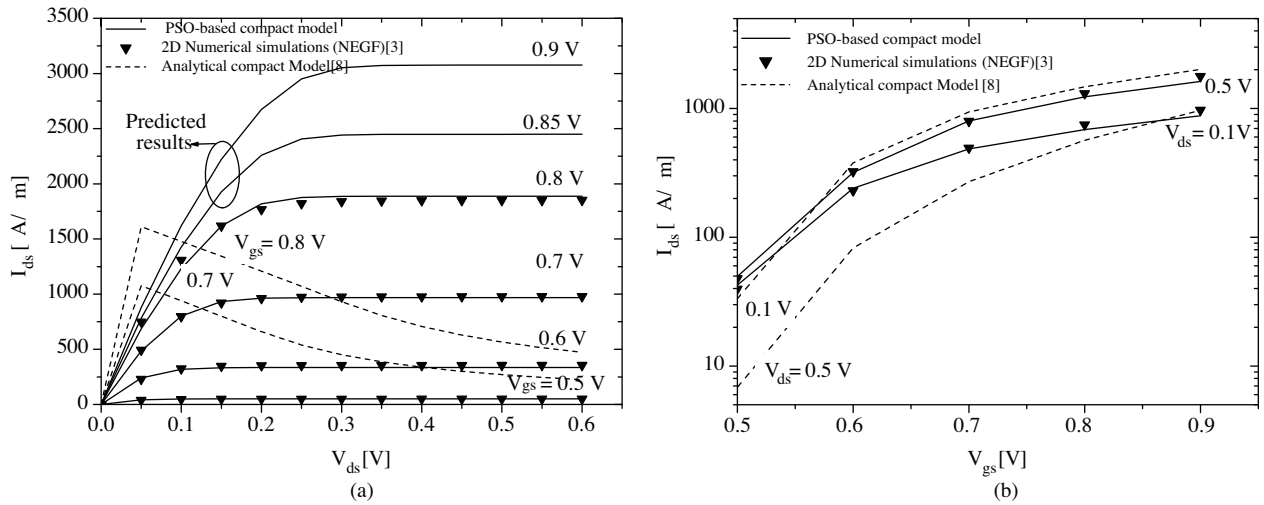**Table 1.** Parameters of the PSO optimization process.

PSO parameters
Swarm size: 20
Maximum number of generations: 8000
c_1, $c_2 = 1, 1$
w, r_1 and r_2 = random values
Obtained fitness value: $1.6.10^{-3}$
Computational time: 3500s

Table 2 summarizes the obtained fitness values for different channel lengths. In order to validate the predictive property of the optimized PSO configuration, a numerical (NEGF) set was compared to the PSO

optimized drain current model. Figure 3 shows good agreement between numerical and predicted results for the short channel length DG MOSFETs. Our simulations were carried out for a wide range of nanoscale channel lengths, from L=10 nm to L=50 nm, where we found that the rout mean square (RMS) errors are within 5%. This last observation shows the applicability of PSO technique to study the nanoscale DG MOSFETs.

Table 2. Obtained fitness values for different channel lengths.

Channel length (nm)	10	20	30	40	50
Fitness value	4.4×10^{-3}	1.7×10^{-3}	1.6×10^{-3}	2.2×10^{-3}	2.3×10^{-3}
Norm Erro (%)	5.24	3.24	3.23	4.06	4.23

Figure 3. Current-voltage characteristics (I-V) calculated from the PSO-based compact model (solid lines), compared with numerical results (symbols) and analytical model (dashed lines) for $L = 30$ nm: (a) I_{ds} vs. V_{ds}; (b) I_{ds} vs. V_{gs}.

In order to validate the predictive property of the optimized PSO configuration, numerical and analytical sets were compared to the PSO-based drain current model. Table 4 gives a comparison of the central processing unit (CPU) time requirements for simulating nano-DG MOSFET with various approaches where the PSO model computation time should be compared to the orders of magnitude increase in computation time for more rigorous drain current models, such as those based on the analytical and numerical computations. The obtained results can be explained by the fact that the evolutionary techniques are characterized as computational models based on parallel distributed processing of data. Hence, the evolutionary computation provides a practical insight into the transport coefficients modeling in materials without the uncertain accuracy or meticulous tuning effort that face more rigorous mobility models. The evolutionary-based modeling is a step towards a new generation of simulation tools that will allow device and material engineers to explore new classes of electronic devices.

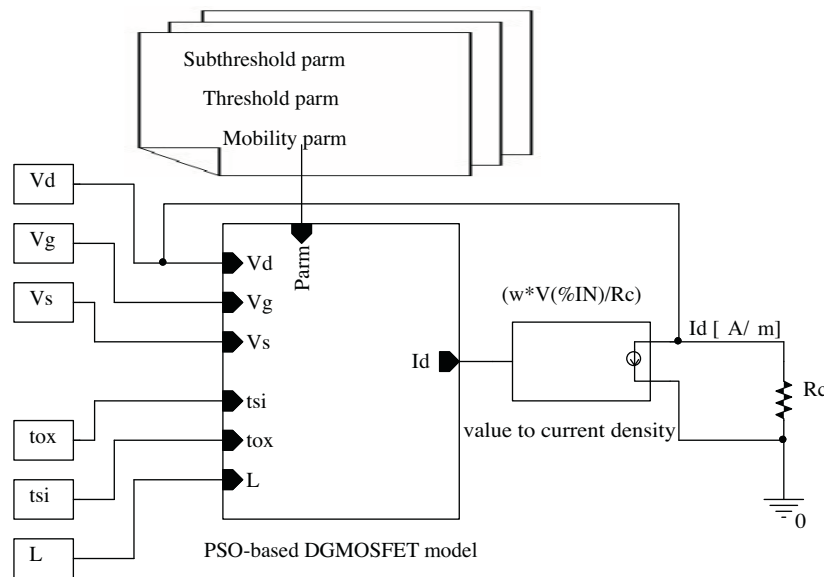## 3.1. Implementation of the PSO-based compact model

In order to validate our PSO-based model, we propose the simulation of the nanoscale CMOS inverter, which is considered the most basic element of digital VLSI circuits [16]. As the CMOS technology enters the nanoscale

regime, quantum effects and SCE become more and more important and consequently a quantum-mechanical simulation of a DG MOSFET is necessary.

Table 3. Comparison between the various approaches of modeling of the DG MOSFETs for 13 drain-source biasing voltages and 5 gate-source biasing voltages.

Approach	CPU time (s)	Effectiveness of the approach
-Real-space NEGF [3] -Manual parameters adjustment - analytical compact model [8] - Our PSO-based compact model	Hours Hours/days Several minutes 3500	Accurate/ slow Less accurate/ very slow Less accurate/ fast Accurate/ fast

In this study, using the developed PSO-based model, we have simulated an inverter gate. The purpose of this simulation is to study the evolution of nano-CMOS inverter transfer curves ($V_{out} - V_{in}$). Each inverter consists of two DG MOSFETs. The I-V characteristics of each DG MOSFET were predicted using the ABM PSO-based model (Analog Behavioral Modeling) as it is shown in Figure 4.

Figure 4. Detailed diagram of the ABM-based Pspice macromodel for PSO-based DG MOSFET model.

The Pspice input/output signals of our PSO-based inverter gate are shown in Figure 5a. Figure 5b shows the transfer curves for the designed CMOS inverters for different channel lengths. It is clear that, as the gate length decreases, the SCEs become more and more serious. Consequently they degrade the performance (voltage gain) of the nano-CMOS inverters. In practice, a high inverter voltage gain can provide a high transition speed of nano-CMOS inverter and better performance of digital operations.
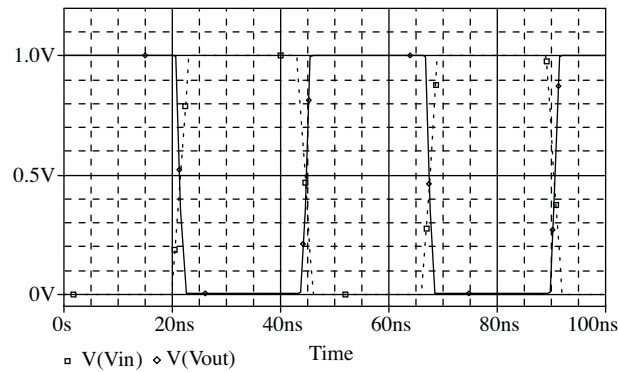
Figure 5a. The Pspice input and output signals of our PSO-based nanoscale inverter gate (L=30nm).
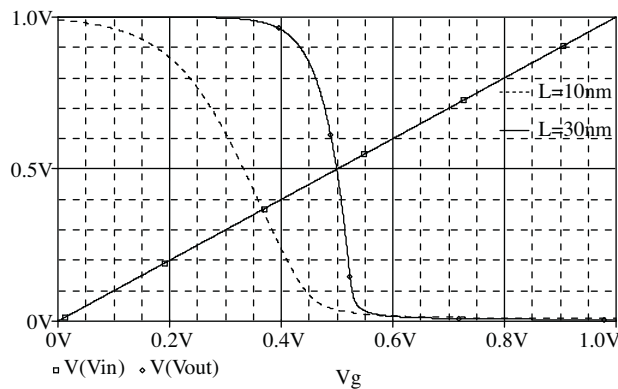

Figure 5b. The transfer curves predicted with PSO-based model as function of channel lengths.

4. Conclusion

In this paper, we showed the applicability of the PSO approach to the nanoscale CMOS circuits simulation problem. The use of 2-D NEGF numerical simulations and our extended long channel DG MOSFET compact model enabled us to build the required database and adjustment parameters in order to evaluate and optimize our short channel DG MOSFET compact model. The model optimization process was completed in a relatively short time, with no need for user intervention during the search. The encouraging comparisons between numerical results and our compact model simulations have indicated that the developed PSO-based approach is particularly suitable to be incorporated in electronic devices simulators to study the nanoscale CMOS circuits.

Nomenclature

N_A	channel doping	n_1	ideality factor
L	channel length	C_{si}	silicon capacitance
T	temperature	C_{ox}	oxide capacitance
t_{si}	silicon thickness	μ_{eff}	effective mobility
t_{ox}	oxide thickness	μ_T	low field mobility
q_s	normalized charge at the source	v_{sat}	saturation velocity
q_d	normalized charge at the drain	ϕ_B	barrier voltage

V_{fb}	flat band voltage	m	number of compounds
V_{ch}	channel voltage	r_1	random number
I_{ds}	drain current	r_2	random numbers
Vt_0	threshold voltage	v_j	velocity of particle
n	number of particles in the swarm	x_j	position of particle
t	number of generations	$pbest_j$	local best of particle j
w	inertia weight factor	$gbest_j$	global best of the group
c_1	cognitive acceleration factor	f	fitness value
c_2	social acceleration factor		

References

[1] A. Kranti , T. M. Chung, D. Flandre and J.P. Raskin, "Analysis of quasi double gate method for performance prediction of deep submicron double gate SOI MOSFETs", Semicond Sci. Technol, Vol. 20, pp. 423–429, 2005.

[2] J. G. Fossum, L. Ge and M.H. Chiang, " Speed superiority of scaled double-gate CMOS" IEEE Trans. Electron Devices, Vol. 49, pp. 808–811, 2002.

[3] F. Djeffal, M. Chahdi, A. Benhaya, M.L. Hafiane, "An approach based on neural computation to simulate the nanoscale CMOS circuits: Application to the simulation of CMOS inverter", Solid State electronics, Vol. 51, pp.26-34, 2007.

[4] F. Djeffal , M.A. Abdi, Z. Dibi, M.Chahdi, A. Benhaya, "A neural approach to study the scaling capability of the undoped Double-Gate and cylindrical Gate All Around MOSFETs", Materials Sci and Eng: B, Vol.147, pp. 239-244, 2008.

[5] F. Djeffal, S. Guessasma, A. Benhaya1, T. Bendib, " A neural computation to study the scaling capability of the undoped DG MOSFET". Semiconductor Physics, Quantum Electronics & Optoelectronics", Vol.11, pp.196-202, 2008.

[6] HA .El-Hamid, J. Roig, B. Iniguez, "Analytical predictive modelling for the study of tha scalability limits of multiple gate MOSFETs", Solid State electronics, Vol(51),pp 414-422, 2007.

[7] S. Datta , "Nanoscale device modelling: the Green's function method", Superlattices Microstruct, Vol (28), pp.253-278, 2000.

[8] Y.Taur , X. Liang, W. Wang, H. Lu, "Continuous analytic drain current model for DG MOSFETs", IEEE Electron Dev Lett, Vol (25), pp.107-109, 2004.

[9] J.Kennedy, R.C. Eberhart, " Particle swarm optimization", In: Proceedings of the IEEE International Conference on the Neural Networks, Piscataway, NJ: IEEE Service Center, pp.1942-1948, 1995.

[10] F. Djeffal , D. Arar, N. Lakhdar, T. Bendib, Z. Dibi and M. Chahdi, "An approach based on particle swarm computation to study the electron mobility in wurtzite GaN", Microelectronic. J, Vol(40), pp. 357-359, 2009.

[11] K.W. Chau, "A split-step particle swarm optimization algorithm in river stage forecasting", J. Hydrology, Vol (346), pp. 131-135, 2007.

[12] M. Chan, Y. Taur, C-H. Lin, J. He, A.M. Niknejad, C. Hu, A framework for generic physics based double-gate MOSFET modeling, in Technical Proceedings of the 2003 Nanotechnology Conference and Trade Show, Volume 2, Sun Francisco California, p270, 2003.

[13] S. Selberherr, "Analysis and Simulation of Semiconductor Devices", Wien: Springer- Verlag, 1984.

[14] R. Venugopal , Z. Ren, S. Datta, M.S. Laundstrom, "Simulating quantum transport in nanoscale MOSFETs: real vs. mode space approaches", J. Appl Phys, Vol (92), pp. 253-278, 2002.

[15] G. Baccararni, S. Reggiani, "A compact double-gate MOSFET model comprising quantum- mechanical and non-static effects", IEEE Trans. Electron Devices, Vol (46), pp.1656–1666, 1999.

[16] Y.Taur, T.H. Ning, "Fundamentals of modern VLSI devices", Cambridge (UK): Cambridge university press, 1998.