

# Four quadrant FGMOS analog multiplier

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## Abstract

*A novel four-quadrant analog multiplier using floating gate MOS (FGMOS) transistors operating in the saturation region is presented. The drain current is proportional to the square of the weighted sum of the input signals. This square law characteristic of the FGMOS transistor is used to implement the quarter square identity by utilizing only six FGMOS transistors. The main features of this remarkably simple multiplier circuit configuration are the large input signal range equal to 100% of the supply voltage, nonlinearity of 0.0081%, bandwidth of 1.4–1.5 GHz and THD of maximum 2.67% (while the inputs are at their maximum values).*

**Key Words:** *FGMOS, four quadrant analog multiplier, rail-to-rail, differential amplifier*

## 1. Introduction

Four quadrant analog multipliers are important building blocks in neural networks and many signal processing circuits like correlators, convolvers, adaptive filters, modulation detection, frequency translation, etc. Several techniques of implementing four-quadrant analog multipliers, using MOS technology, have been reported. They are the variable transconductance technique (modified Gilbert cell) [1–3], the voltage-controlled transconductance technique, which employs MOS transistors operating in the triode region [4–6], the bias feedback technique [7], techniques based on square-law characteristics of MOS transistors operating in the saturation region, implementing either the quarter-square identity [8–10] or other algebraic identity [11–12], and the technique based on linear transconductors [13–15]. The Gilbert six-transistor cell (GSTC), using the variable transconductance technique, is very popular in bipolar technology since its output current has a linear relationship with the tail current source which allows a nonlinear relationship with input signals  $V_x$  and  $V_y$ , to be compensated simply by an appropriate predistortion circuit [16]. However, the output current of a MOS transistor multiplier, based on the modified GSTC, has a nonlinear relationship with the tail current source and makes compensation by a predistortion circuit very difficult [2]. This limits the linear input range of the multiplier to only a few hundred millivolts [1]. On the other hand, most of the square-law based multipliers reported so far have input signal range limited to about 50% of the supply voltage range.

In this paper, a novel four-quadrant analog multiplier using floating-gate MOS (FGMOS) transistors operating in the saturation region is presented. The drain current is proportional to the square of the weighted sum of the input signals. This square law characteristic of the FGMOS transistor is used to implement the

quarter square identity by utilizing only six FGMOS transistors. The main features of this remarkably simple multiplier circuit configuration are the large input signal range equal to 100% of the supply voltage, nonlinearity of 0.0081%, bandwidth of 1.4 GHz and THD of maximum 2.67% (while the inputs are at their maximum values).

Remainder of this paper is organized as follows. In Section II, the basic structure of the FGMOS transistor is described. The principle of operation of the FGMOS differential pair and four-quadrant analog FGMOS multiplier are presented in Section III and Section IV, respectively. Simulation results of the proposed circuit are shown in Section V followed by conclusion in Section VI.

## 2. The FGMOS transistor

Floating gate (FG) MOSFETs are being utilized in a number of new and exciting analog applications [17–22]. These devices are available in standard CMOS technology because they are being widely used in digital circuits. Thus floating gate devices are now finding wider applications by analog researchers. As a result the floating gate devices are not only used for memories but are also being used as circuit elements. FGMOS transistors are used as analog memory elements, as part of capacitive biased circuits, and as adaptive circuit elements [17]. An FGMOS can be fabricated by electrically isolating the gate of a standard MOS transistor, so that there are no resistive connections to its gate. A number of secondary gates or inputs are then deposited above the floating gate (FG) and electrically isolated from it. These inputs are only capacitively connected to the FG, since the FG is completely surrounded by highly resistive material. So, in terms of its DC operating point, the FG is a floating node [17]. The equivalent schematic for an  $n$ -input  $n$ -channel FGMOS transistor is given in Figure 1.

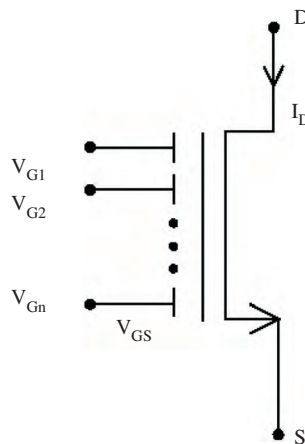


Figure 1. Diagram of a  $n$ -input  $n$ -channel FGMOS transistor.

## 3. FGMOS differential pair

There are two types of FGMOS differential pair. One of them is biased by a floating voltage source and the other is biased by a non-floating voltage source [18]. The differential pair, which is biased by floating voltage source, cannot have a rail-to-rail range and the floating voltage source may limit its common mode swing range if the floating voltage source cannot swing out of the supply rails. Figures 2(a) and 2(b) shows the differential pairs biased by floating voltage source and non-floating voltage source, respectively.

To derive under what condition we can get a rail-to-rail input common mode range for the differential pair biased by non-floating voltage source, it is known that for 2-input floating gate transistors  $V_F = w_0V_0 + w_1V_1 + w_2V_2$  where  $w_i = C_i / C_{tot}$ ,  $i = 0, 1, 2$ . Normally,  $C_i$  is much larger than  $C_0$ , which means  $w_0$  is very small and the approximation  $w_1 + w_2 = 1$  can be assumed. When  $V_{iCM}$  (common mode input voltage) is  $V_{DD}$ , for a n-type transistor, the floating gate can be  $V_{DD}$ , as long as  $V_{DRAIN}$  is greater than  $V_{DD} - V_{TN}$ . So, for the differential pair biased by non-floating voltage source,  $V_b$  can directly be  $V_{DD}$ . When  $V_{iCM}$  is at the negative rail ( $-V_{SS}$ ), for n-type differential pair, there is a tendency that tail current transistor will have no room to work in saturation region. We should try to increase  $V_{FG,cm}$ , the common mode voltage on the floating gate.  $V_{FG,cm}$  is given by  $V_{FG,cm} = w_1V_{iCM} + w_2V_b$ . That is, one should have a high  $V_b$ , which has the maximum value of  $V_{DD}$ . Let  $V_b = V_{DD}$ ; so, when  $V_{iCM} = -V_{SS}$ ,  $V_{FG,cm} = w_1V_{iCM} + w_2V_b = -w_1V_{SS} + w_2V_{DD} = -w_1V_{SS} + (1-w_1)V_{DD} = V_{DD} - w_1(V_{SS} + V_{DD})$ . To make sure  $M_1$ ,  $M_2$  and tail current transistor work properly, the following inequality should be satisfied.  $V_{FG,cm} \geq -V_{SS} + (V_{GS,M1,M2} + V_{dsat,MTAIL})$ . So, we can get from these two equations,  $(V_{DD} + V_{SS}) \geq (V_{GS,M1,M2} + V_{dsat,MTAIL}) / (1 - w_1)$ . The minimum supply voltage is  $(V_{GS,M1,M2} + V_{dsat,MTAIL}) / (1 - w_1)$  [18].

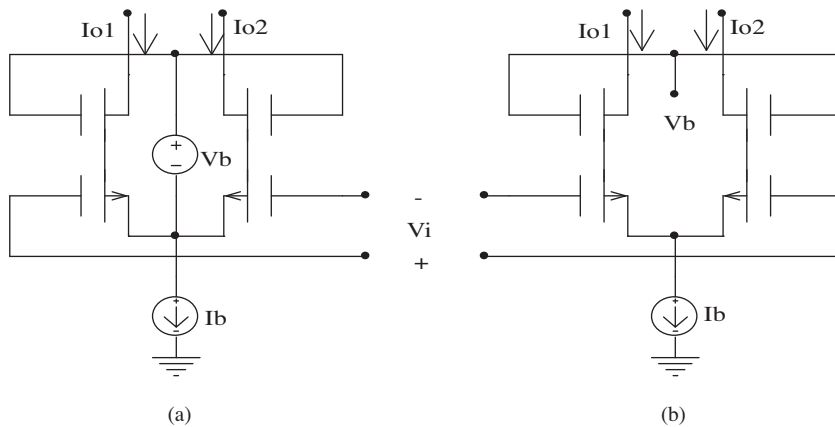


Figure 2. FGMOS differential pairs.

Figure 3 shows the output drain current of the differential pair biased by non-floating voltage source. To show how the input voltage swing is increased by using FGMOS transistors, output drain currents of both conventional differential pair and FGMOS differential pair are plotted together on the same axis. As it is seen from the figure, input voltage swing is increased by using FGMOS transistors.

## 4. Four quadrant FGMOS analog multiplier

Figure 4(a) shows a conventional multiplier circuit based on the folded CMOS Gillbert Cell. Figure 4(b) shows the proposed floating gate multiplier circuit; this is based on the topology given in [2], employing FGMOS differential pairs instead of conventional pairs to improve the circuit behavior. Transistors  $M1a$ ,  $M1b$  form one differential pair where as  $M2a$ ,  $M2b$  form the other. They are cross connected by connecting the drains of the transistors  $M1a$ ,  $M2a$  and  $M1b$ ,  $M2b$  together. A differential input  $V_X$  is applied to the cross connected differential pairs while the other differential input  $V_Y$  is applied to the differential pair formed by  $M3a$  and  $M3b$ .  $M3a$  and  $M3b$  transistors form tail transistors for the two differential pairs. The bias currents

( $I_{SS1} = I_{SS2} = I_{SS3} = I_{SS}$ ) are provided as tail currents to the differential pairs. A preliminary version of this work appeared in a previous work of the authors [22].

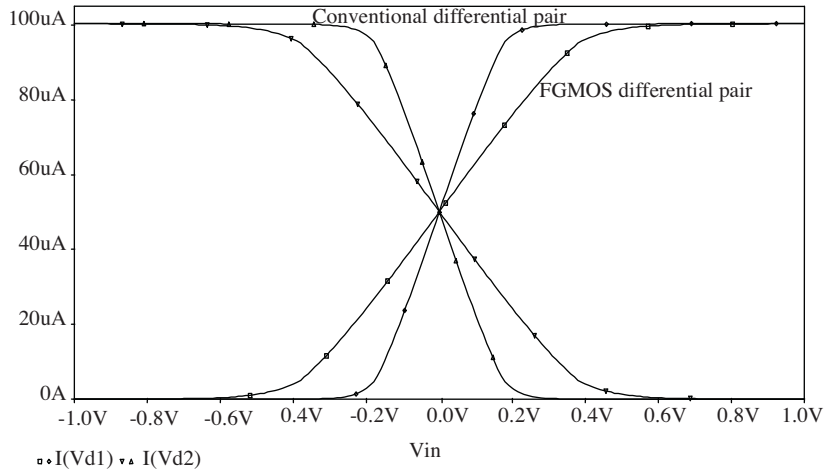


Figure 3. Output drain current of the differential pair biased by non-floating voltage source.

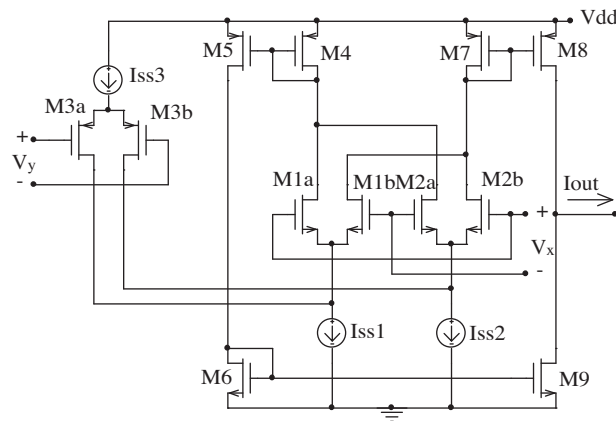


Figure 4(a). Conventional multiplier circuit.

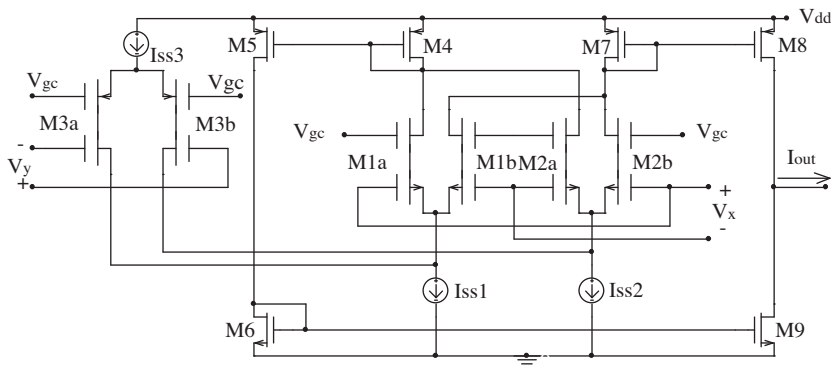


Figure 4(b). Proposed floating gate multiplier circuit.

Each transistor in differential pairs has two inputs which are applied through two equal sized capacitors,  $C_i$ . The differential signals of the inputs are applied to one of the floating gates in the differential pairs.  $V_X$  and  $V_Y$  act as input signals while  $V_{GC}$  as a control voltage to the floating gates. Since the voltage at the gate is less than the input voltage the differential pair transistors can work in saturation even when large signals are applied. This leads to increase the input dynamic swing.

In order to find out the input swing of the FGMOS differential amplifier, floating gate voltages of the input transistors and  $\partial\Delta I_D / \partial\Delta V_{in}$ , are given as

$$V_{FG1} = \frac{C_1}{C_T}V_1 + \frac{C_2}{C_T}V_{GC} \quad (1)$$

$$V_{FG2} = \frac{C_1}{C_T}V_2 + \frac{C_2}{C_T}V_{GC} \quad (2)$$

$$\frac{\partial\Delta I_D}{\partial\Delta V_{in}} = \frac{1}{2}\mu C_{OX} \frac{W}{L} \frac{C_1}{C_T} \frac{\frac{4I_{SS}}{\mu C_{OX} \frac{W}{L}} - 2\Delta V_{in}^2 \left(\frac{C_1}{C_T}\right)^2}{\sqrt{\frac{4I_{SS}}{\mu C_{OX} \frac{W}{L}} - \Delta V_{in}^2 \left(\frac{C_1}{C_T}\right)^2}}. \quad (3)$$

From equation (3), one can derive

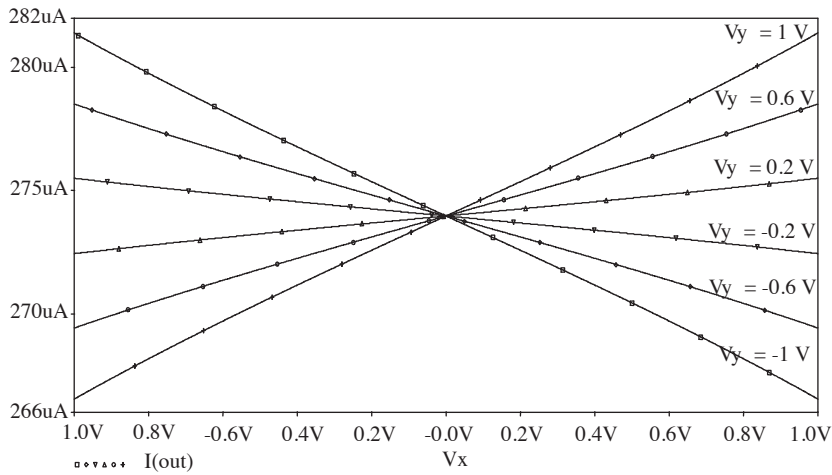
$$\Delta V_{in} = \frac{C_T}{C_1} \sqrt{\frac{2I_{SS}}{\mu C_{OX} \frac{W}{L}}}. \quad (4)$$

Relation (4) shows FGMOS transistors exhibit a voltage swing proportional to the factor  $C_T / C_1$ .

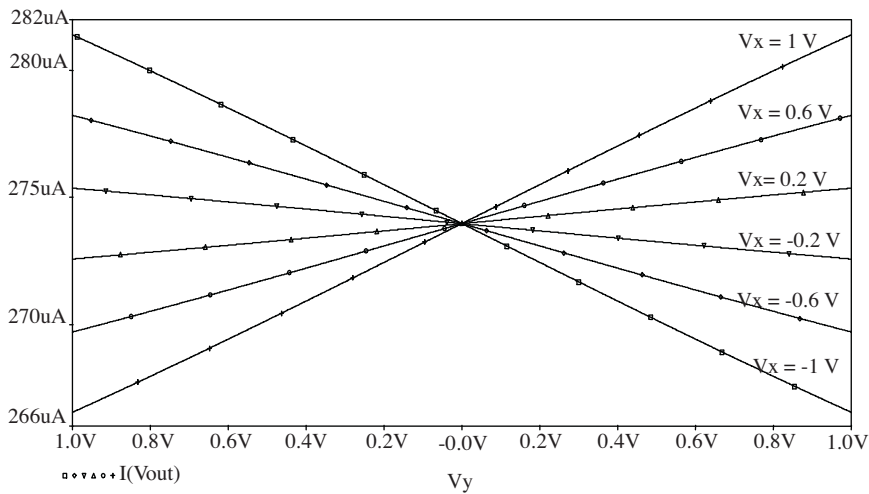
## 5. Simulation results

The proposed circuit of Figure 4(b) was simulated using 0.35  $\mu\text{m}$  TSMC technology parameters. The supply voltage is  $V_{DD} = 2\text{ V}$ ,  $V_{GC}$  is set to  $V_{DD}$  for n-type FGMOS and is set to ground for p type FGMOS. The tail currents are  $I_{SS1} = I_{SS2} = I_{SS3} = 100\ \mu\text{A}$ . The input capacitor value is  $C_i = 32.5\ \text{fF}$ ; and values of  $C_{FGD}$  and  $C_{FGS}$  are calculated as 0.395 fF and 3.25 fF, respectively. The dimension for cross connected differential pair transistors M1a, M1b, M2a and M2b is  $W/L = 1.4\ \mu\text{m} / 0.7\ \mu\text{m}$ , for M3a and M3b is  $W/L = 2.8\ \mu\text{m} / 0.7\ \mu\text{m}$ . The current ratio of the transistors M4, M5 and M7, M8 is chosen as  $I_{D5} / I_{D4} = I_{D8} / I_{D7} = 5$ .

Figures 5(a) and 5(b) show the DC transfer characteristics of the proposed circuit. In Figure 5(a) DC voltage  $V_Y$  was stepped between -1 V and 1 V with 0.4 V step size while the DC voltage  $V_X$  was swept from -1 V to 1 V and the reverse is applied in Figure 5(b). The nonlinearity of the circuit was simulated as 0.0081% under full scale input conditions.



**Figure 5(a).** DC transfer characteristics of the proposed multiplier circuit ( $I_{OUT} = I_{out}(V_X)$ ,  $V_Y$  is taken as parameter).



**Figure 5(b).** DC transfer characteristics of the proposed multiplier circuit ( $I_{OUT} = I_{out}(V_Y)$ ,  $V_X$  is taken as parameter).

Figure 6 shows the DC transfer characteristics of the proposed circuit and the conventional MOS circuit together. During the simulation  $V_X$  is swept from -1 V to 1 V while  $V_Y$  takes the values of -1 V, 0 V, 1 V for proposed circuit and -30 mV, 0 V, 30 mV for the conventional CMOS circuit. As it is seen from the figure, input swing is increased by using FGMOS transistors.

Figure 7 and Figure 8 show the AC transfer characteristics of the proposed circuit and the conventional CMOS circuit together. In Figure 7  $V_X$  is set to DC 1 V and the  $V_Y$  is set to AC 1 V while the reverse case is applied in Figure 8. As it is seen from the figures, bandwidth of the multiplier circuit is increased almost 3 to 3.5 times by using FGMOS transistors.

Figure 9 shows the inputs of 10 kHz and 300 kHz sinusoidal signals with 2 V amplitudes applied at  $V_X$  and  $V_Y$ , respectively and Figure 10 shows the transient output waveform of the proposed circuit.

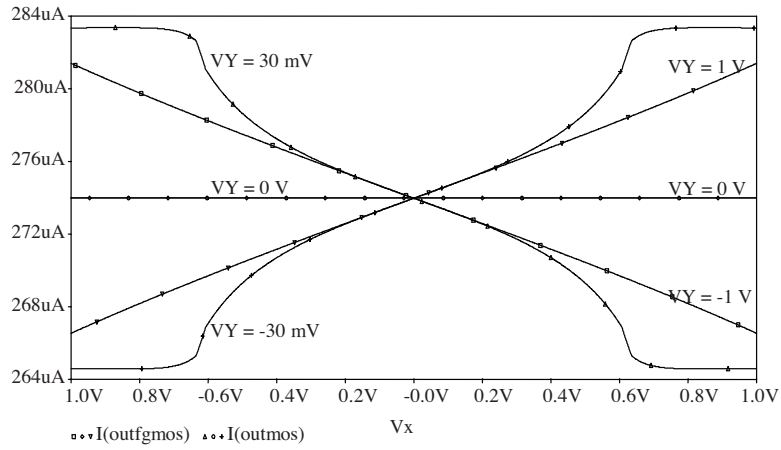


Figure 6. DC transfer characteristics of the proposed multiplier circuit and the conventional multiplier circuit.

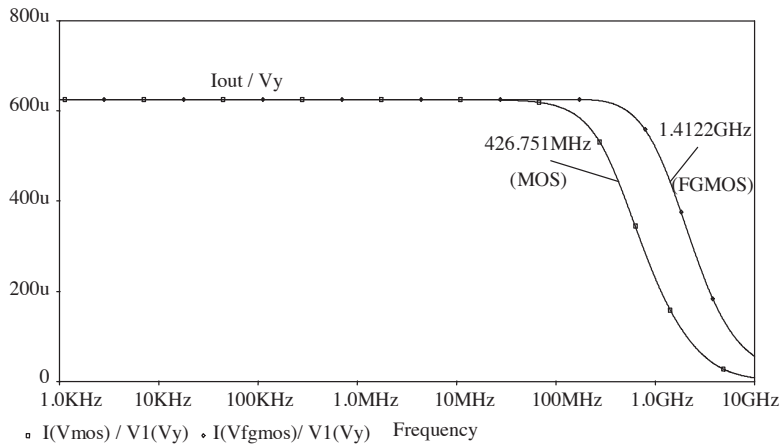


Figure 7. AC transfer characteristics ( $I_{OUT} / V_Y$ ) of the proposed multiplier circuit and the conventional multiplier circuit ( $V_X$  is set to DC 1 V).

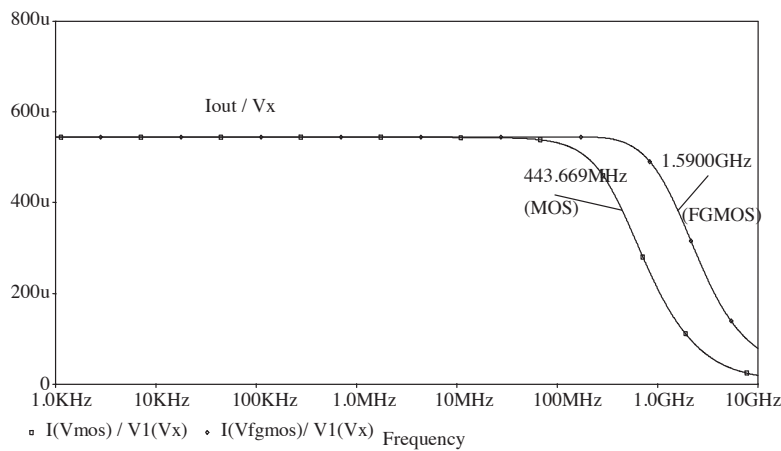


Figure 8. AC transfer characteristics ( $I_{OUT} / V_X$ ) of the proposed multiplier circuit and the conventional multiplier circuit ( $V_Y$  is set to DC 1 V).

Figure 11 shows the THD variation of the proposed circuit and the conventional CMOS circuit together due to the input voltage swing of  $V_Y$  between 0 V and 1 V while  $V_X$  is set to 1 V DC. Total harmonic distortion of the proposed circuit under full scale input conditions ( $V_X = 2$  V,  $V_{Y_{max}} = 2$  V) is 2.67 %.

The extended linearity provided by the proposed circuit has been demonstrated on the intermodulation distortion properties by applying 10 kHz and 300 kHz signals of 2 V amplitude respectively to the X and Y inputs, the resulting output products are investigated by SPICE simulations. Intermodulation products of the frequencies  $f_1 + f_2 = 310$  kHz and  $f_1 - f_2 = 290$  kHz are taken as 0 dB, and the other products are normalized to those values. The intermodulation products obtained are illustrated in Table 1. It is obvious from the results that the intermodulation products at the output of the proposed circuit of Figure 4(b) are considerably lower than those at the output of the conventional multiplier topology of Figure 4(a).

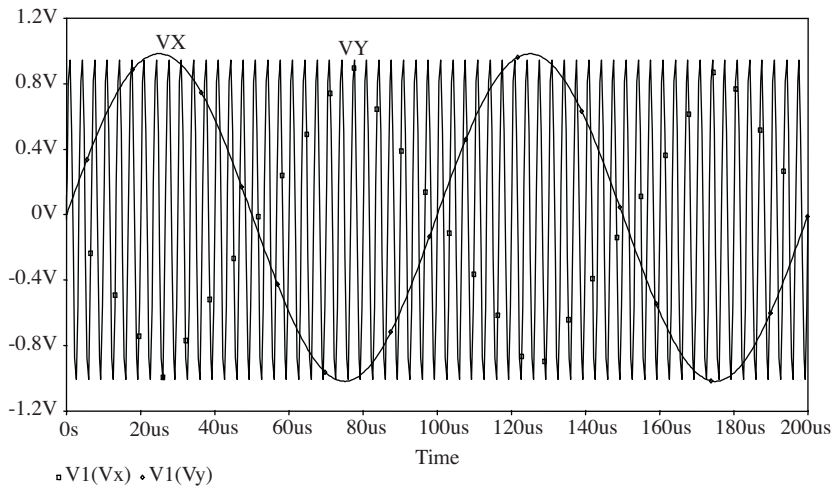


Figure 9. Input signals  $V_X$  and  $V_Y$  of the proposed circuit.

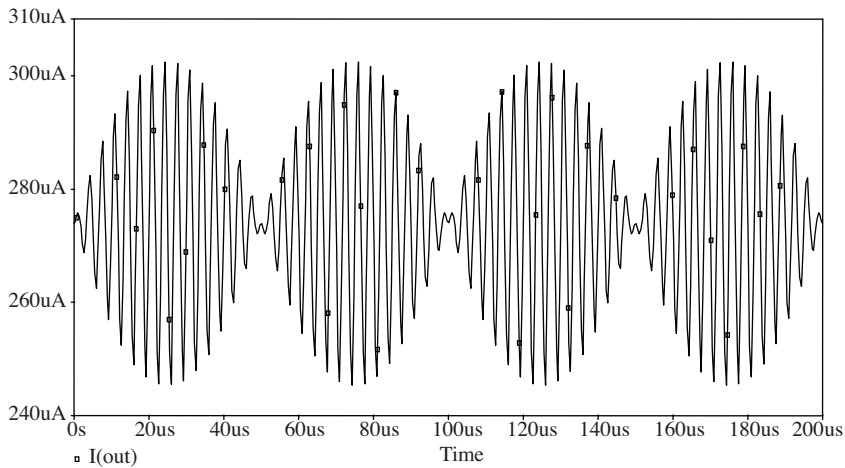
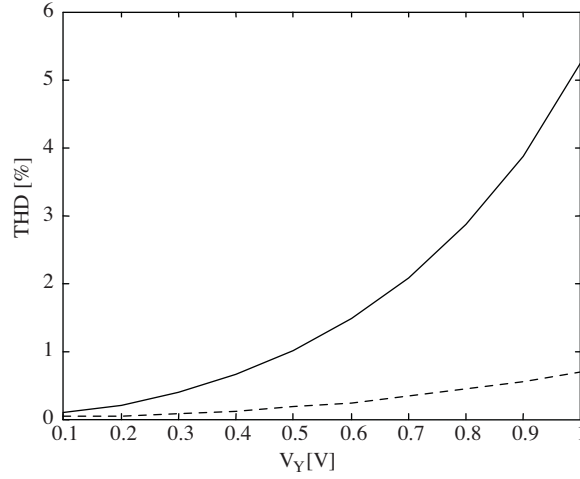


Figure 10. Transient output waveform of the proposed circuit.

Table 2 summarizes the main characteristics of the proposed FGMOS multiplier, drawing at the same time a comparison with the conventional CMOS multiplier. As can be seen, the proposed multiplier has better results than the conventional multiplier in all characteristics which are mentioned in the Table 2.





**Figure 11.** THD variation due to the input voltage swing of  $V_Y$  while  $V_X$  is set to 1 V DC.

**Table 1.** Intermodulation products of the proposed multiplier and conventional multiplier.

Frequency	Proposed Multiplier	Conventional Multiplier
10 kHz	-77.7 dB	-41.68 dB
30 kHz	-79.06 dB	-41.85 dB
50 kHz	-79.07 dB	-53.18 dB
270 kHz	-23.17 dB	-10.69 dB
290 kHz	0 dB	0 dB
300 kHz	-77.87 dB	-43.66 dB
310 kHz	0 dB	0 dB
330 kHz	-23.37 dB	-10.67 dB
570 kHz	-80 dB	-49.35 dB
590 kHz	-79.77 dB	-40.3 dB
600 kHz	-58.25 dB	-39 dB
610 kHz	-81.49 dB	-44.28 dB
630 kHz	-80.15 dB	-39.1 dB

**Table 2.** Comparison between the proposed multiplier and conventional multiplier.

	Proposed Multiplier	Conventional Multiplier
Input voltage swing	100% (supply)	25% (supply)
Nonlinearity	0.0081%	0.092%
THD	0.688%	5.245%
Bandwidth ( $I_{out} / V_x, I_{out} / V_y$ )	1.59 GHz, 1.41GHz	443.67 MHz, 426.75 MHz

## 6. Conclusions

A novel FGMOS four quadrant multiplier has been designed and simulated. It is based on the square law dependence of the drain current on the weighted sum of the input signals. The circuit configuration is remarkably simple. It has a large input voltage range equaling the supply voltage. Significantly larger input capacitances have been employed in our circuit, therefore reducing mismatching effects and contribution of

parasitic capacitances, but at the same time increasing area and reducing the bandwidth, which is 1.4–1.5 GHz. The measured nonlinearity and total harmonic distortion are 0.0081% and 2.67% under full scale input conditions, respectively.

## References

- [1] D. C. Soo, R. G. Meyer, "A four-quadrant NMOS analog multiplier," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 6, pp. 1174–1178, December, 1982.
- [2] J. N. Babanezhad, G. C. Temes, "A 20-V four-quadrant CMOS analog multiplier," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 6, pp. 1158–1168, December, 1985.
- [3] S. C. Qin, R. L. Geiger, "A  $\pm 5$ -V CMOS analog multiplier," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 6, pp. 1143–1146, December, 1987.
- [4] M. Yasumoto, T. Enomoto, "Integrated MOS four-quadrant analog multiplier using switched-capacitor technology for analog signal processor IC's," *IEEE J. Solid-State Circuits*, vol. SC-20, no. 4, pp. 852–859, August, 1985.
- [5] B. S. Song, "CMOS RF circuits for data communication application," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 2, pp. 310–317, April, 1986.
- [6] C. W. Kim, S. B. Park, "New four-quadrant CMOS analog multiplier," *Electron. Lett.*, vol. 23, no. 24, pp. 1268–1270, November, 1987.
- [7] S. I. Liu, Y. S. Hwang, "CMOS four-quadrant multiplier using bias feedback techniques," *IEEE J. Solid-State Circuits*, vol. 29, no. 6, pp. 750–752, June, 1994.
- [8] J. Pena-Fino, J. A. Connelly, "A MOS four-quadrant analog multiplier using the quarter-square technique," *IEEE J. Solid-State Circuits*, vol. SC-22, no. 6, pp. 1064–1073, December, 1987.
- [9] H. G. Song, C. K. Kim, "A MOS four-quadrant analog multiplier using simple two-input squaring circuits with source followers," *IEEE J. Solid-State Circuits*, vol. 25, no. 3, pp. 841–848, June 1990.
- [10] C. W. Kim, S. B. Park, "Design and implementation of a new four quadrant MOS analog multiplier," *Analog Integrated Circuits and Signal Processing*, vol. 2, pp. 95–103, 1992.
- [11] Z. Hong, H. Melchior, "Analogue four-quadrant CMOS multiplier with resistors," *Electron. Lett.*, vol. 21, no. 12, pp. 531–532, June, 1985.
- [12] F. Keles, T. Yildirim. "Pattern recognition using n- input neuron circuits based on floating gate MOS transistors." *International IEEE Region 8 Conference EUROCON 09*, pp. 224–229, Saint Petersburg, Russia, May 2009.
- [13] K. Bult, H. Wallinga, "A CMOS four-quadrant analog multiplier," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 3, pp. 430–435, June, 1986.
- [14] S. L. Wong, N. Kalyansundaram, C. A. T. Salama, "Wide dynamic range four-quadrant CMOS analog multiplier using linearized transconductance," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 6, pp. 1120–1122, December, 1986.
- [15] Z. Wang, "A CMOS four-quadrant analog multiplier with single-ended voltage output and improved temperature performance," *IEEE J. Solid-State Circuits*, vol. 26, no. 9, pp. 1293–1301, September, 1991.
- [16] P. R. Gray, R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, 2nd ed. New York: Wiley, pp. 593–605, 1984.
- [17] E. Rodriguez-Villegas, *Low Power and Low Voltage Circuit Design with the FGMOS transistor*, The Institution of Engineering and Technology, London, United Kingdom, 2006.

- [18] Edgar Sánchez-Sinencio, Floating Gate Techniques and Applications: A Tutorial, Analog and Mixed-Signal Center TAMU, 2000.
- [19] F. Keles, T. Yildirim. Low voltage low power neuron circuit design based on subthreshold FGMOS transistors and xor implementation, 11th international Workshop on Symbolic and Numerical Methods Modeling and Applications to Circuit Design- SM2ACD 2010. pp. 1-5, Tunis-Gammarth, Tunisia, 2010.
- [20] S. S. Jamuar, S. Sharma, S. S. Rajput, "Analog Signal processing Using FGMOS Based Structures: A Tutorial," J. Of Active and Passive Electronic Devices, vol. 3, pp. 109–124, 2008.
- [21] I. Navarro, A.J. Lopez-Martin, C. A. de la Cruz, A. Carlosena, "A compact low-voltage four quadrant FGMOS multiplier," International Conference on Electronics, Circuits and Systems, pp. 393–396, Scottsdale, Arizona, 2002.
- [22] S. Keleş, H. H. Kuntman, "Four Quadrant FGMOS Multiplier," Proceedings of ELECO'2009: The 6th International Conference on Electrical and Electronics Engineering, Vol. 2, pp. 45–48, Bursa, Turkey, November 2009.