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A unified series-parallel active filter system for nonperiodic disturbances

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Abstract

This paper presents a 3-phase, 4-wire unified series-parallel active filter (USPAF) system for periodic and nonperiodic disturbance compensation using a generalized nonactive power theory. The USPAF system consists of a series active filter (AF), parallel AF, and split DC-link capacitors with the midpoint of the DC-link connected to the neutral wire. The generalized nonactive power theory is applicable to single-phase or multiphase, sinusoidal or nonsinusoidal, periodic or nonperiodic, and balanced or unbalanced electrical systems. The theory was implemented previously in a parallel AF. In this study, the USPAF system is proposed to compensate for the nonsinusoidal and nonperiodic currents and voltages. Distorted source voltages, source voltage sag, and unbalanced nonlinear load current compensation were simultaneously tested in the experiments. Subharmonic and stochastic nonperiodic current and voltage compensation were simulated in MATLAB/Simulink. Simulation and experimental results verified the validity of the generalized nonactive power theory for the compensation of periodic (nonsinusoidal) and nonperiodic current and voltage disturbances with the USPAF system.

Key Words: *Active filter, harmonics, nonactive power, nonperiodic, subharmonic, unbalance*

1. Introduction

Many of the loads encountered in modern power electronics cause a significant level of nonsinusoidal and/or nonperiodic voltage and current disturbances in electrical power systems. Arc furnaces, welders, and motor drives are typical nonlinear loads that can cause not only characteristic harmonics (frequency integer multiple of the line frequency) but also subharmonic (frequency lower than the line frequency) and stochastic nonperiodic (frequency higher than the line frequency but not the integer multiple of the line frequency) components to appear in the spectra of voltages and currents [1-5].

The harmonic currents will produce voltage distortions that can affect other sensitive loads at points of common coupling (PCC) as they interact with the impedance of an electrical distribution system. These

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current and voltage waveforms are considered as nonperiodic, although mathematically the currents may still have a periodic waveform; in any event, the period of the currents is not equal to the period of the line voltage [1,2]. The effects of nonperiodic components of voltage and current are similar to those caused by harmonics. They may contribute to power loss, disturbances, measurement errors, and control malfunctions, and thus to the degradation of the power quality in distribution systems [2]. In addition, voltage sags are one of the most important power quality problems in the distribution system and are usually caused by fault conditions or by the starting of large electric motors [6].

The unified power quality conditioner (UPQC) has been widely studied to compensate for the disturbances of source voltages and load currents simultaneously. The UPQC has been applied to the compensation of voltage fluctuations related to nonperiodic waveforms in recent years [7-11]. In addition, some recent UPQC topologies have been proposed, such as UPQC with distributed generation [12], MC-UPQC [13], and modular UPQC [14], for solving power quality problems at the PCC. There are also proposed new control types for the UPQC [15-17].

Various nonactive power theories in the time domain were discussed in [18]. In previous studies, the control algorithms for current and voltage compensators were often based on the assumption that the load currents and source voltages were periodic. The generalized nonactive power theory was applied compensation of the periodic and nonperiodic load current with a parallel active filter (AF) [19,20] and static synchronous compensator (STATCOM) [21]. The theory does not specify the characteristics of voltage $\boldsymbol{v}(t)$ or current $\boldsymbol{i}(t)$; they can theoretically be any wave shape. The main objective of this paper is to compensate for the periodic (but nonsinusoidal) and nonperiodic current and voltage disturbances using the unified series-parallel active filter (USPAF) system based on the generalized nonactive power theory. The USPAF system consists of a series AF and a parallel AF combined with a common DC-link. The shunt AF compensates for the current-related problems and regulates the DC-link voltage, while the series AF compensates for voltage-related problems [7,22-24]. Figure 1 shows the general power circuit configuration of the USPAF system.

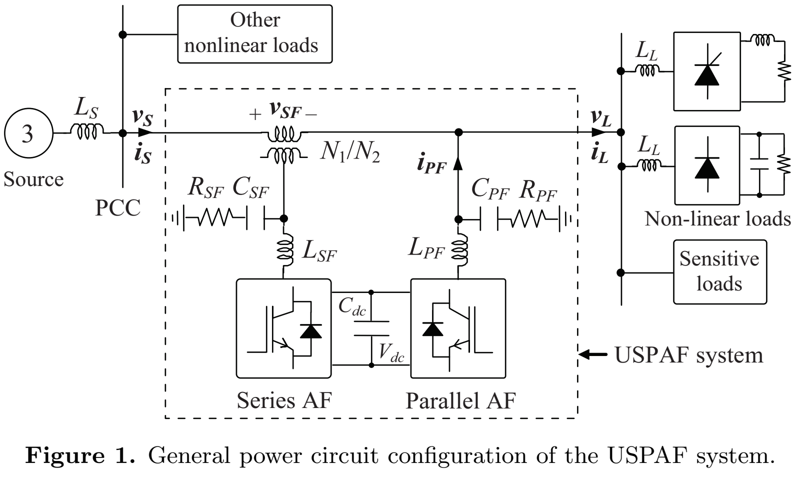

Figure 1. General power circuit configuration of the USPAF system.

The simulation and the experimental results show that the USPAF system, using the proposed theory, can regulate the load voltage, compensating for source voltage sags, voltage harmonics, and nonperiodic voltage components while simultaneously eliminating load current harmonics, unbalance, and nonperiodic current components.

2. Generalized nonactive power theory

The instantaneous nonactive power theory was first presented by Fryze [25] for periodic (but nonsinusoidal) waveforms in the time domain. The generalized nonactive power theory [19] implemented on the USPAF system is based on Fryze's idea of nonactive power and an extension of the theory proposed in [26] for periodic and nonperiodic waveforms in the time domain. In this paper, all vectors are denoted by lowercase bold letters. Voltage vector $\boldsymbol{v}(t)$ and current vector $\boldsymbol{i}(t)$ in an m-phase system are:

$$v(t) = [v_1(t),\, v_2(t), ..., v_m(t)]^T, \tag{1}$$

$$i(t) = [i_1(t),\, i_2(t), ..., i_m(t)]^T. \tag{2}$$

The instantaneous power $p(t)$ and the average power $P(t)$, which is defined as the average value of instantaneous power $p(t)$ over the averaging interval $[t - T_c,\, t]$, are

$$p(t) = v^T(t)\, i(t) \; = \sum_{k=1}^{m} v_k(t)\, i_k(t), \tag{3}$$

$$P(t) = \frac{1}{T_c} \int_{t-T_c}^{t} p(\tau)\, d\tau. \tag{4}$$

In Eq. (4), the averaging time interval T_c can be chosen manually for different cases, such as a periodic system with harmonics, a periodic system with subharmonics, or a nonperiodic system. For each case, a specific value of T_c can be chosen to fit the application or to achieve an optimal result. Instantaneous active current $\boldsymbol{i}_a(t)$ and instantaneous nonactive current $\boldsymbol{i}_n(t)$ are given by Eqs. (5) and (6).

$$i_a(t) = \frac{P(t)}{V_p^2(t)}\, v_p(t) \tag{5}$$

$$i_n(t) = i(t) - i_a(t) \tag{6}$$

In Eq. (5), voltage $\boldsymbol{v}_p(t)$ is the reference voltage which is chosen on the basis of the characteristics of the system and the desired compensation results. $V_p(t)$ is the corresponding RMS value of the reference voltage $\boldsymbol{v}_p(t)$, that is:

$$V_p(t) = \sqrt{\frac{1}{T_c} \int_{t-T_c}^{t} v_p^T(\tau)\, v_p(\tau)\, d\tau}. \tag{7}$$

Instantaneous active power $p_a(t)$ and instantaneous nonactive power $p_n(t)$ are defined by the following equations:

$$p_a(t) = v^T(t)\, i_a(t) \; = \sum_{k=1}^{m} v_k(t)\, i_{ak}(t), \tag{8}$$

$$p_n(t) = v^T(t)\, i_n(t) \; = \sum_{k=1}^{m} v_k(t)\, i_{nk}(t). \tag{9}$$

Average active power $P_a(t)$ and average nonactive power $P_n(t)$, defined by averaging the instantaneous powers over time interval $[t - T_c,\ t]$, are

$$P_a(t) = \frac{1}{T_c} \int_{t-T_c}^{t} p_a(\tau)\, d\tau, \tag{10}$$

$$P_n(t) = \frac{1}{T_c} \int_{t-T_c}^{t} p_n(\tau)\, d\tau. \tag{11}$$

The RMS values of the system voltage, active current $\boldsymbol{i}_a(t)$, nonactive current $\boldsymbol{i}_n(t)$ and current $\boldsymbol{i}(t)$ were given in [19]. The apparent power $S(t)$, apparent active power $P_p(t)$, and apparent nonactive power $Q(t)$ were also defined based on the RMS values of the voltage and currents.

In the generalized nonactive power theory, the standard definitions for an ideal 3-phase sinusoidal power system use the fundamental period T to define the RMS values, the average active power, and the nonactive power. The averaging interval T_c does not change the compensation results as long as it is an integral multiple of $T/2$, where T is the fundamental period of the system, if there are only harmonics in the load current in the periodic disturbances conditions. The nonactive current is completely compensated and a purely sinusoidal source current with a unity power factor is achieved. However, in other cases, if the disturbance is nonperiodic, such as a 3-phase load with subharmonics, or a nonperiodic load, T_c has a significant influence on the compensation results and the power and energy storage rating of the compensator's components [21]. The T_c selection procedure under these conditions is explained in Sections 4.3 and 4.4.

The choice of the time averaging interval T_c is also significant in the energy storage design consideration of the USPAF system. Choosing a longer T_c results in a smoother source current with a smaller amplitude; however, this requires that the compensator current increase as well as the energy storage requirement of the compensator. If T_c is large enough, increasing T_c further will not typically improve the compensation results significantly. Generally, there is no need to increase T_c to a larger value, as the small decrease in total harmonic distortion (THD) is often not worth the larger capital costs (higher ratings of the compensator components and therefore higher capital expenses) [19]. This depends on the frequency of the nonperiodic or periodic signal.

3. Control of the USPAF system

The USPAF system was realized as 2 3-leg voltage source inverters (VSI) with split DC-link capacitors and the generalized nonactive power theory-based voltage and current control strategies. This theory, used at first for the parallel AF, is now proposed for the USPAF system.

3.1. Voltage control strategy

The voltage control block diagram of the series AF is shown in Figure 2. In the voltage control strategy, the positive sequence detector generates auxiliary control signals (i_{a1+}, i_{b1+}, i_{c1+}) used as a reference current $\boldsymbol{i}_p(t)$ for the generalized nonactive power theory.

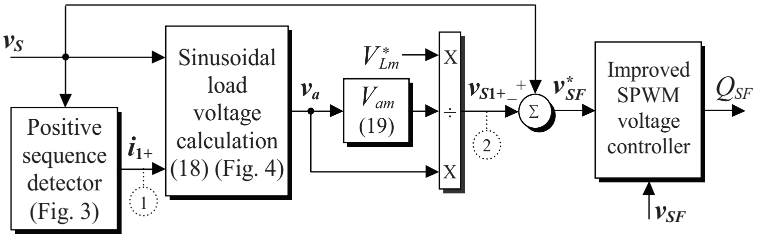
v_S
Positive sequence detector (Fig. 3)
i_{1+}
1
Sinusoidal load voltage calculation (18) (Fig. 4)
v_a
V^*_{Lm}
V_{am} (19)
X
÷
X
v_{S1+}
2
+
_
Σ
v^*_{SF}
Improved SPWM voltage controller
Q_{SF}
v_{SF}

Figure 2. Control block diagram of the series AF.

The block diagram of the positive sequence detector is shown in Figure 3. The fundamental frequency ω_1 $(2\pi 50)$ is used in a sine wave generator to produce $\sin(\omega_1 t)$ and $\cos(\omega_1 t)$ signals at unity magnitude. The source voltages (v_{Sa}, v_{Sb}, v_{Sc}) are inputs of the positive-sequence detector that includes a phase-locked loop (PLL) function. These voltages are transformed into the synchronous dq reference frame by using Eq. (12) with the reference frame rotating at the fundamental frequency ω_1:

$$v_{Sdq} = T^{dq}_{abc}\, v_{Sabc}, \tag{12}$$

where the transformation matrix is shown in Eq. (13).

$$T^{dq}_{abc} = \frac{2}{3}\begin{bmatrix} sin(\omega_1 t) & sin(\omega_1 t - 120^\circ) & sin(\omega_1 t + 120^\circ) \\ cos(\omega_1 t) & cos(\omega_1 t - 120^\circ) & cos(\omega_1 t + 120^\circ) \end{bmatrix}\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \tag{13}$$

By this transform, the fundamental positivesequence component, which is transformed into DC quantities in the d and q axes, can be extracted by Eq. (14) and then transformed back into the abc reference frame using Eq. (15).

$$\bar{v}_{d,q} = \frac{1}{T_c}\int_{t-T_c}^{t} v_{d,q}\,dt \tag{14}$$

$$v_{abc1+} = T^{abc}_{dq}\,\bar{v}_{d,q}; (T^{abc}_{dq} = {T^{dq}_{abc}}^{-1}) \tag{15}$$

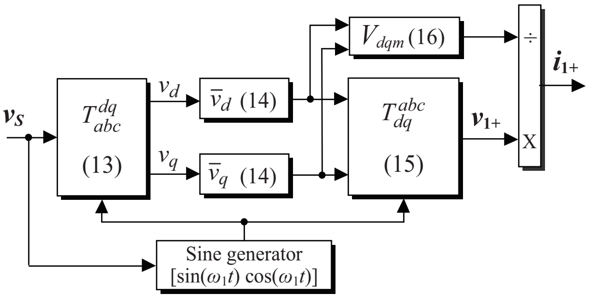
v_S
T^{dq}_{abc} (13)
v_d
v_q
$\bar{v}_d$ (14)
$\bar{v}_q$ (14)
V_{dqm} (16)
T^{abc}_{dq} (15)
v_{1+}
÷
X
i_{1+}
Sine generator [sin($\omega_1 t$) cos($\omega_1 t$)]

Figure 3. Block diagram of the positive-sequence detector.

As shown in Figure 3, $\boldsymbol{v}_{1+}(t)$ is divided by its amplitude, V_{dqm}, using Eq. (16), and the output signals of the positive-sequence detector (i_{a1+}, i_{b1+}, i_{c1+}), having unity amplitude and being in phase with the fundamental positive-sequence component of the source voltages (v_{Sa1+}, v_{Sb1+}, v_{Sc1+}), are obtained. The effective value of reference current $\boldsymbol{i}_p(t)$ is given in Eq. (17).

$$V_{dqm} = \sqrt{\bar{v}_d^2 + \bar{v}_q^2} \tag{16}$$

$$I_p(t) = \sqrt{\frac{1}{T_c} \int_{t-T_c}^{t} i_p^T(\tau)\, i_p(\tau)\, d\tau} \tag{17}$$

The average power is calculated, as given in Eq. (4), by using the reference currents and the source voltages. The sinusoidal load voltage $\boldsymbol{v}_a(t)$ is derived by using Eq. (18) [27]. Figure 4 shows the block diagram of the generalized nonactive power theory that is applied to series AF control. As is clearly shown in Figure 2, $\boldsymbol{v}_a(t)$ is divided by its amplitude, V_{am}, using Eq. (19), and is multiplied by the desired load voltage magnitude, V_{Lm*}, to convert it to the desired load voltage, $\boldsymbol{v}_{S1+}$. The compensation reference voltages (v_{SFa*}, v_{SFb*}, v_{SFc*}) of the series AF are then derived by Eq. (20) and compared with the series AF voltages. Thus, the series AF switching signals Q_{SF} are obtained by using the improved sinusoidal pulsewidth modulation (SPWM) [22].

$$v_a(t) = \frac{P(t)}{I_p^2(t)}\, i_p(t) \tag{18}$$

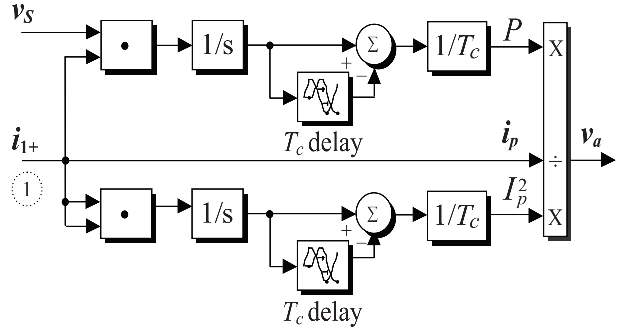

Figure 4. Block diagram of the generalized nonactive power theory.

$$V_{am} = \frac{2}{3}\sqrt{v_{aa}^2 + v_{ab}^2 + v_{ac}^2} \tag{19}$$

$$v_{SF}^*(t) = v_S(t) - v_{S1+}(t) \tag{20}$$

3.2. Current control strategy

The current control block diagram of the parallel AF is shown in Figure 5.

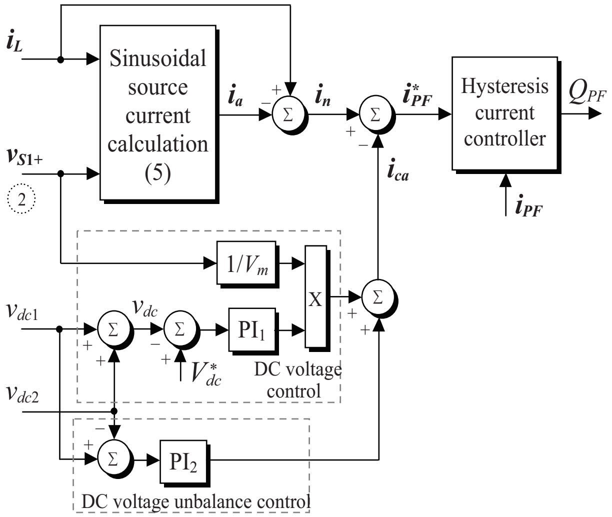

Figure 5. Control block diagram of the parallel AF.

The average power is calculated as given in Eq. (4) by using load currents and fundamental positivesequence source voltages (v_{Sa1+}, v_{Sb1+}, v_{Sc1+}) over the averaging interval $[t - T_c,\ t]$. The desired sinusoidal source currents (i_{La1+}, i_{Lb1+}, i_{Lc1+}) are derived by using Eq. (5) and a similar block diagram as shown in Figure 4. The instantaneous nonactive current $\boldsymbol{i}_n(t)$ is calculated as in Eq. (6).

An additional active current, $\boldsymbol{i}_{ca}(t)$ also required to meet the losses in Eq. (21) is drawn from the source by regulating DC-link voltage v_{dc} to reference voltage V_{dc*}. The PI_1 controller is used to regulate DC-link voltage v_{dc}, as shown in Figure 5. The error between the actual DC voltage and its reference value is treated in the PI_1 controller, and the output is multiplied by a sinusoidal fundamental template of unity amplitude for each phase of the 3 phases. In addition, as shown in Figure 5, the difference between v_{dc1} and v_{dc2} is applied to the PI_2 controller for DC voltage unbalance compensation. Thus, equal voltage sharing between the capacitors is accomplished.

The compensation reference currents (i_{PFa*}, i_{PFb*}, i_{PFc*}) of the parallel AF are obtained by Eq. (22). The reference currents are compared with the parallel AF currents and applied to a hysteresis current controller. Thus, the parallel AF switching signals Q_{PF} are obtained.

$$\begin{aligned} i_{ca}(t) = {} & \left(\tfrac{v_{S1+}}{V_m}\left[K_{P1}\left(V^*_{dc} - v_{dc}\right) + K_{I1}\int_0^t \left(V^*_{dc} - v_{dc}\right) dt\right]\right) \\ & +\left(K_{P2}\left(v_{dc1} - v_{dc2}\right) + K_{I2}\int_0^t \left(v_{dc1} - v_{dc2}\right) dt\right) \end{aligned} \tag{21}$$

$$i^*_{PF}(t) = i_n(t) - i_{ca}(t) \tag{22}$$

4. Simulation and experimental results

The USPAF system prototype was designed and developed in a laboratory to validate the generalized nonactive power theory proposed in this paper. A 3-phase delta-star (Δ-Y) step-down transformer, rated at 380/110 V and 25 kVA, was used to provide 3-phase, 4-wire experimental system voltages. In this system, the line-to-neutral voltage was 110 V and the frequency was 50 Hz. The power circuit and control block diagram of the USPAF system implementation are given in Figures 6 and 7 respectively.

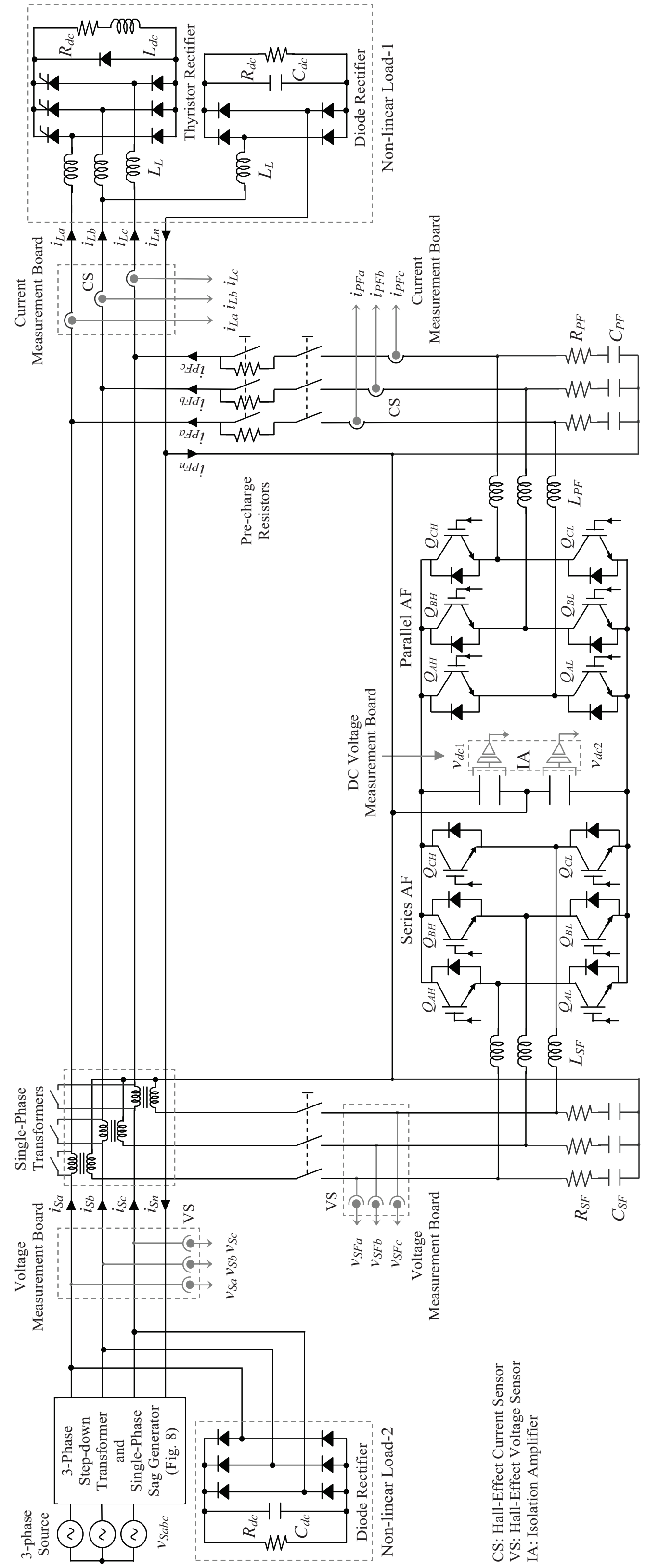
Thyristor Rectifier
Diode Rectifier
Non-linear Load-1
R_{dc}
L_{dc}
C_{dc}
L_L
Current Measurement Board
CS
i_{La}
i_{Lb}
i_{Lc}
i_{Ln}
i_{La} i_{Lb} i_{Lc}
i_{PFa}
i_{PFb}
i_{PFc}
i_{PFn}
Pre-charge Resistors
R_{PF}
C_{PF}
L_{PF}
Parallel AF
Q_{AH}
Q_{BH}
Q_{CH}
Q_{AL}
Q_{BL}
Q_{CL}
DC Voltage Measurement Board
v_{dc1}
v_{dc2}
IA
Series AF
L_{SF}
R_{SF}
C_{SF}
Single-Phase Transformers
Voltage Measurement Board
VS
i_{Sa}
i_{Sb}
i_{Sc}
i_{Sn}
v_{Sa} v_{Sb} v_{Sc}
v_{SFa}
v_{SFb}
v_{SFc}
3-phase Source
v_{Sabc}
3-Phase Step-down Transformer and Single-Phase Sag Generator (Fig. 8)
Non-linear Load-2
CS: Hall-Effect Current Sensor
VS: Hall-Effect Voltage Sensor
IA: Isolation Amplifier

Figure 6. Power circuit block diagram of the USPAF system implementation.

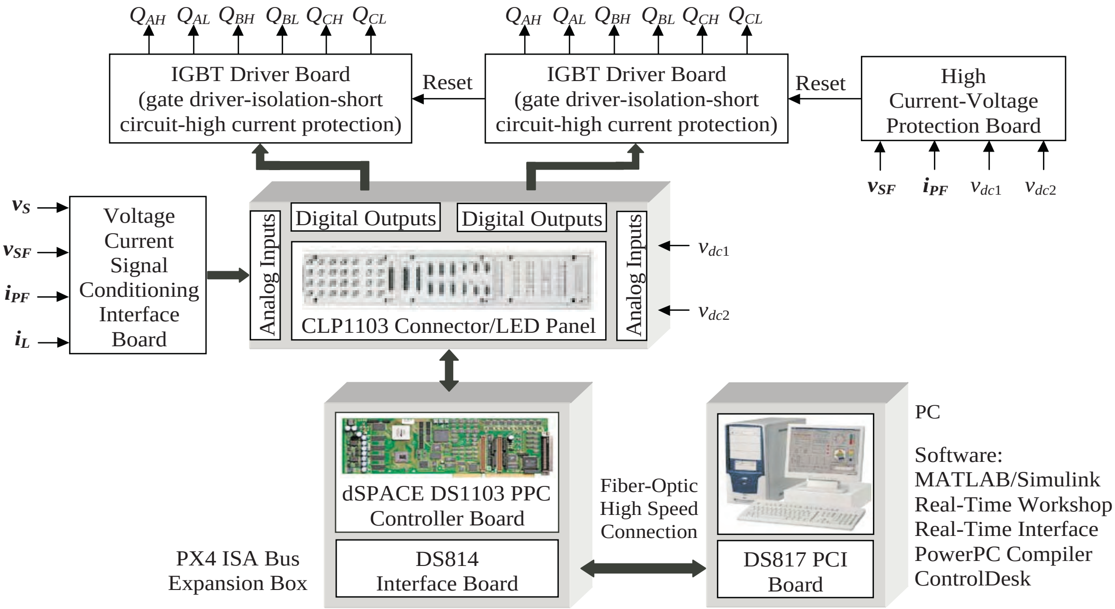
Q_{AH} Q_{AL} Q_{BH} Q_{BL} Q_{CH} Q_{CL}
Q_{AH} Q_{AL} Q_{BH} Q_{BL} Q_{CH} Q_{CL}
IGBT Driver Board (gate driver-isolation-short circuit-high current protection)
Reset
IGBT Driver Board (gate driver-isolation-short circuit-high current protection)
Reset
High Current-Voltage Protection Board
v_{SF} i_{PF} v_{dc1} v_{dc2}
v_S
v_{SF}
i_{PF}
i_L
Voltage Current Signal Conditioning Interface Board
Analog Inputs
Digital Outputs
Digital Outputs
CLP1103 Connector/LED Panel
Analog Inputs
v_{dc1}
v_{dc2}
dSPACE DS1103 PPC Controller Board
DS814 Interface Board
PX4 ISA Bus Expansion Box
Fiber-Optic High Speed Connection
DS817 PCI Board
PC
Software:
MATLAB/Simulink
Real-Time Workshop
Real-Time Interface
PowerPC Compiler
ControlDesk

Figure 7. Control block diagram of the USPAF system implementation.

In Figure 6, nonlinear load-1 (RL loaded 3-phase half-controlled thyristor rectifier with firing angle of 30°, and RC loaded single-phase diode rectifier) is the load group that requires ideal source voltages. Nonlinear load-2 (RC loaded 3-phase diode rectifier) is connected to the PCC to create source voltage distortion and resembles the effect of other loads on a radial network. The 3-phase source voltages with distortion were synthesized by increasing the system impedance from 59 μH to 4 mH and connecting nonlinear load-2 to the PCC, as is clearly shown in Figure 6. The voltage sag generator was employed to simulate the single-phase source voltage sag for phase-a in the laboratory, as shown in Figure 8. The 3-phase step-down transformer was also used to test the experimental single-phase voltage sag problem.

The USPAF system has a 3-phase, 4-wire power circuit configuration based on the 3-leg VSI with a split DC-link capacitor. The DC-link includes 2 capacitors with the midpoint connected to the neutral wire of the supply system. The DC-link voltage is adjusted at 400 V. The parallel AF is connected in parallel with the load while the series AF is connected in series with the utility and the load through 3 single-phase series injection transformers.

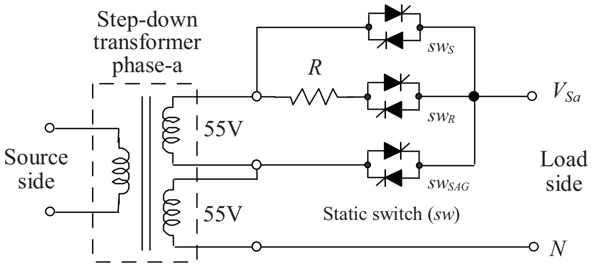
Step-down transformer phase-a
R
sw_S
sw_R
sw_{SAG}
V_{Sa}
Source side
55V
55V
Static switch (sw)
Load side
N

Figure 8. Power circuit of the single-phase voltage sag generator.

Both AFs are digitally controlled using a dSPACE DS1103 controller board. The dSPACE controller board includes a real-time processor and the necessary I/O interfaces to allow the carrying out of the control operation. This hardware supports the real-time interface (RTI) tool that allows programming via MAT-

LAB/Simulink. In this way, all of the control circuit components are implemented graphically within the Simulink environment.

In the USPAF system, the load currents and parallel AF currents are measured by utilizing TEG NA-50P Hall-effect current sensors, the source voltages and series AF voltages are measured by utilizing TEG NV-25P Hall-effect based isolated voltage sensors, and DC bus voltages are measured with an AD210 isolation amplifier for control and protection purposes. All of the measured signals are scaled in the signal conditioning board, which provides the measured signals at the required voltage level for the dSPACE ADC unit. The parallel VSI uses the variable frequency hysteresis current controller. The series VSI uses an improved triangular carrier signal-based fixed switching frequency PWM controller. The proposed algorithm for USPAF system requires a sampling time of 20 μs to execute the MATLAB/Simulink generated C-codes in real time. The generated switching signals are taken out of the DS1103 with the help of digital I/O channels.

The 2 3-leg VSIs of the USPAF system consist of 6 SEMIKRON SKM75GB128D dual-pack IGBT modules, which are driven by CONCEPT 6SD106EI gate drivers. The gate drivers have an analog dead-time generation facility and also monitor the collector-emitter voltage for short-circuit failure conditions. The DC-link capacitance rating is proportional to the maximum energy storage variation of the capacitor. The energy exchange is different for a given DC-link voltage variation in a particular application [20]. Different capacitance values are required to meet different compensation cases. Under periodic conditions, because the instantaneous nonactive power is zero at all times, the current flowing into or out of the DC-link capacitor is zero. Therefore, a small capacitor can meet the requirements of this case. Under nonperiodic conditions, average power $P(t)$ is time-varying. The net energy flowing into the DC-link capacitor is no longer zero over one cycle. The capacitor must have sufficient storage capacity under these conditions to be able to absorb the load power fluctuations. In the USPAF system design presented, the necessary DC-link capacitor size was determined through MATLAB/Simulink simulations. To form the split DC-link of the USPAF system, 2 electrolytic capacitors (4700 μF, 450 V) were connected in series.

The parallel AF currents and series AF voltages are also utilized in the overcurrent and overvoltage protection board. If a fault occurs, all IGBT gate signals are set to zero-level so that the 2 VSIs are disabled. Owing to the switching of the parallel and series VSIs, the compensating currents and voltages have unwanted high-order harmonics. High-pass passive filters, represented by R_{PF} andC_{PF} for parallel AF and R_{SF} andC_{SF} for series AF in Figure 6, are connected to prevent the flow of switching harmonics into the PCC. Coupling inductances L_{PF} and L_{SF} are necessary to limit *di/dt* in the VSIs. The coupling inductance was chosen so that the fundamental voltage drop on this inductor is 3%-9% of system voltage V_s [20]. Precharge resistors are also utilized at the AC side of the parallel AF to limit the inrush current during the startup and are bypassed after the DC-link capacitors are charged to their steady-state value.

The experimental waveforms were recorded with a Tektronix DPO3054 digital oscilloscope, and the harmonic analyses were done with a Fluke 434 power quality analyzer. Figure 9 shows the photographs of the USPAF system laboratory prototype. Table 1 shows the circuit parameters used in the simulation and experiment.

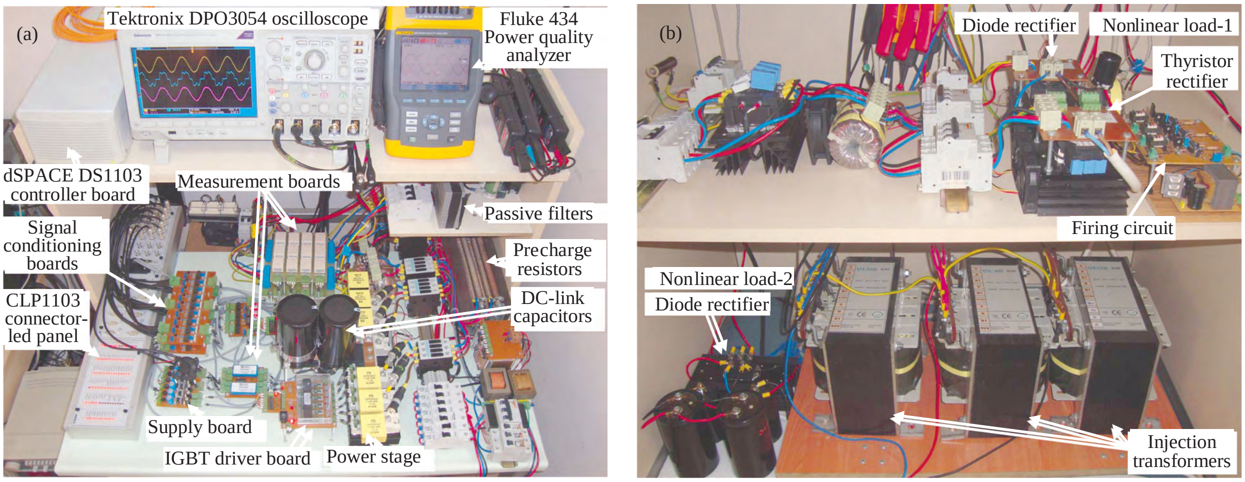
(a)
Tektronix DPO3054 oscilloscope
Fluke 434
Power quality
analyzer
dSPACE DS1103
controller board
Measurement boards
Passive filters
Signal
conditioning
boards
Precharge
resistors
DC-link
capacitors
CLP1103
connector-
led panel
Supply board
IGBT driver board
Power stage
(b)
Diode rectifier
Nonlinear load-1
Thyristor
rectifier
Firing circuit
Nonlinear load-2
Diode rectifier
Injection
transformers

Figure 9. Photographs of the experimental test setup: a) top view of the experiment desk, b) bottom view of the experiment desk.

Table 1. The USPAF system parameters.

Components	Symbol	Parameters
Power source		
Voltage, frequency	V_{Sabc},f_s	110 V, 50 Hz
Impedance	L_S	59 μH
DC-link		
Capacitors	C_{dc1},C_{dc2}	4700 μF, 4700 μF
Reference voltage	V_{dc*}	400 V
Parallel AF		
Filter	L_{PF}, R_{PF},C_{PF}	2.5 mH, 5 Ω, 30 μF
Switching frequency	f_{SWp}	10 kHz
Series AF		
Filter	L_{SF},R_{SF},C_{SF}	2.5 mH, 2 Ω, 150 μF
Switching frequency	f_{SWs}	10 kHz
Injection transformer	N_1/N_2, S	2, 5.4 kVA
Nonlinear loads		
3-phase thyristor rectifier	L_L, L_{dc}, R_{dc}	3 mH, 5.6 mH, 12 Ω
1-phase diode rectifier	L_L, C_{dc}, R_{dc}	3 mH, 330 μF, 45 Ω
3-phase diode rectifier	C_{dc}, R_{dc}	8800 μF, 15 Ω

The USPAF nonactive power compensation system was simulated, and an experimental setup was also built, so that different cases could be studied in simulations or experiments. The first 2 cases for periodic current and voltage compensation (Section 4.1 and 4.2) were tested in the experimental setup, and the last 2 cases (Sections 4.3 and 4.4) were simulated with MATLAB/Simulink software since they were difficult to carry out in an experimental setup. The IEEE-519 standard limit of 5% THD in voltage or current was set on the THD of the source currents and load voltages after compensation.

4.1. Distorted source voltage and unbalanced nonlinear load current compensation

The nonlinear loads on the electric power system draw highly distorted currents, resulting in voltage distortions that can affect the other loads. For compensation of the periodic current and voltage with fundamental period T, using a compensation period T_c that is a multiple of $T/2$ is enough for complete compensation [19]. The 3-phase distorted load voltages before compensation are demonstrated in Figure 10a. After compensation with a period of $T_c = T/2$, the source voltages with distortion were compensated to the sinusoidal waveforms shown in Figure 10b. The THD of the load voltages, which was approximately 9.7% before compensation, was about 4.4% after compensation, which is well within the limits specified by IEEE-519.

Shown in Figure 10c, from top to bottom, are the phase-a source voltage, injected voltage, compensated load voltage, and DC-link voltage. By means of the parallel AF current compensation, the THD values of the source voltages were approximately decreased from 9.7% to 6.8%. After the series AF compensation, the load voltage THD values were decreased to about 4.4%.

The unbalanced nonlinear source currents before compensation are presented in Figure 10d. After compensation, choosing the period as $T_c = T/2$, it was evident that the source currents were nearly sinusoidal with constant amplitude, as is shown in Figure 10e. Moreover, the neutral line current was almost eliminated. The THD of the source currents, which was 27.9% before compensation, was 4.9% after compensation.

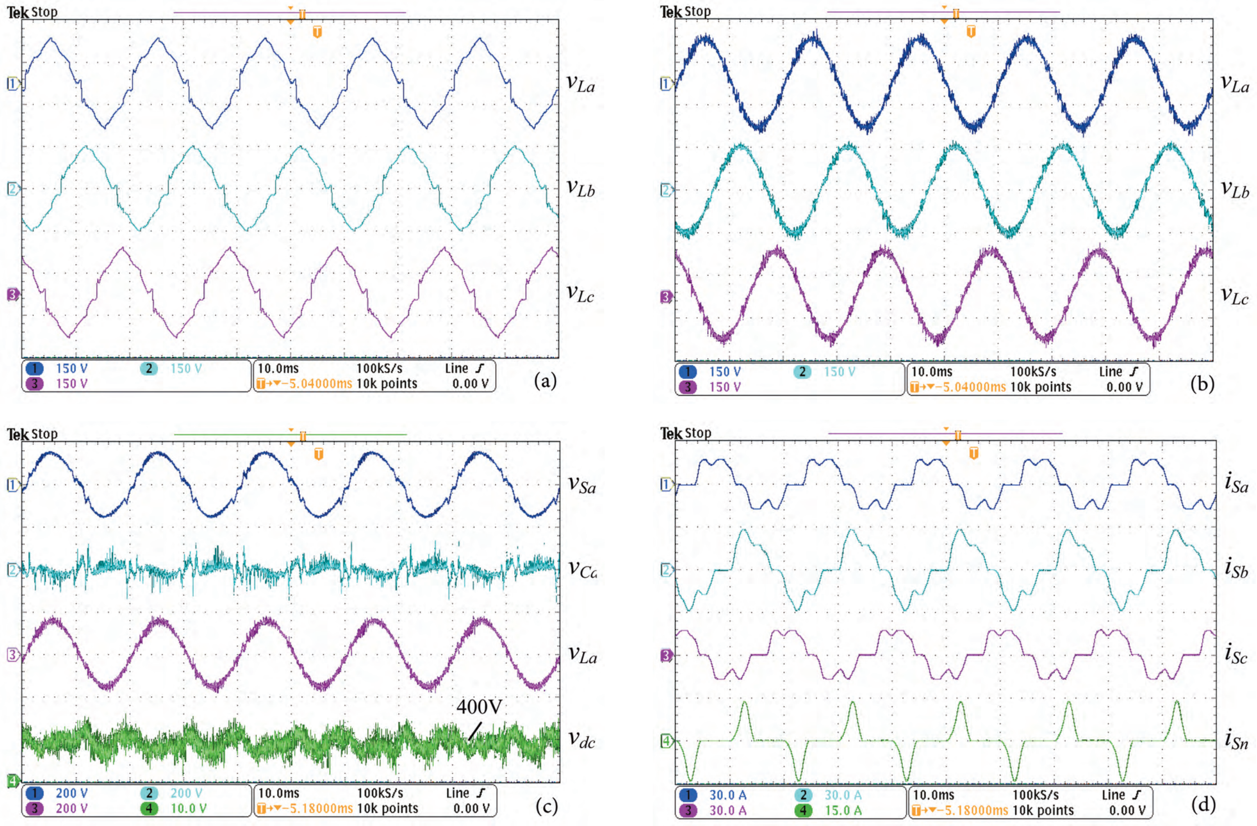

Figure 10. Experimental results with distorted source voltage and unbalanced nonlinear load current compensation: a) load voltages before compensation; b) load voltages after compensation; c) source, series AF, load, and DC voltage waveforms; d) source currents before compensation; e) source currents after compensation.

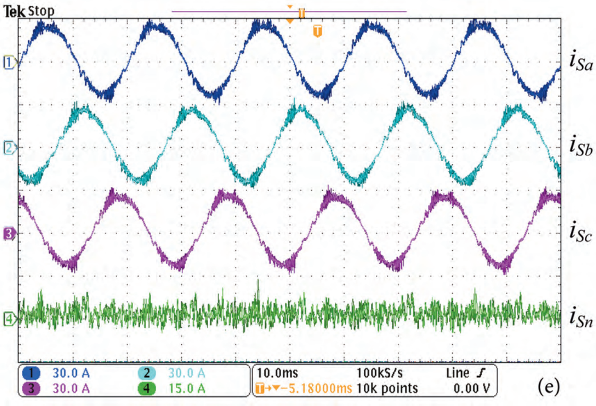

Figure 10. Contunied.

The harmonic spectra of the phase-a source current before and after compensation are shown in Figures 11a and 11b, respectively. The harmonic spectra of the phase-a load voltage before and after compensation are shown in Figures 12a and 12b, respectively. The compensation results are summarized in Tables 2 and 3.

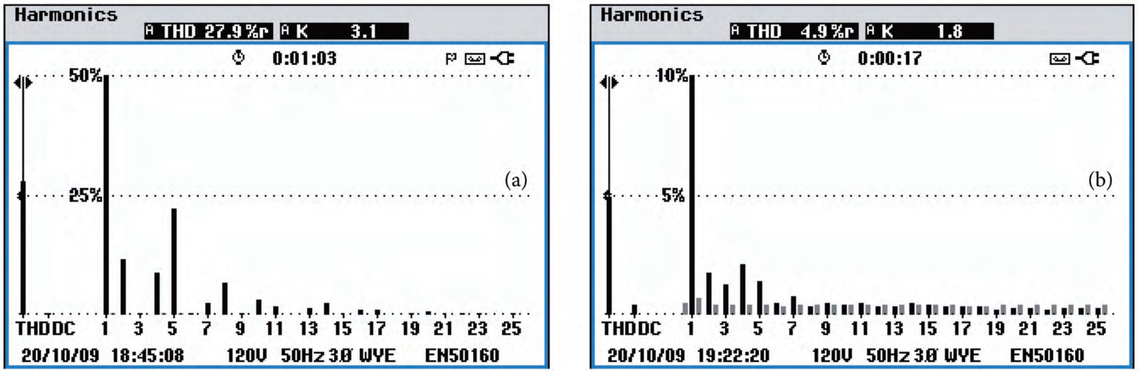

Figure 11. Harmonic spectra of phase-a source current: a) before compensation, b) after compensation.

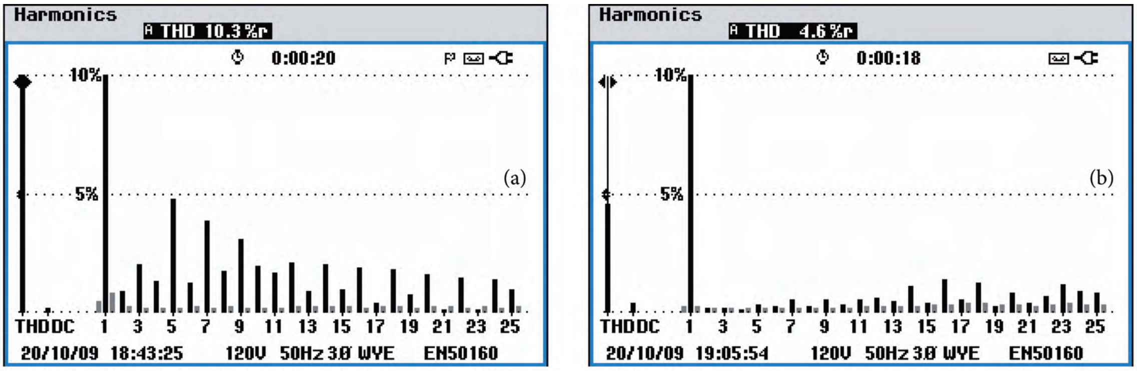

Figure 12. Harmonic spectra of phase-a load voltage: a) before compensation, b) after compensation.

4.2. Source voltage sag and unbalanced nonlinear load current compensation

Voltage sags are the most common power disturbance and are typically caused by remote faults, such as a single line-to-ground fault in the power system, or are due to the starting of large electric motors. Figure 13 shows the experimental waveforms under a single-phase voltage sag with a depth of 50% and a period of $T_c = T/2$. Shown in Figure 13a, from top to bottom, are the phase-a source voltage, injected voltage, compensated load voltage, and DC-link voltage. During the single-phase 50% voltage sag condition, the series AF provides the required power of the load by injecting in-phase compensating voltage v_{Ca} equal to the difference between the reference load voltage and source voltage, as shown in Figure 13a. The load terminal voltage is regulated and at an almost constant nominal value during the voltage sag of phase-a. Additionally, shown in Figure 13b, from top to bottom, are the phase-a source voltage, compensated load voltage, load current, and compensated source current.

Table 2. Summary of the distorted source voltage compensation.

Load voltage ($\boldsymbol{v}_L$)	Before compensation	After compensation
RMS (V)		
phase-a	103.3	110.4
phase-b	102.4	109.5
phase-c	103.6	109.9
THD (%)		
phase-a	10.3	4.6
phase-b	9.1	4.5
phase-c	9.8	4.3

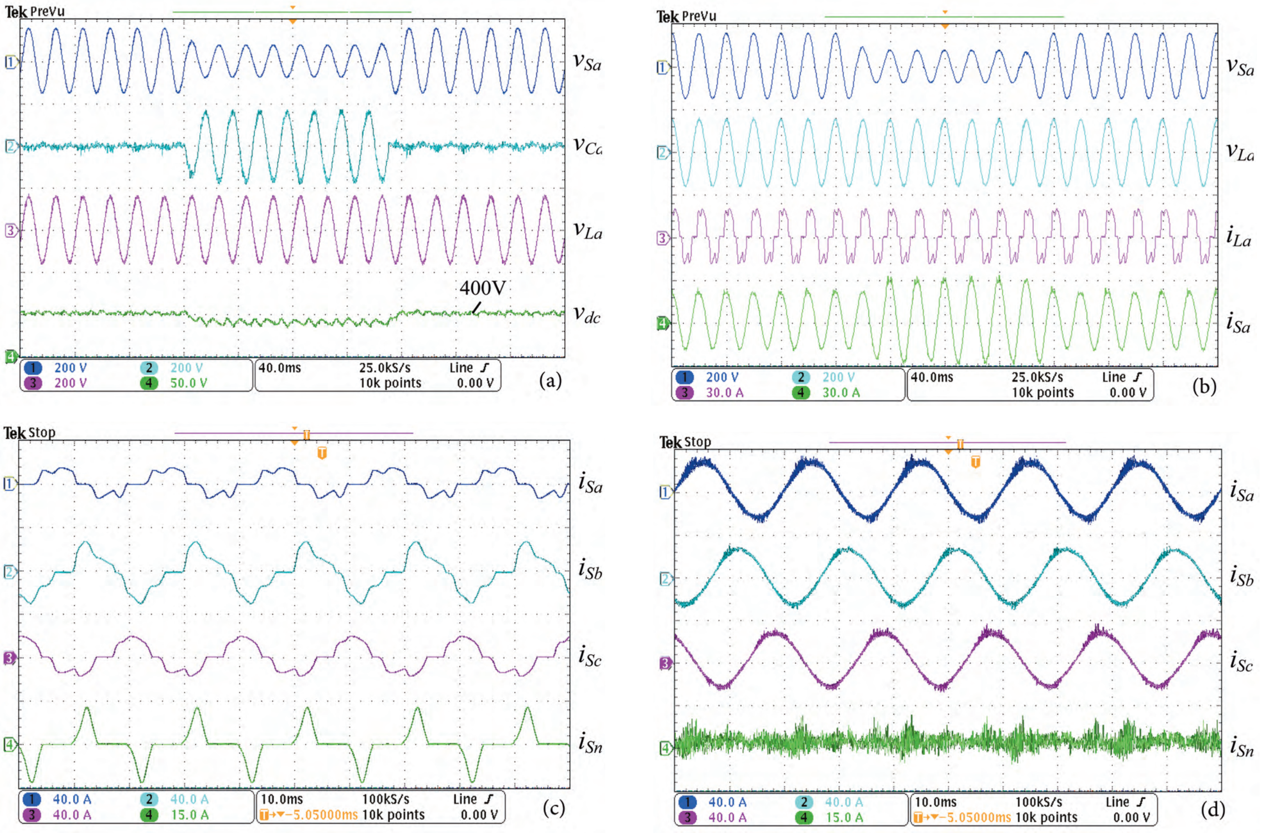

Figure 13. Experimental results with source voltage sag and unbalanced nonlinear load current compensation: a) source, series AF, load, and DC voltage waveforms; b) source, load voltage and load, and source current waveforms; c) source currents before compensation; d) source currents after compensation.

In the voltage sag compensation case, the energy storage requirement will be very high, so large capacitor banks required. External energy sources should be used to meet such requirements. But, as is clearly shown in this study, the required load power for the compensation of the load voltage is supplied from the source only, by delivering more current. While the series AF is providing the required real power to the load, the parallel AF is maintaining the DC-link voltage at the desired level. In order to maintain the DC-link voltage at a constant level, the source delivers more current. Source current i_{Sa} was increased, as shown in Figure 13b. This extra power flowed from the source to the parallel AF, the parallel AF to the series AF via the DC-link, and from the series AF to the load.

Table 3. Summary of the load current compensation.

Source current ($\boldsymbol{i}_S$)	Before compensation	After compensation
RMS (A)		
phase-a	11.6	16.5
phase-b	15.3	16.6
phase-c	11.6	16.3
neutral	5.2	2.3
THD (%)		
phase-a	27.9	4.9
phase-b	29.6	4.6
phase-c	27.9	4.7
Unbalance (%)		
neg. seq.	9.5	0.9
zero seq.	10.2	1.5
PF	0.86	0.99

The unbalanced nonlinear source currents before compensation are shown in Figure 13c. The source currents were forced to be approximately balanced by choosing the period $T_c = T/2$. It can be noticed from Figure 13d that the source currents were nearly sinusoidal and balanced. Moreover, the neutral line current was obviously diminished. The harmonic spectra of the phase-a source current before and after compensation are presented in Figures 14a and 14b, respectively. The compensation results are summarized in Tables 4 and 5.

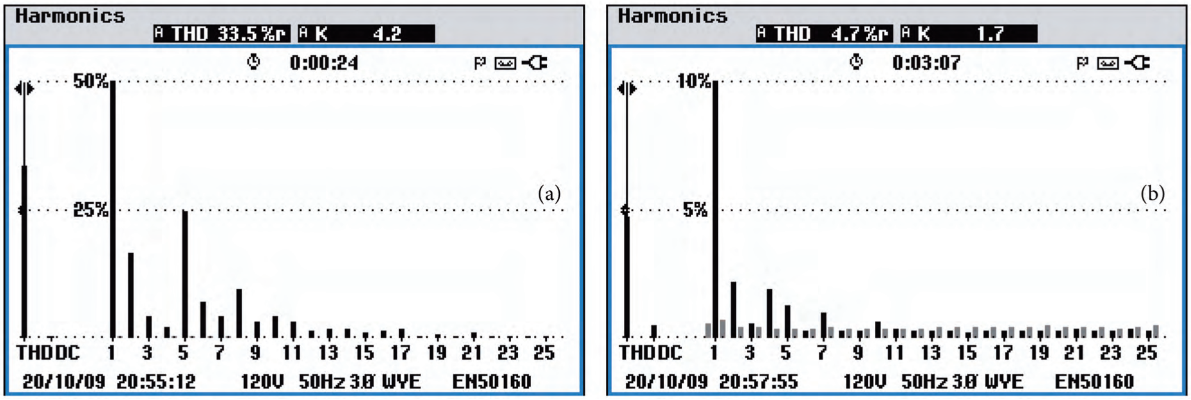

Figure 14. Harmonic spectra of phase-a source current: a) before compensation, b) after compensation.

Table 4. Summary of the single-phase voltage sag compensation.

Load voltages ($\boldsymbol{v}_L$)	Before compensation	After compensation
RMS (V)		
phase-a	54.7	110.2
phase-b	110.4	110.5
phase-c	111.0	108.2
Unbalance (%)		
neg. seq.	20.0	1.2
zero seq.	20.6	0.3

Table 5. Summary of the load current compensation.

Source currents ($\boldsymbol{i}_S$)	Before compensation	After compensation
RMS (A)		
phase-a	8.3	17.8
phase-b	15.2	17.5
phase-c	11.6	17.3
neutral	5.1	1.9
THD (%)		
phase-a	33.5	4.7
phase-b	31.4	3.9
phase-c	25.6	4.9
Unbalance (%)		
neg. seq.	26.5	1.0
zero seq.	11.8	0.5
PF	0.86	0.99

4.3. Subharmonic current and voltage compensation

The subharmonic currents (frequency lower than fundamental frequency) are typically generated by power electronic converters [19]. The main feature of these nonperiodic currents is that they may have a repetitive period. When the fundamental frequency of the source voltage is an odd multiple of the subharmonic frequency, the minimum T_c for complete compensation is 1/2 of the common period of both f_s and f_{sub}. When the f_s values are an even multiple of f_{sub}, the minimum T_c for complete compensation is the common period of both f_s and f_{sub} [20]. If T_c is chosen as an integral multiple of the periods of all frequencies in $p(t)$, the average value $P(t)$ is a constant. Therefore, $\boldsymbol{i}_a(t)$ is purely sinusoidal and in phase with the fundamental component of $v(t)$. If T_c is not chosen this way, there will still be subharmonic components in $\boldsymbol{i}_a(t)$ and the nonactive component will not be completely eliminated.

In this study, the source voltage and load current containing subharmonic properties of 10 Hz frequency and 20% amplitude are given by Eqs. (23) and (24) for phase-a. Figure 15 shows the subharmonic current and voltage compensation simulation results. The positive sequence detector output waveforms for this test case are shown in Figure 15b.

$$v_{Sa} = (155 + 15.5sin(2\pi 10t))sin(2\pi 50t) \tag{23}$$

$$i_{La} = (21 + 2.1sin(2\pi 10t))sin(2\pi 50t) \tag{24}$$

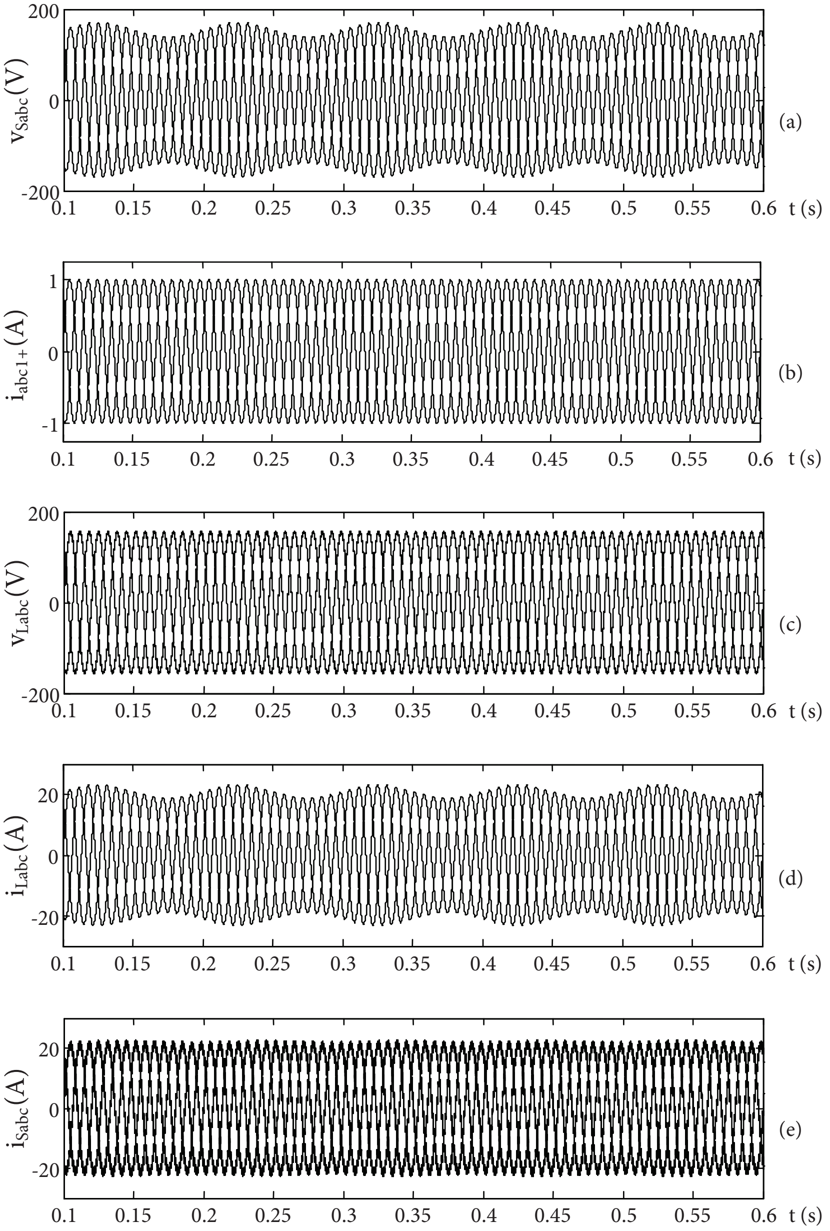

Figure 15. Simulation results with subharmonic voltage and current compensation: a) 3-phase subharmonic source voltage waveforms, b) positive-sequence detector output waveforms, c) 3-phase load voltages after compensation, d) 3-phase subharmonic load current waveforms, e) 3-phase source currents after compensation.

The subharmonic component can be completely compensated by choosing $T_c = 2.5T$. The USPAF system is able to compensate for the subharmonic component of the load current, and the voltage at the load terminals is almost free of subharmonics and has a constant amplitude.

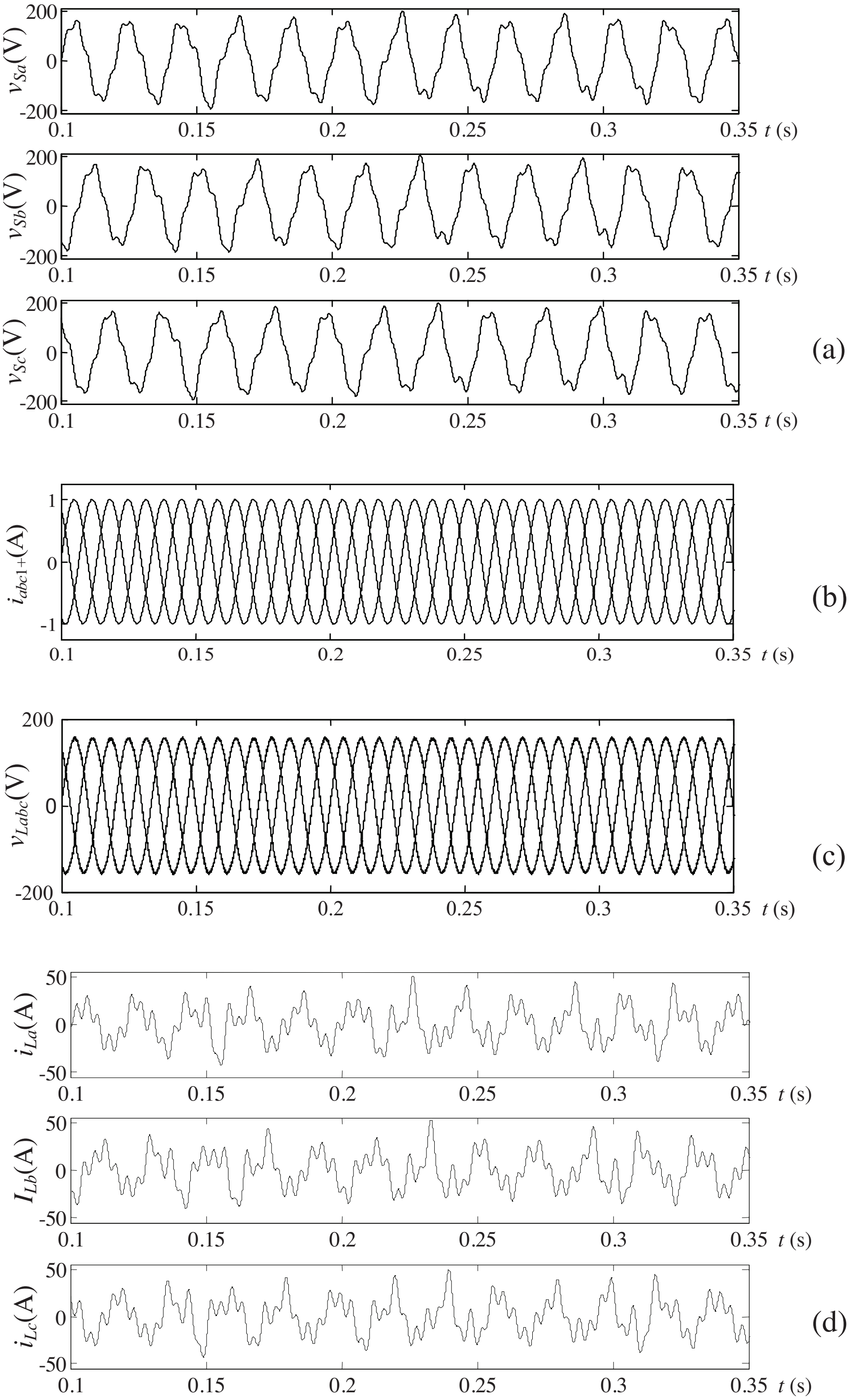

Figure 16. Simulation results with stochastic nonperiodic voltage and current compensation: a) 3-phase stochastic nonperiodic source voltage waveforms, b) positive-sequence detector output waveforms, c) 3-phase load voltages after compensation, d) 3-phase stochastic nonperiodic load current waveforms, e) 3-phase source currents after compensation, f) load neutral current waveforms, g) source neutral current after compensation.

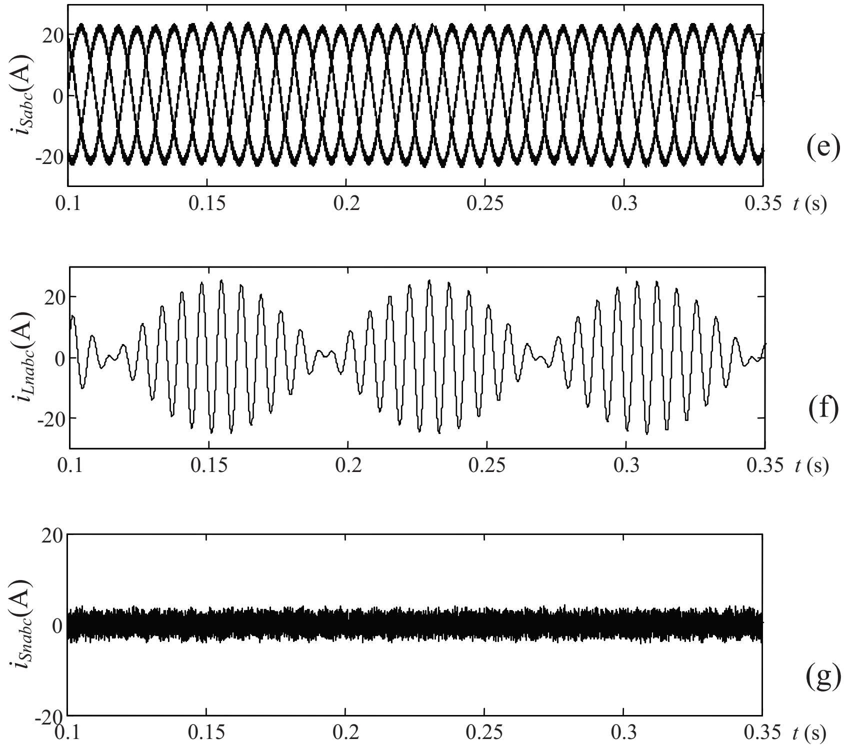

Figure 16. Continued.

4.4. Stochastic nonperiodic current and voltage compensation

The arc furnace load currents may contain stochastic nonperiodic currents (frequency higher than fundamental frequency but not an integer multiple of it) [19,28] Theoretically, the period T of a nonperiodic load is infinite [19]. The generalized nonactive power theory is valid for the voltage and current of any wave shape, and the nonactive current can only be completely eliminated when $T_c = t$ and $t \to \infty$ ($\boldsymbol{i}_a(t)$ is the same shape as and in phase with $\boldsymbol{v}_p(t)$ so that the unity power factor is achieved). However, this is not practical in a power system, and T_c is chosen to have a finite value (1-10 times that of the fundamental period). Additionally, the nonactive components in these loads cannot be completely compensated by choosing T_c as $T/2$ or T, or even several multiples of T. Choosing that period may result in both an acceptable source current and load voltage that are quite close to a sine wave. If T_c is large enough, increasing T_c further will not typically improve the compensation results significantly [20]. In this work, the phase-a source voltage and load current components are given by Eqs. (25) and (26) [28].

$$\begin{aligned} v_{Sa} &= 155sin(2\pi 50t) + 11.6sin(2\pi 104t - 120°) \\ &\quad +15.5sin(2\pi 117t - 120°) + 7.7sin(2\pi 134t) \\ &\quad +7.7sin(2\pi 147t) + 31sin(2\pi 250t - 120°) \end{aligned} \tag{25}$$

$$\begin{aligned} i_{La} &= 21sin(2\pi 50t) + 6.3sin(2\pi 104t - 120°) \\ &\quad +8.4sin(2\pi 117t - 120°) + 4.2sin(2\pi 134t) \\ &\quad +4.2sin(2\pi 147t) + 10.5sin(2\pi 250t - 120°) \end{aligned} \tag{26}$$

Figure 16 shows the stochastic nonperiodic voltage and current compensation with a period of $T_c = 5T$. The positive-sequence detector output waveforms from this test case are shown in Figure 16b.

After compensation, the load voltages and source currents were balanced and almost sinusoidal, with low THD, as clearly shown in Figures 16c and 16e. In addition, the source neutral current was reduced considerably, as presented in Figure 16g.

5. Conclusion

The increasing applications of nonlinear, disturbing loads connected to the electrical power system are responsible for the presence of periodic and nonperiodic disturbances in the line currents and voltages. In this paper, the generalized nonactive power theory, which is applicable to sinusoidal or nonsinusoidal, periodic or nonperiodic, and balanced or unbalanced electrical systems, was presented. It was applied to a 3-phase, 4-wire USPAF system. This theory was adapted to different compensation objectives by changing the averaging interval, T_c. The USPAF experimental setup system was built and tested in the laboratory. A dSPACE DS1103 controller was used to implement the proposed approach in real time. Two cases, distorted source voltage and source voltage sag with unbalanced nonlinear load current compensations, were tested in the experiments. The subharmonic and the stochastic nonperiodic current and voltage compensations were simulated in MATLAB/Simulink. The simulation and experimental results showed that the theory proposed in the USPAF system was applicable to nonactive power compensation in 3-phase, 4-wire systems for periodic and nonperiodic disturbances.

Acknowledgements

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