A new, improved CMOS realization of CDTA and its filter applications

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Abstract

This paper presents a high-performance current differencing transconductance amplifier (CDTA), a recently reported active element, especially suitable for analog signal processing applications. A high linearity CMOS configuration for a CDTA is made up of high linearity input and output stages. The proposed CDTA provides high output impedance at port X and excellent input/output current tracking. A biquad filter circuit was chosen as an application example in order to demonstrate the performance of the CDTA. PSpice simulation results using a TSMC 0.35-μm CMOS process model were included to verify the expected values.

1. Introduction

Circuits based on the current-mode approach [1-3], such as current conveyors [4-6], current amplifiers [7,8], and operational transconductance amplifiers [9,10], seem to have a better signal dynamic range and closed-loop bandwidth performance than conventional voltage amplifiers [11,12]. Moreover, they are particularly suitable whenever the input sources and/or the outputs are current signals [13,14]. Great interest has been devoted to the analysis and design of the current differencing transconductance amplifier proposed by Biolek [15,16], mainly because it exhibits better performance, particularly higher speed and better bandwidth, than classic voltage mode operational amplifiers, which are limited by a constant gain-bandwidth product [17,18].

This device, with 2 current inputs and 2 kinds of current output, provides an easy implementation of current-mode active filters. A CDTA is a synthesis of the well-known advantages of the current differencing amplifier and a transconductance amplifier to facilitate the implementation of current-mode active filters [19-26].

The main features of a CDTA are low gain errors (high accuracy), high linearity, high transconductance, and wide frequency response. In addition, high output resistance at terminal X of the CDTA is required

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to enable easy cascading without the need for additional active elements in applications. The conventional CDTA structure available in the literature [17] employs a well-known current differencing amplifier followed by a standard transconductor. As a result, the overall performance of this circuit differs strongly from the expected active element characteristics. The circuit exhibits low output resistance and limited linearity range, which causes deviations in the expected performance of the application circuits employing the CDTA.

There are several works available in the literature on extending the performance of current-mode active elements, including operational transconductance amplifiers (OTAs) and second generation current conveyors (CCIIs), where input stages with a wide linearity range and output stages providing high output impedance are necessary [27-33]. However, good linearity, high accuracy, and high output resistance can be obtained by using high performance current mirrors and adequate input stages in the structure of the CDTA.

The aim of this paper is to introduce a new, improved CMOS configuration of a CDTA providing low input impedances at ports p and n, very high output impedances at ports z and x, an extended linearity range, and high transconductance. To provide high output impedance values, cascode current mirrors and regulated cascode current mirrors were used in the CDTA structure. Furthermore, the input linearity range of the transconductor section was increased by introducing a cross-coupled quad configuration. To demonstrate the performance of the CDTA circuit, a biquad filter was chosen. The next sections include the PSpice simulations of the CDTA device characteristics, and the filter characteristics. The simulations showed that the proposed CDTA circuit exhibits a very good performance and that the results obtained for the filter are in good agreement with the theory.

2. Current differencing transconductance amplifier (CDTA)

A CDTA consists of an input current differencer and a dual output transconductance stage. The input stage takes the difference of input signals and transfers this difference current to the intermediate z terminal, where this current is converted to voltage via an external impedance.

A CDTA is a 5-terminal current-mode active building block [16]. It can be also considered as a current operational amplifier, as in Figure 1, and the defining equations matrix is given in Eq. (1).

$$
\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix}
\tag{1}
$$

Considering the deviation of the voltage and current gains from their ideal values, the defining equation of the CDTA in Figure 1b becomes:

$$
\begin{bmatrix} V_p \\ V_n \\ I_z \\ I_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ \alpha_p & -\alpha_n & 0 & 0 \\ 0 & 0 & 0 & \pm g_m \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ V_x \\ V_z \end{bmatrix},
\tag{2}
$$

where α_p and α_n are current gains, $\alpha_p = 1 - \varepsilon_p$, and $\alpha_n = 1 - \varepsilon_n$. Here, ε_p and ε_n are the current tracking errors, and their absolute values are much less than the unit value.
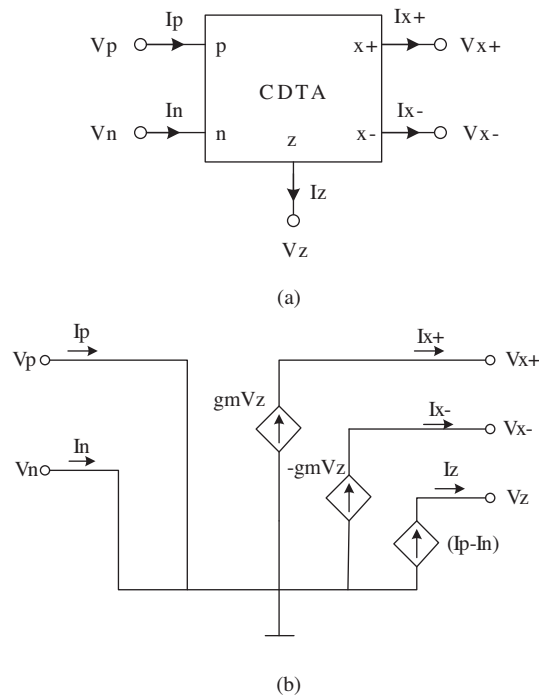
(a)

(b)

Figure 1. The a) circuit symbol and b) equivalent circuit of the CDTA.

The differential input current flows over the z terminal. An external impedance is usually connected to this node and the voltage over this impedance is converted to the output currents by the output transconductors with transconductance g_m for the positive output and -g_m for the negative output.

According to above equation and the circuit of Figure 1, the current through terminal z follows the difference of the currents through the terminals p and n ($i_p - i_n$), and flows from terminal z into impedance Z_z. The voltage drop at terminal z is transferred to a current at terminal x (i_x) by a transconductance gain (g_m), which is electronically controllable by an external bias current [18].

3. CMOS realization of CDTA and simulation results

A CMOS realization of CDTA available in the literature is shown in Figure 2a [17]. The proposed CMOS realization of the CDTA element is shown in Figure 2b. Transistors M1 to M24 form the input differential current-controlled current source (DCCCS) stage, which is used for transforming the differential input current to the intermediate voltage, or the voltage at the z terminal. Transistors M25 to M60 form the high-performance dual-output transconductor stage.

In the literature, some linear transconductance elements have been presented [27-29]. The cross-coupled quad configuration proposed in [29], shown in Figure 3, has superior linearity and input voltage range compared with conventional source-coupled differential pairs. In this circuit, the large-signal i-v transfer characteristic will be given by:

$$i = (n + 1)kIv_1 - (kv_2)4I,$$
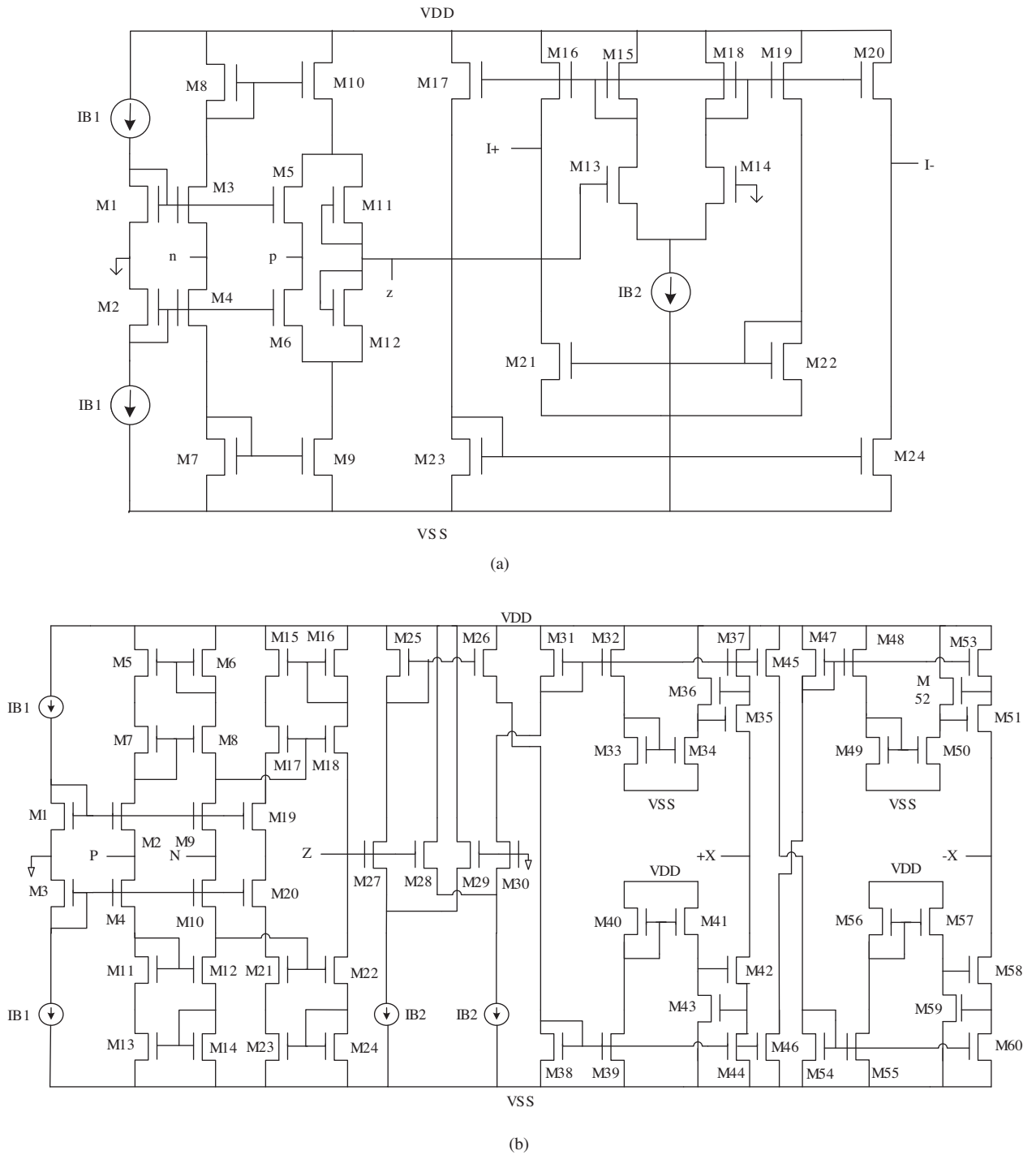$$v \leq (n + 1)Ik$$

$$\tag{3}$$

(a)

(b)

Figure 2. The a) classical [17] and b) proposed CMOS implementation of a CDTA.

This means that the linear region of the input differential voltage v increases by the amount of $(n + 1)/2$. For this purpose, transistors M1, M2, M3, and M4 should be identical in channel length, but M3 and M4 should be made n times wider than M1 and M2.

The high-performance output stage, shown in Figure 4, was proposed in [30]. The 2 complementary current mirrors are composed of transistors M1P-M7P and M1N-M7N. In the regulated-gate-cascode (RGC)

parts [31] of the output stage (transistors M2i, M3i, and M4i for i = P,N), high output impedance is achieved by the negative active-feedback loop along M4i and the source follower M3i. The current mirror M6i-M7i employs the RGC stage to achieve very high output impedance.
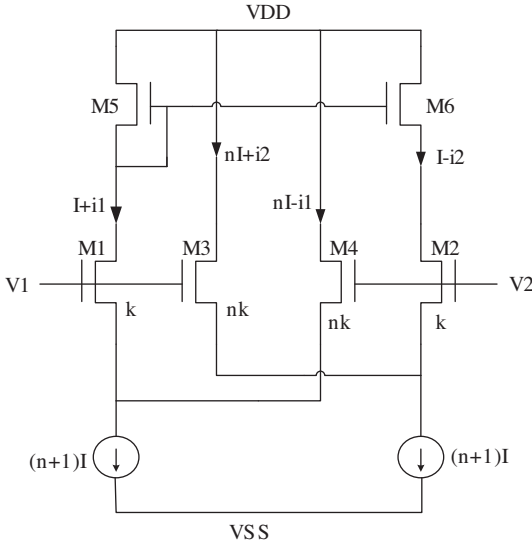

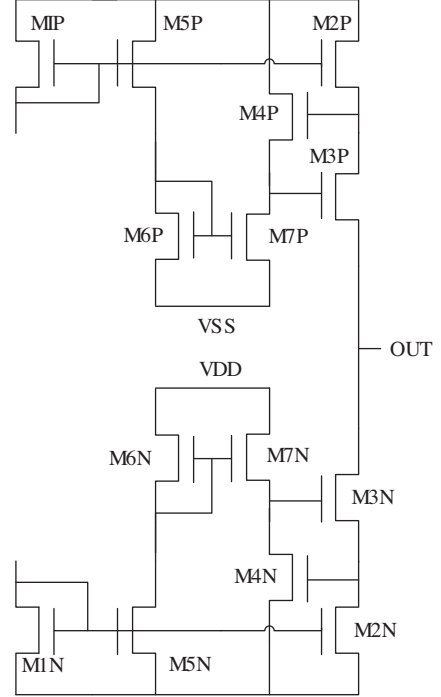**Figure 3.** Circuit realization of the cross-coupled quad configuration proposed in [29].

Figure 4. Circuit realization of the current output stage proposed in [30].

Input resistances of the p and n terminals and output resistance of z, x+, and x- can be calculated approximately using the following equations [4].

$$R_p \cong \frac{1}{(g_{m2} + g_{m4}) + (g_{ds2} + g_{ds4})}$$

$$R_n \cong (r_{ds9}r_{ds8}g_{m9})//(r_{ds10}r_{ds12}g_{m10})$$

$$R_z \cong \frac{1}{(g_{m18} + g_{m22}) + (r_{ds18}//r_{ds22})} \tag{4}$$

$$R_{x-} \cong [g_{m58}g_{m59}r_{ds57}r_{ds60}(r_{ds57}//r_{ds58})]//[g_{m51}g_{m52}r_{ds50}r_{ds53}(r_{ds50}//r_{ds52})]$$

$$R_{x+} \cong [g_{m43}g_{m42}r_{ds41}r_{ds44}(r_{ds41}//r_{ds43})]//[g_{m35}g_{m36}r_{ds34}r_{ds37}(r_{ds34}//r_{ds36})]$$

The performance of the proposed CDTA was verified using the PSpice simulation program. The MOS transistors were simulated using TSMC CMOS 0.35-μm process model parameters. The aspect ratios of the transistors are given in Table 1. The supply voltages and biasing currents are given by $V_{DD} = -V_{SS} = 1.5$ V, $I_{B1} = 100$ μA, and $I_{B2} = 50$ μA, respectively.

Table 1. Transistor aspect ratios for the proposed circuit.

Transistors	W (μm)	L (μm)
M_1, M_2, M_9, M_{19}, M_{39}, M_{43}, M_{55}, M_{59}	0.7	0.7
M_3, M_4, M_{10}	2.8	0.7
M_5-M_8, M_{15}-M_{18}	28	0.7
M_{11}-M_{14}, M_{21}-M_{24}	14	0.7
M_{20}, M_{28}, M_{29}, M_{38}, M_{42}, M_{44}, M_{46}, M_{54}, M_{58}, M_{60}	7	0.7
M_{25}, M_{26}	22.4	0.7
M_{27}, M_{30}	2.8	2.8
M_{31}, M_{35}, M_{37}, M_{45}, M_{47}, M_{51}, M_{53}	21	0.7
M_{32}, M_{36}, M_{48}, M_{52}	2.1	0.7
M_{33}, M_{34}, M_{40}, M_{41}, M_{49}, M_{50}, M_{56}, M_{57}	1.75	0.7

The input terminals' current transfer characteristics are given in Figure 5, obtained when one input is open-circuited. The input stage transfers the difference of the input currents to the z terminal with good accuracy, as demonstrated in the Figures. Since few internal nodes exist over the signal path from the input to the z terminal of the input stage, a high frequency operation is satisfied, exploiting the high frequency capability of current mode signal processing. Figure 6 shows AC responses of the variation of the current at the z terminal with respect to input currents. Variation of the dual output transconductance stage's output currents with respect to the input current is given in Figure 7. The lower and upper boundaries of current Ix for the proposed CDTA were determined as $I_{x\,\max} = 530$ μA and $I_{x\,\min} = 530$ μA for the X terminal.
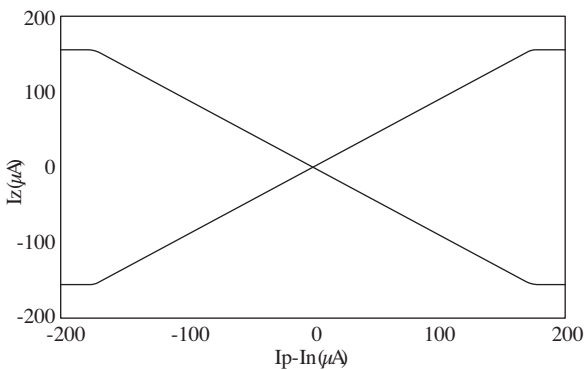

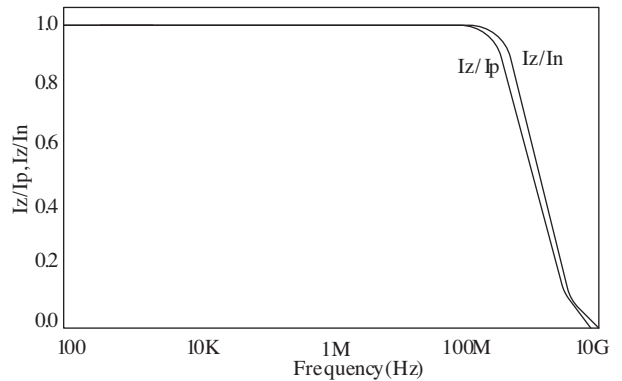**Figure 5.** Current transfer from p and n to z.

Figure 6. Frequency response of I_z/I_p and I_z/I_n.
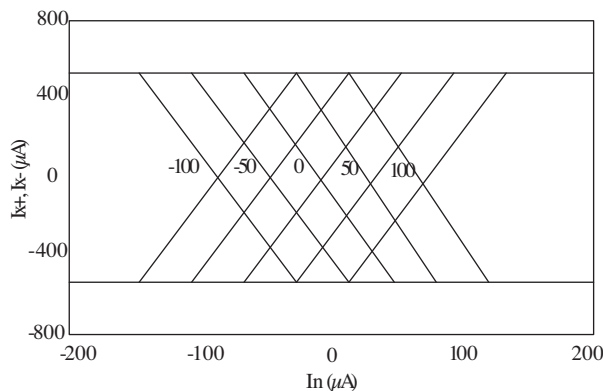

Figure 7. Variation of the z terminal current with respect to input currents (I_P: parametric).

Transconductance of both the positive and negative output is given in Figure 8. The transconductance of the proposed CDTA has a large bandwidth, which makes it suitable for high frequency operations. Transconductance is a very important feature of CDTAs because it directly affects circuit equations. The transconductance for the proposed CDTA is higher than that of classical CDTAs. The frequency responses of the input impedances at terminals n and p and the output impedances z and x are given in Figures 9, 10, and 11, respectively. The output resistances for the proposed CDTA at terminals Z and X± were found to be 1.08 GΩ, 178 GΩ, and 167 GΩ, respectively. It can be seen that at Z and X±, the output resistances for the proposed CDTA are much higher than those of the classical CDTA [17]. The simulation results confirm the high linearity and high performance of the circuit in terms of good input and output resistances and wide bandwidths for both the voltage and current operations. The main performances of the proposed and classical CDTAs are summarized in Table 2, where the improvements provided by the proposed circuit can be easily observed. The p and n terminal input impedances were lower than those of the conventional circuit, the linearity range of the output currents I_{X+} and I_{X-} was extended to twice the amount, and the linearity range of V_Z was extended by the same amount. The output impedance of the X+ and X- terminals increased from the level of several hundred kΩ to the order of the GΩ level. The Z and x terminals' impedances were close to ideal at low frequencies. Although impedances were seen to decrease at high frequencies, they were high enough for these terminals. As a result, the proposed circuit can be assumed to operate with high performance in a wide frequency range. The power consumption is nearly the same for both CDTA circuits.
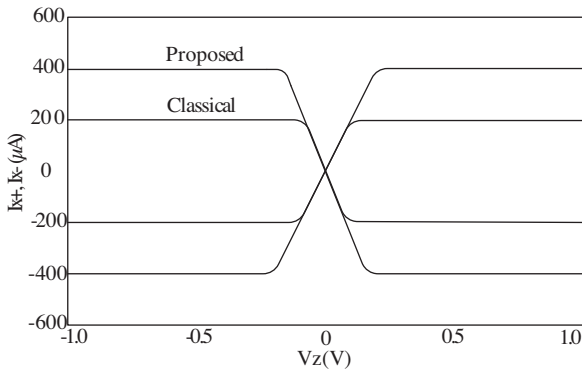

Figure 8. X terminal current with respect to z terminal voltages ($I_{B1} = 100$ μA, $I_{B2} = 50$ μA).
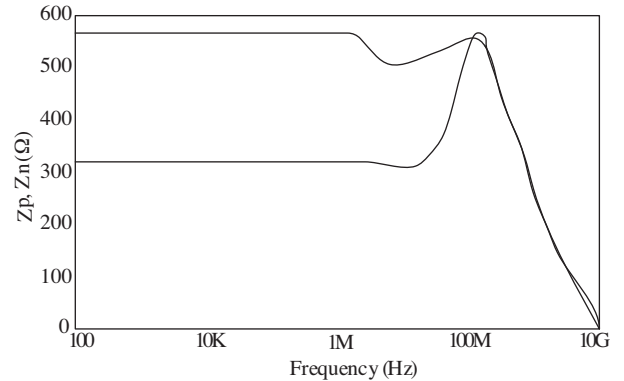

Figure 9. Frequency response of the input impedance at Z_n and Z_p terminals.
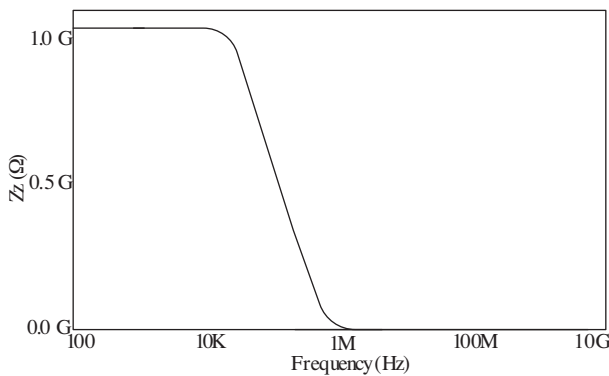

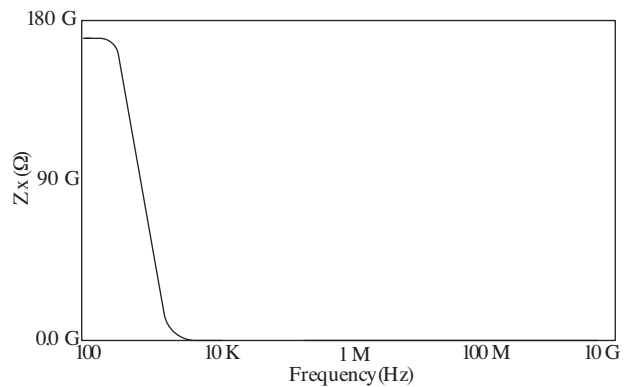**Figure 10.** Frequency response of the impedance at Z_z terminal.

Figure 11. Frequency response of the output impedance at Z_x terminal.

Table 2. Circuit performances of the classical and proposed CDTAs.

	Proposed	Classical
Supply voltages	±1.5 V	±2.5 V
Bias currents	$I_{B1} = 100$ μA, $I_{B2} = 50$ μA	$I_{B1} = 85$ μA, $I_{B2} = 200$ μA
Output current range	-530 μA $\leq I_{O+}$, $I_{O-} \leq +530$ μA	-320 μA $\leq I_{O+}$, $I_{O-} \leq +$ 320 μA
Iz/Ip (−3 dB) bandwidth	609 MHz	632 MHz
Iz/In (−3 dB) bandwidth	462 MHz	483 MHz
Linearity	-424 μA $\leq I_{X+}$, $I_{X-} \leq 412$ μA	-196 μA $\leq I_{X+}$, $I_{X-} \leq 198$ μA
	-240 mV $\leq V_{Z+}$, $V_{Z-} \leq 240$ mV mVA	-160 mV $\leq V_{Z+}$, $V_{Z-} \leq 160$ mV
p input impedance	812 Ω	3.9 kΩ
n input impedance	348 Ω	1.59 kΩ
z output impedance	1.08 MΩ	303 kΩ
x+ output impedance	178 GΩ	211 kΩ
x- output impedance	167 GΩ	268 kΩ
Power consumption	3.61 mW	3.45 mW

4. Biquad filter and simulation results

A biquad filter is a very important filter for analog signal processing. The proposed universal filter, employing current differencing transconductance amplifiers, is shown in Figure 12. Each of the proposed circuits is composed of 2 CDTAs. The configuration uses only 2 capacitors, without any resistors.

The proposed current-mode universal biquad is shown in Figure 13. Circuit analysis yields the following filter current transfer functions:

$$\frac{I_{HP}}{I_{IN}} = \frac{C_1 C_2 s^2}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2}, \tag{5}$$

$$\frac{I_{BP}}{I_{IN}} = \frac{C_2 g_{m1} s}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2}, \tag{6}$$

$$\frac{I_{LP}}{I_{IN}} = \frac{g_{m1} g_{m2}}{g_{m1} g_{m2} + C_2 g_{m1} s + C_1 C_2 s^2}, \tag{7}$$

The pole angular frequency ω_o and quality factor Q are given by:

$$\omega_0 = \sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}}, \tag{8}$$

$$Q = \sqrt{\frac{g_{m2} C_1}{g_{m1} C_2}}. \tag{9}$$

Finally, to verify the theoretical prediction of the proposed biquad filter, a PSpice simulation with a 0.35-μm TSMC process was performed. The CMOS implementation of a CDTA is shown in Figure 2b. The aspect ratios of the MOS transistors are given in Table 1. The supply voltages were taken as ±1.5 V.
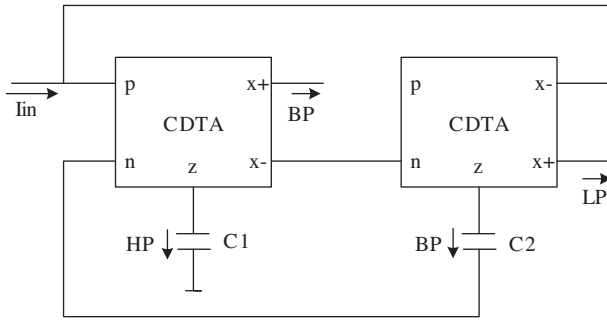
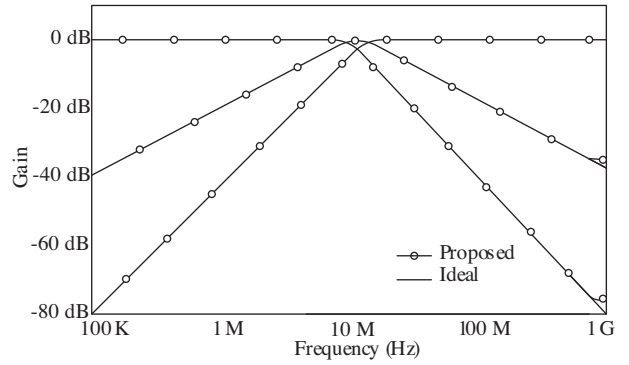**Figure 12.** Proposed biquad filters employing CDTAs.

Figure 13. Frequency response of the proposed biquad filter.

In Figure 12, the current-mode biquad was designed for $f_0 = 10.7$ MHz by choosing $g_{m1} = g_{m2} = 673$ uA/V and $C_1 = C_2 = 1$ pF. Figure 13 shows the simulated and theoretical response of the low-pass, band-pass, and high-pass of Figure 12.

5. Application example and simulation results

The aim was to construct a double-tuned amplifier with band-pass characteristics employing circuits constructed with CDTAs and passive elements. The center frequency f_0 and the bandwidth B were given as $f_0 = 10.7$ MHz and B = 2 MHz, respectively. There are many applications that require narrow bandpass tuned amplifiers such as video signal processing, TV receivers and wireless communications stages. By using the filter topology shown in Figure 12, a fourthorder bandpass filter was implemented which is shown in Figure 14. To obtain a filter with a center frequency of 10.7 MHz and a bandwidth of 4.2 MHz, the pole frequencies and the quality factors of the resonant circuits were chosen as $f_{P1} = 7.59$ MHz, $f_{P2} = 15.9$ MHz, $Q_{P1} = 1$, and $Q_{P2} = 1$, respectively. The simulation result of the filter response is given in Figure 15; it was in very good agreement with the predicted theory.
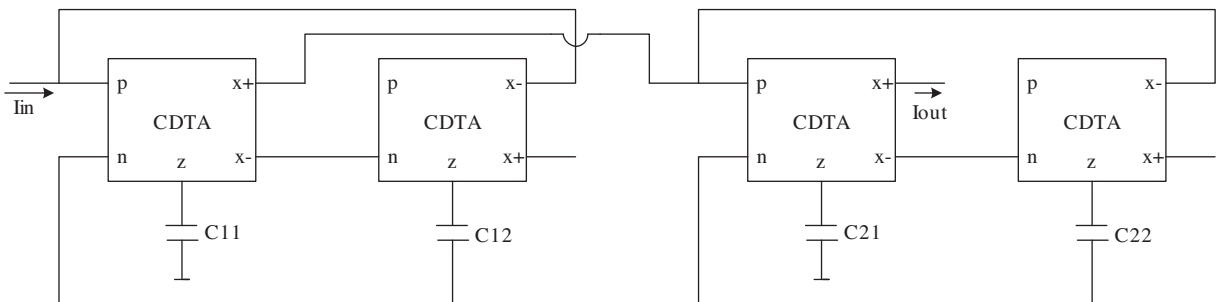

Figure 14. A fourth-order band-pass filter realized with CDTAs.

The total harmonic distortion (THD) results for the fourth-order BP filter from Figure 14 are given in Figure 16, which clearly shows that for an input signal lower than 200 μA, the THD remains within acceptable limits, thus confirming the practical utility of the proposed circuit. In Figure 17, for an input signal of 100 μA at 10 MHz, the variation of the THD value versus output load resistance is shown. For a load resistance lower than 20 k, THD is low, less than 3%. Output amplitude change with load resistance for constant input signal is given in Figure 17; it is seen that at 10 MHz, a large swing of $V_O = 1.43$ V is obtained at the output.
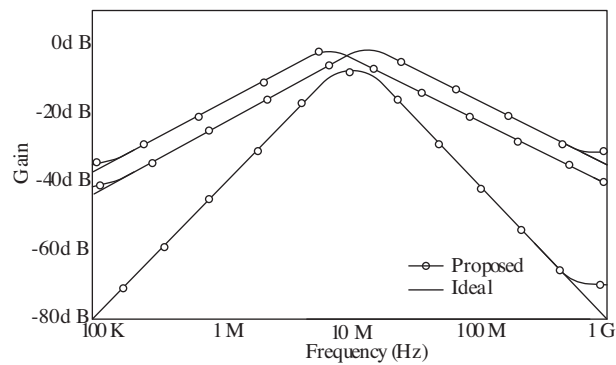
Figure 15. PSpice simulation results of frequency response of the fourth-order band-pass filter.
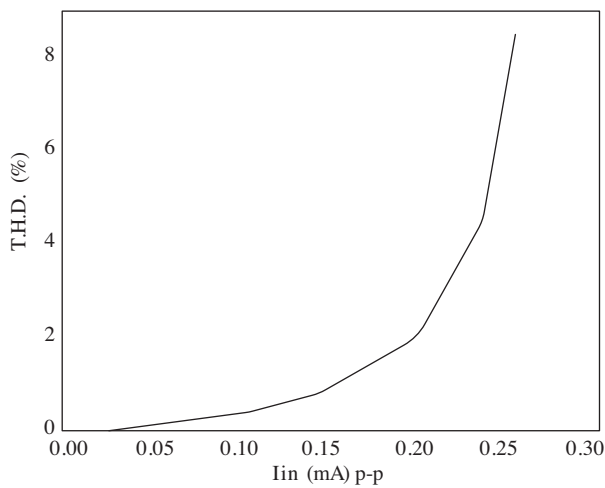

Figure 16. THD of the fourth-order band-pass filter for an input signal of 100 μA at 10 MHz.
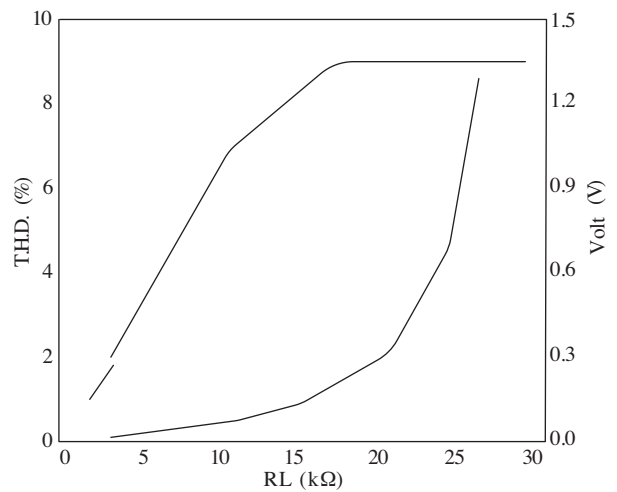

Figure 17. THD and dependence of the output amplitude versus load resistance for an input signal of 100 μA at 10 MHz.

6. Conclusion

In this paper, a high performance CMOS implementation of current differencing transconductance was presented. Simulated device characteristics showed that the proposed circuit exhibits a very good performance. The simulation results confirmed the high performance provided by the circuit in terms of low input, high output resistances, and a wide linearity range for both the voltage and current operations. The performance of the proposed circuit was tested with an application example of a current-mode universal biquad filter. A fourth-order band-pass filter was realized to illustrate the practical use of the proposed topologies as an application example. PSpice simulation results were given to verify the theory. It was seen that the simulation results verified the theory. The circuit can be considered another good alternative for the circuit designer besides the other topologies in the literature realized with CMOS and BJT technologies [15-26].

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