

Application of asymmetrical periodic signals as test vectors for analog fault detection: a novel perspective of classical concepts

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Abstract

Analog fault diagnosis is a field of paramount importance, and test signal generation is an important prerequisite for analog fault detection. Several stimuli have been used as input test vectors. This study presents a novel approach for the adoption of classical methods and signals for fault detection. This involves the use of asymmetrical periodic signals and comparison of their effectivity in maximizing output response between faulty and conforming circuits. The technique helps to determine a minimal set of test signals for a circuit. It also enables the test designer to identify the parts of the frequency spectra of various signal types that can pose problems of fault masking and fault dominance. In addition, the technique indicates certain sets of components forming ambiguity groups, which exhibit complementary fault-masking effects. The method does not require access to internal nodes of the circuit. It only requires generation of standard asymmetrical signals and hence can be implemented with the use of commonly available function generators. The technique is applicable to integrated circuits and printed circuit boards, as well as analog subsystems. It can also be applied for fault isolation. The results include responses from representative benchmark analog circuits.

Key Words: Analog fault detection, analog test vector generation, asymmetrical periodic signals

1. Introduction

Analog and mixed-signal testing is a field of paramount importance in today's monolithic integrated circuit (IC) production, as well as in printed circuit boards (PCBs) and subsystem and system-level integration and production. The significance of analog testing is further increased by the constantly growing and widening field of system-on-chip ICs.

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1.1. Historical perspective

The emergence of analog fault diagnosis can be roughly traced back to the 1960s, when the US Department of Defense expressed interest in provision of rapid field servicing of circuit boards in weapons, navigation, and communication systems [1]. Contrary to digital domain testing, however, analog testing had many challenges to overcome. Among these, the one that could be termed most formidable was the development of methodologies for differentiation between conforming and faulty circuits. In this regard, in contrast to their digital counterparts, the continuum and nondiscrete nature of analog signals (both excitations and responses) posed a great difficulty [1]. The situation was further worsened with the realization that the parametric values of analog components also follow a nondiscrete trend. Efforts were continuously made in past decades to clear the roadblocks to progress in analog fault detection, but one of the primary problems is the absence of (automatic) test pattern (vector) generation [2].

In the digital world, the goal of a test vector is to force the responses of nonfaulty and faulty circuits into opposite states, while the purpose of analog test vectors is to maximize the difference between the responses of faulty and nonfaulty circuits [3]. Since the advent of the discipline of analog fault detection, a number of test signal configurations have been used to constitute input test signal vectors for the purpose of analog fault detection. These concepts were further applied for the purposes of fault isolation and localization, as well. The most used input test signals so far include direct current (DC) voltages [4], piecewise continuous functions [5], step input signals [6], and piecewise linear [7] test signals. Concurrently, instead of test signal injection, power supply parameters have also been monitored for variations in order to detect faults; [8] employs steady state current testing and [9] suggests ramping power supply voltage and obtaining quiescent current signatures. Triangular wave and ramp signals were used for analog-to-digital converter testing in [10]. In one of the more relevant works [11], ramp signals, including square as well as sawtooth waveforms, were used for fault detection. However, in the majority of earlier as well as more recent works, sinusoidal signals have predominantly been used as the input test signal. The emphasis is gradually shifting toward determining signal attributes such as frequency or amplitude for achieving better fault coverage by the use of various techniques, including heuristics, but the signal waveform is mostly sinusoidal [12-16].

1.2. Purpose and contribution

This paper presents the details of a study that was carried out to investigate the comparative effectivity of 3 asymmetrical waveforms. These waveforms include sine wave, sawtooth wave, and square wave. Although a multitude of works have exploited one or another of these waveforms, to our knowledge, so far no study has been attempted to undertake a simultaneous comparative study of all 3 waveforms, particularly employing usage of variable T-rise for the sawtooth waveform and variable duty cycle for square waveform signals. The yardstick for comparison is the maximization of output response. As symmetrical signals are special cases of asymmetrical signals, they were also included in the study. The intent was also to find a test vector with a minimal number of test signals that could be used for fault detection in a circuit. It is therefore envisaged that the technique can be used in addition to and in conjunction with functional testing for the segregation of circuits with faulty components. The methodology presented can also be applied for the purpose of fault isolation and localization.

2. The methodology of investigation and algorithm

In [17], it was suggested that the parametric approach offers better fault coverage and test quality with shorter test time as compared to functional and structural approaches. Hence, this investigation encompassed the study of parametric variations in the values of capacitances for capacitors, resistances for resistors, and forward current gain (h_{fe}) for NPN bipolar junction transistors, respectively. The study comprised sine wave, sawtooth wave, and square wave signal waveforms. The V_{pp} for all waveforms was set to 2 V, and V_p was set to 1 V. The study involved a frequency sweep for the sine wave. Eleven frequency sweeps were carried out for the sawtooth waveform. For each individual frequency sweep, the waveform followed the relation:

$$T\text{-rise} = (X/100) \times T\text{-period}, \quad (1)$$

where T-rise is the rise time for the sawtooth waveform, T-period is the time period of the waveform, and X was incremented from 0 to 100 in incremental steps of 10.

Nine frequency sweeps were carried out for the square wave. For each individual frequency sweep, the waveform followed the relation:

$$\text{Duty cycle} = (Y/100) \times T\text{-period}, \quad (2)$$

where the duty cycle is the portion of pulse for which the voltage level remains high, T-period is the time period of the waveform, and Y was incremented from 10 to 90 in incremental steps of 10.

One fault was simulated at one instance. The value of each component was varied from 50% of nominal value to 150% of nominal value in incremental steps of 10% of the nominal value. Frequency sweeps for each type and configuration of the test signals under discussion were then carried out for each component value. Log scale was used for frequency sweep. The V_{out} (V_o) was determined by simulation at each frequency. As V_{in} was set to $V_p = 1$ V, V_o could be termed as analogous to the numerical value of the system transfer function. The log scale graph of V_o versus frequency was plotted for each component value. This resulted in 11 tracks for a particular component and particular T-rise or duty cycle for the sawtooth and square waveform, respectively.

Subsequently, 2 additional tracks were plotted versus frequency. These were the modulus of difference between the magnitudes of V_o (ΔV_o) for tracks having values of 50% and 90% of nominal component value, and the modulus of difference between the magnitude of V_o (ΔV_o) for tracks having values of 150% and 110% of nominal component value, respectively. This effectively resulted in the assumption that component variations of values within $\pm 10\%$ of nominal values were within the acceptable limits. The maximum ΔV_o points were identified from these 2 tracks of ΔV_o for each graph. Finally, the test signal configurations (waveform type and T-rise or duty cycle, if applicable) with the maximum ΔV_o for each component were selected. As there are 2 maximum ΔV_o values for each component, 1 for parameter variations having magnitudes less than the nominal value and 1 for parameter variations having magnitudes greater than the nominal value, the number of test vectors for a circuit/system with N-components can be defined as below.

$$\text{No. of test signals} \leq 2N \quad (3)$$

The inequality holds when same signal is used to detect faults on both sides of the tolerance values around the nominal value of a particular component, or when one signal configuration is used for more than one component.

3. The study and findings

3.1. The experimental circuits

Simulation studies were carried out to apply the above methodology to 3 benchmark circuits using MATLAB. It has to be acknowledged here that there is a scarcity of benchmark circuits for mixed-signal and analog testing and fault detection. The latest set of benchmark circuits for analog and mixed-signal testing was formalized and reported at the International Test Conference in 1997 [18]. A subsequent study based on [18] proposed some additional circuits [19]. An attempt was made to base this study on diverse analog circuits so that the findings would be more generic; hence, 2 important analog circuit building blocks, a filter and an amplifier, were selected for this study.

The 3 benchmark circuits used for this study were:

- i) Continuous-time state variable filter (CT filter) [18], in Figure 1;
- ii) Active low-pass filter (LP filter) [19], in Figure 2;
- iii) Single stage common emitter amplifier (CE amplifier) [19], in Figure 3.

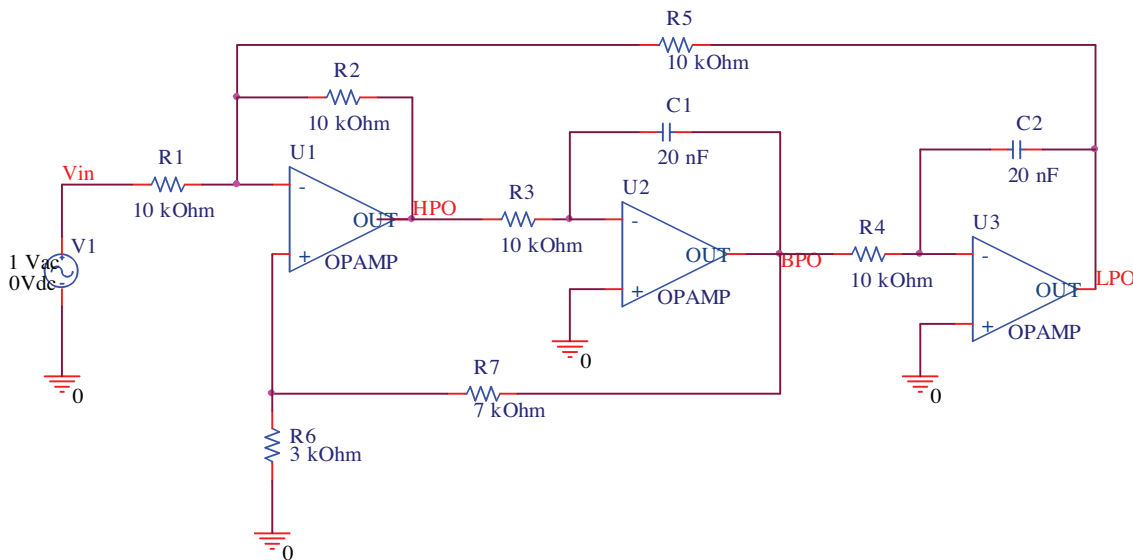


Figure 1. Continuous-time state variable filter schematic.

The CT filter has 3 outputs, a high-pass output (HPO), band-pass output (BPO) and low-pass output (LPO). For this study, the magnitudes of all of these outputs were summed to obtain a single output parameter. For the LP filter and the CE amplifier, single typical outputs were used, as shown in Figures 2 and 3.

3.2. The selection of test signals

Tables 1 and 2 correspond to the CT filter, Table 3 corresponds to the LP filter, and Tables 4 and 5 correspond to the CE amplifier. These tables summarize the results obtained in regards to the selection of test signal configurations that maximize ΔV_o for a particular component as a given circuit. As mentioned earlier, separate

signals were identified for tolerance values above and below the nominal value. However, in Tables 1-5, the percentage of ΔV_o obtained with the same signal for the opposite tolerance band is also indicated. This enables the test designer to determine the trade-off if he or she wants to use the same signal for tolerance values on both sides of the nominal value for a component.

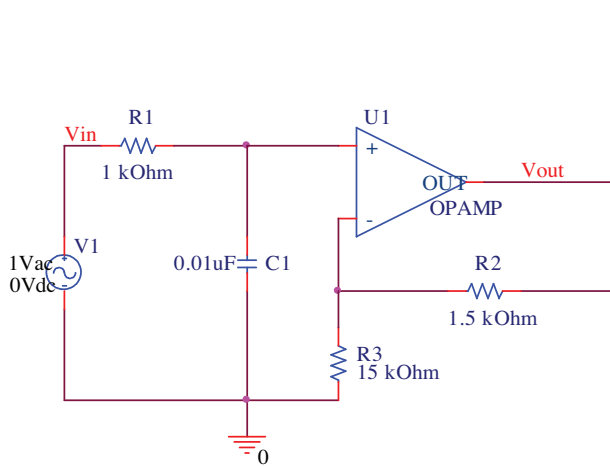


Figure 2. Low-pass filter schematic.

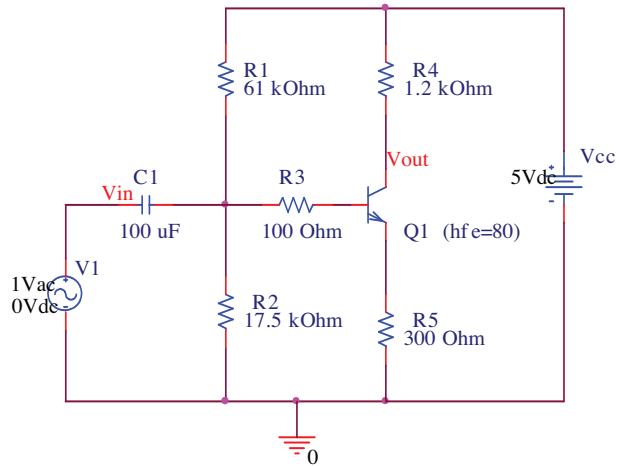


Figure 3. Common emitter amplifier schematic.

Table 1. Signals maximizing ΔV_o for CT filter (Part A).

Attributes of test signals maximizing ΔV_o						
Component		R1	R2	R3	R4	R5
Max ΔV_o signal	Tolerance side	-ve	-ve	-ve	-ve	-ve
	Signal waveform ¹	SQ	SQ	SQ	SQ	SQ
	T-rise or DC (X%) ²	90	60	60	70	50
	Frequency (Hz)	100	800	700	1000	700
	V_o amplitude (V) (a)	3.484	2.104	0.8481	1.468	1.61
Corresponding antagonistic signal	V_o amplitude (V) (b)	1.043	0.9465	0.2904	0.447	0.4544
	% of antagonistic max ΔV_o signal (c) ³	89.84	61.74	34.30	69.70	45.55
Antagonistic max ΔV_o signal	Tolerance side	+ve	+ve	+ve	+ve	+ve
	Signal waveform ¹	SQ	SQ	SQ	SQ	SQ
	T-rise or DC (X%) ²	70	70	50	60	90
	Frequency (Hz)	500	1000	600	800	40
	V_o amplitude (V) (d)	1.161	1.533	0.8466	0.6413	0.9976
Corresponding antagonistic signal	V_o amplitude (V) (e)	3.404	1.646	0.547	0.052	0.8146
	% of antagonistic max ΔV_o signal (f) ⁴	97.7	78.23	64.5	3.54	50.6

¹Signal waveform: sine = SN, sawtooth = ST, square = SQ.

²T-rise = X% of T-period of sawtooth waveform; DC = duty cycle = X% of T-period of square wave while signal level is high.

³c = (b / d) × 100.

⁴f = (e / a) × 100.

Table 2. Signals maximizing ΔV_o for CT filter (Part B).

Attributes of test signals maximizing ΔV_o					
Component		R6	R7	C1	C2
Max ΔV_o signal	Tolerance side	-ve	+ve	-ve	-ve
	Signal waveform ¹	SQ	SQ	SQ	SQ
	T-rise or DC (X%) ²	50	50	60	70
	Frequency (Hz)	800	800	700	1000
	V_o amplitude (V) (a)	2.321	1.076	0.8481	1.468
Corresponding antagonistic signal	V_o amplitude (V) (b)	0.6464	1.029	0.2904	0.447
	% of antagonistic max ΔV_o signal (c) ³	100	95.63	34.30	69.7
Antagonistic max ΔV_o signal	Tolerance side	+ve	-ve	+ve	+ve
	Signal waveform ¹	SQ	SQ	SQ	SQ
	T-rise or DC (X%) ²	50	60	50	60
	Frequency (Hz)	800	700	600	800
	V_o amplitude (V) (d)	0.6464	1.076	0.8466	0.6413
Corresponding antagonistic signal	V_o amplitude (V) (e)	2.321	0.988	0.547	0.052
	% of antagonistic max ΔV_o signal (f) ⁴	100	91.82	64.5	3.54

¹Signal waveform: sine = SN, sawtooth = ST, square = SQ.

²T-rise = X% of T-period of sawtooth waveform; DC = duty cycle = X% of T-period of square wave while signal level is high.

³c = (b / d) × 100.

⁴f = (e / a) × 100.

Table 3. Signals maximizing ΔV_o for LP filter.

Attributes of test signals maximizing ΔV_o					
Component		R1	R2	R3	C1
Max ΔV_o signal	Tolerance side	-ve	-ve	-ve	-ve
	Signal waveform ¹	ST	SQ	SQ	ST
	T-rise or DC (X%) ²	100	10 to 90	10 to 90	100
	Frequency (Hz)	290k	70	70	290k
	V_o amplitude (V) (a)	0.2906	0.04	0.089	0.2906
Corresponding antagonistic signal	V_o amplitude (V) (b)	0.1066	0.04	0.0248	0.1066
	% of antagonistic max ΔV_o signal (c) ³	68.91	100	100	68.91
Antagonistic max ΔV_o signal	Tolerance side	+ve	+ve	+ve	+ve
	Signal waveform ¹	ST	SQ	SQ	ST
	T-rise or DC (X%) ²	90	10 to 90	10 to 90	90
	Frequency (Hz)	90k	70	70	90k
	V_o amplitude (V) (d)	0.1547	0.04	0.0248	0.1547
Corresponding antagonistic signal max	V_o amplitude (V) (e)	0.2467	0.04	0.089	0.2467
	% of antagonistic max ΔV_o signal (f) ⁴	84.89	100	100	84.89

¹Signal waveform: sine = SN, sawtooth = ST, square = SQ.

²T-rise = X% of T-period of sawtooth waveform; DC = duty cycle = X% of T-period of square wave while signal level is high.

³c = (b / d) × 100.

⁴f = (e / a) × 100.

3.3. Discussion of results and observations

Of the 3 circuits studied, the sine wave maximized the value of ΔV_o in only 1 circuit. Hence, it can be inferred that the sine wave is least effective in maximizing the value of ΔV_o when compared with sawtooth and square waveforms. However, this statement can be circuit-specific and may or may not be considered as a general trend. In all cases, sawtooth waveforms with step-rising edges produce a peculiar response that is different from those of other sawtooth waveforms with different T-rise values. The tolerance tracks as well as the ΔV_o tracks may overlap in some portion of the frequency response curve. Such portions should be avoided while selecting the input test signal, as phenomena such as fault masking and/or fault dominance [20] are likely to occur. In such cases, the distinction in the response due to different tolerances of the same component is not discernable. It has been further observed that the one test vector that maximizes ΔV_o on one side of the nominal value does not necessarily maximize ΔV_o on the other side of the nominal value. Hence, the number of test vectors approximately approaches the value of $2 \times N$, where N is the number of components studied in the system. Another favorable finding that emerged was that, in most cases, a unique value of max ΔV_o was found. In the event that a unique test signal cannot be determined and a range is indicated by this analysis, an appropriate signal can be chosen that possibly fulfills some functional testing requirements or even some other constraints.

3.3.1. Observations on CT filter

The response to a sawtooth waveform with T-rise = 0 (Figure 4) is analogous to the response to square waveforms (Figure 5). Furthermore, at T-rise = T-period, the response shows a flattened peak (Figure 6). This presents a comparatively larger part of the frequency spectrum from which a test signal can be selected (possibly with a ΔV_o value less than the maximum value but reasonably close to it) if it also covers some functional testing requirements.

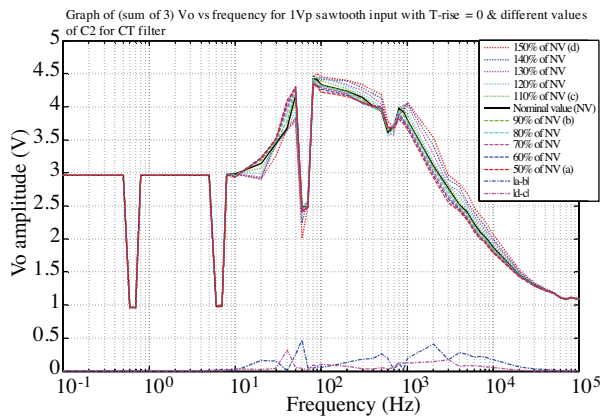


Figure 4. Response of C2 in CT filter for sawtooth waveform with T-rise = 0.

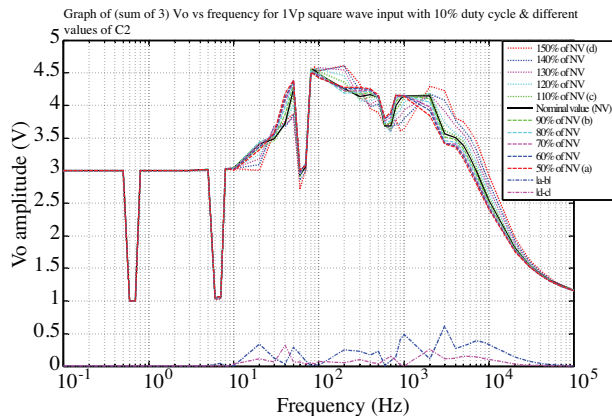


Figure 5. Response of C2 in CT filter for square waveform with 10% duty cycle.

The peaks of tracks depicting V_o for different tolerance values drop in magnitude and flatten gradually as the T-rise for the sawtooth waveform increases from 10% to 90%. Moreover, the responses of the circuit to sawtooth waveforms (except for T-rise = 0 and T-fall = 0) are analogous to circuit responses to the sinusoidal waveform. In the case of square waveforms, the tolerance tracks initially show pointed peaks, but gradually flattened portions appear up to a certain duty cycle. As the duty cycle is increased further, additional peaks arise in the farther regions of the spectrum. Figures 7-9 reflect this trend.

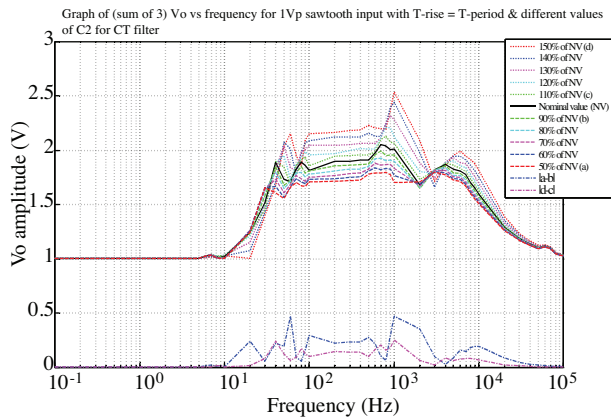


Figure 6. Response of C2 in CT filter for sawtooth waveform with $T\text{-rise} = T\text{-period}$.

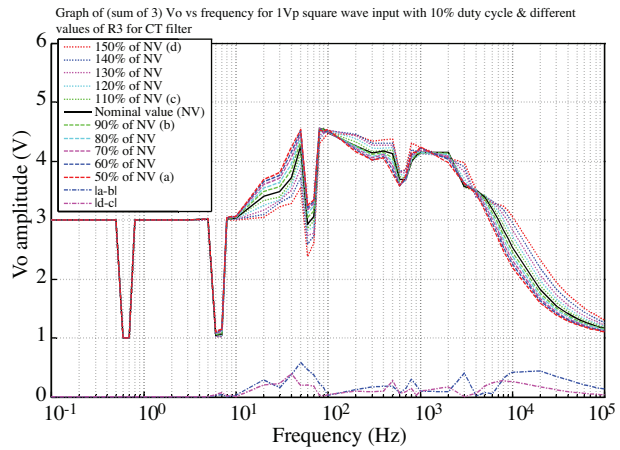


Figure 7. Response of R3 in CT filter for square waveform with 10% duty cycle.

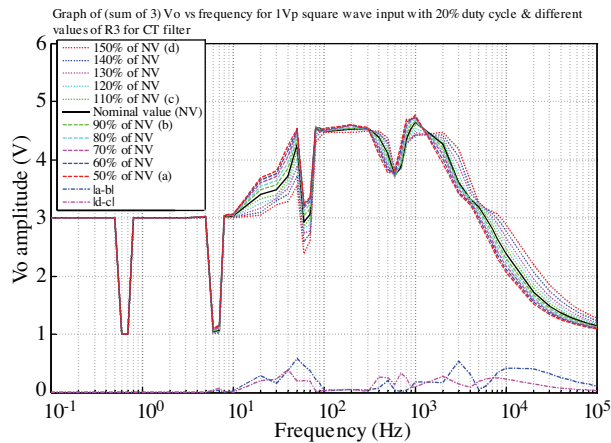


Figure 8. Response of R3 in CT filter for square waveform with 20% duty cycle.

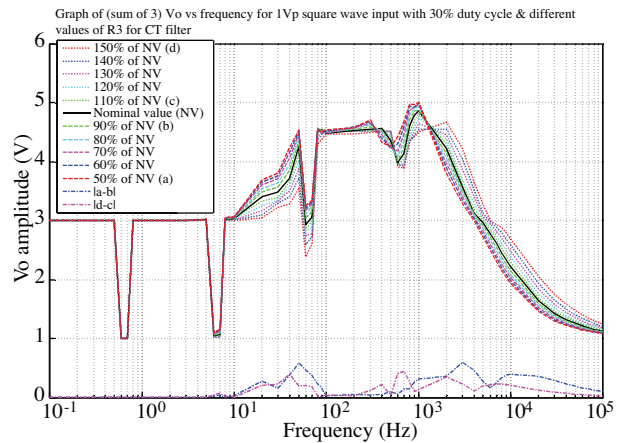


Figure 9. Response of R3 in CT filter for square waveform with 30% duty cycle.

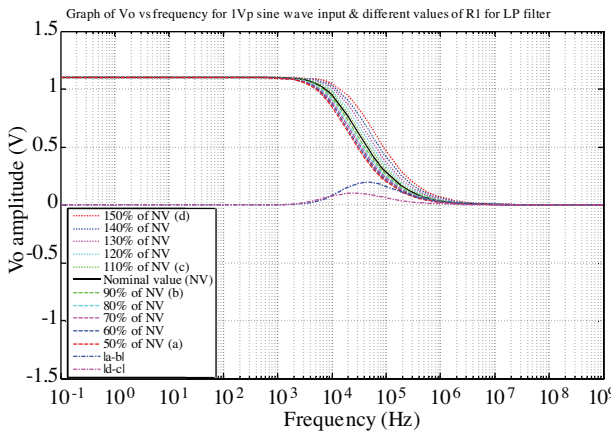


Figure 10. Response of R1 in LP filter for sine wave.

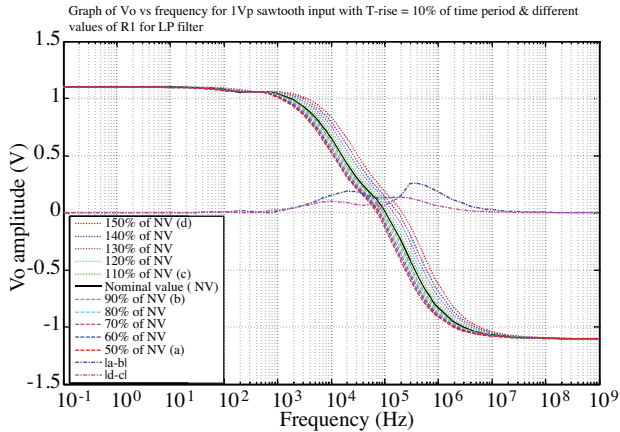


Figure 11. Response of R1 in LP filter for sawtooth wave with $T\text{-rise} = 10\%$ of $T\text{-period}$.

3.3.2. Observations on LP filter

The circuit response to the sine wave (Figure 10) can be termed similar to the sawtooth waveform response with T-rise values from 10% to 100%, except that in case of the sawtooth waveform, the response swings symmetrically about the +ve frequency axis. In these cases, the roll-off rate increases as the T-rise increases. Figures 11-13 depict this phenomenon. A square wave with all duty cycle values produces the same value of ΔV_o at the same frequency for all components in the LP filter.

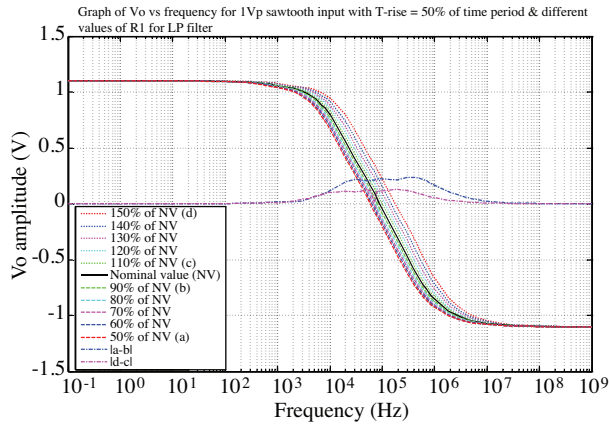


Figure 12. Response of R1 in LP filter for sawtooth wave with T-rise = 50% of T-period.

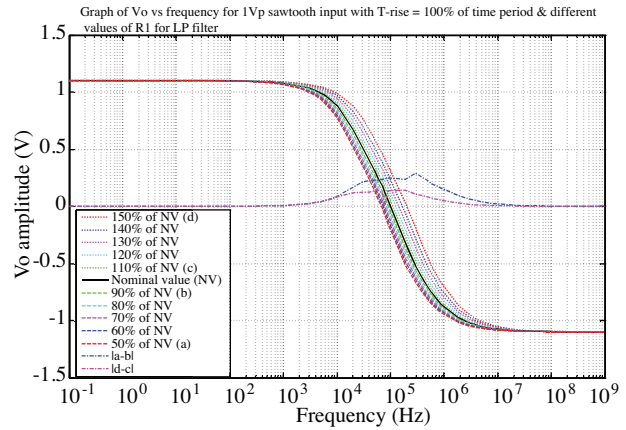


Figure 13. Response of R1 in LP filter for sawtooth wave with T-rise = 100% of T-period.

3.3.3. Observations on CE amplifier

In response to sinusoidal signals, the tolerance tracks overlap in the initial elevated flat portion of the response curve prior to the roll-off region. It is advisable to avoid this region while selecting a test signal. The frequency sweep start point selected for the CE amplifier was 10 kHz, as initial studies indicated that the part of the frequency spectrum prior to this value did not produce significantly observable results. The higher cut-off frequency (f_{ch}) was, of course, included in the frequency sweep. The end frequency of the sweep was arbitrarily chosen after the response remained fairly constant; however, the end frequency for a particular circuit may be selected while keeping in view the circuit operations and devices' operation frequency constraints.

The response of the circuit to variations in the values of R1 and R2, which form the voltage divider biasing scheme, and variations in the forward current gain (h_{fe}) of transistor Q1 (Figure 3) produce similar results when the square waveform is used with different duty cycles. For these components, ΔV_o occurs at the terminal end of the frequency spectrum used for this study.

The responses to sawtooth waveforms can be called mirror images of the sine wave response, but with different gain values. Moreover, the roll-off portion of the frequency response traverses up the spectrum as the T-rise increases. The roll-off rate of the frequency response curve decreases for almost all components as the duty cycle of the square wave is increased. Figures 14-16 illustrate this observation.

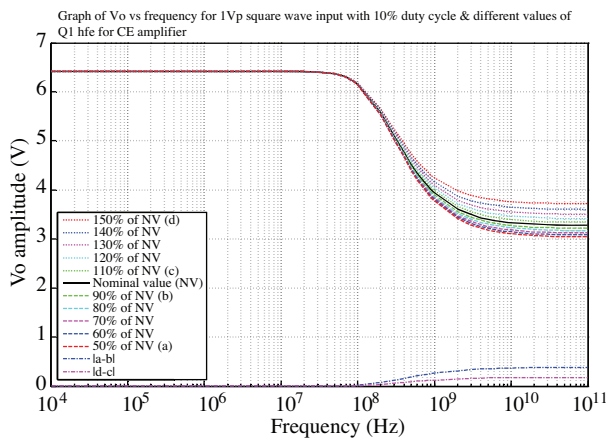


Figure 14. Response of Q1 in CE amplifier for square wave with 10% duty cycle.

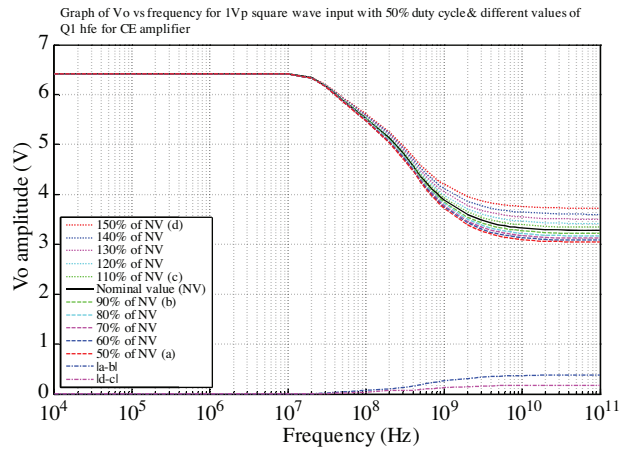


Figure 15. Response of Q1 in CE amplifier for square wave with 50% duty cycle.

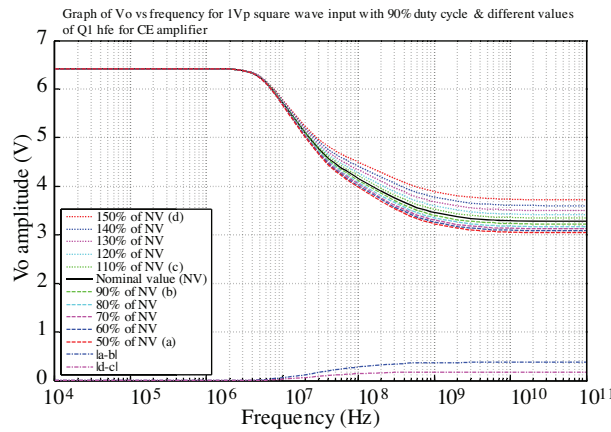


Figure 16. Response of Q1 in CE amplifier for square wave with 90% duty cycle.

4. Conclusion

4.1. Limitations of the proposed approach

The proposed technique has some limitations, like any other method. In some cases, the peaks of consecutive tolerance tracks are skewed. In this case, the difference in V_o among all of the tracks might not be maximal, but the test designer can determine an optimal test signal by considering the relevant trade-offs. However, this might present a problem when the method is employed for fault isolation.

Some typical cases of fault masking between 2 components are observed in the filter circuit topologies. Tables 2 and 3 for the CT filter show that 2 component sets have the same test signals that maximize ΔV_o . One set is R3 and C1, while the other is R4 and C2. A similar situation is observed in the case of R1 and C1 in the LP filter, as seen in Table 4. In such cases, the methodology adopted in this paper might help to detect faults attributable to the 2 relevant components as a set, but some additional techniques might be needed to further determine which of the 2 components is faulty.

Table 4. Signals maximizing ΔV_o for CE amplifier (Part A).

Attributes of test signals maximizing ΔV_o					
Component		R1	R2	R3	R4
Max ΔV_o signal	Tolerance side	-ve	-ve	-ve	-ve
	Signal waveform ¹	ST	ST	SQ	SQ
	T-rise or DC (X%) ²	80	40	90	10
	Frequency (Hz)	2G	400M	6M	1G
	V_o amplitude (V) (a)	1.671	0.9624	0.214	0.8067
Corresponding antagonistic signal	V_o amplitude (V) (b)	0.5292	0.5199	0.121	0.7205
	% of antagonistic max ΔV_o signal (c) ³	88.66	99.35	85.03	95.3
Antagonistic max ΔV_o signal	Tolerance side	+ve	+ve	+ve	+ve
	Signal waveform ¹	ST	ST	ST	SN
	T-rise or DC (X%) ²	70	50	60	
	Frequency (Hz)	900M	600M	39G	80M
	V_o amplitude (V) (d)	0.5969	0.5233	0.1423	0.756
Corresponding antagonistic signal	V_o amplitude (V) (e)	1.667	0.9582	0.1976	0.6722
	% of antagonistic max ΔV_o signal (f) ⁴	99.76	99.56	92.34	83.33

¹Signal waveform: sine = SN, sawtooth = ST, square = SQ.

²T-rise = X% of T-period of sawtooth waveform; DC = duty cycle = X% of T-period of square wave while signal level is high.

³c = (b / d) \times 100.

⁴f = (e / a) \times 100.

Table 5. Signals maximizing ΔV_o for CE amplifier (Part B).

Attributes of test signals maximizing ΔV_o				
Component		R5	C1	Q1 h_{fe}
Max ΔV_o signal	Tolerance side	-ve	-ve	-ve
	Signal waveform ¹	ST	ST	ST
	T-rise or DC (X%) ²	80	30	10
	Frequency (Hz)	900M	10k	40M
	V_o amplitude (V) (a)	1.061	0.0105	0.394
Corresponding antagonistic signal	V_o amplitude (V) (b)	0.465	0.0024	0.1807
	% of antagonistic max ΔV_o signal (c) ³	88.96	70.59	95.26
Antagonistic max ΔV_o signal	Tolerance side	+ve	+ve	+ve
	Signal waveform ¹	ST	ST	ST
	T-rise or DC (X%) ²	70	20 to 70	10
	Frequency (Hz)	400M	10k	90M
	V_o amplitude (V) (d)	0.5227	0.0034	0.1897
Corresponding antagonistic signal	V_o amplitude (V) (e)	0.9183	0.009	0.3893
	% of antagonistic max ΔV_o signal (f) ⁴	86.55	85.71	98.81

¹Signal waveform: sine = SN; sawtooth = ST; square = SQ.

²T-rise = X% of T-period of sawtooth waveform; DC = duty cycle = X% of T-period of square wave while signal level is high.

³c = (b / d) \times 100.

⁴f = (e / a) \times 100.

In some cases, the difference in the ΔV_o values for different test signal configurations is not significant. As a uniform rule, ΔV_o was measured to up to 4 decimal places and used for discrimination between the test signals in this study. However, this can be varied according to given criteria and circumstances.

This paper primarily demonstrates the concept of asymmetrical signal application as input test signals. For indication of conforming circuit response, nominal component values are used. However, this limitation is not very significant, as the emphasis is on separation between conforming and nonconforming component parameter values.

The study involved the generation of 21 graphs for each individual component. On a P-IV 2.66 GHz system with 512 MB RAM, it takes about 189 min to generate 21 graphs for a single component. In this scenario, the proposed technique might (or might not) be deemed computationally expensive. However, this computational expense might appear insignificant and affordable if this method is employed at the design and/or industrialization stage.

4.2. Advantages and applications

The technique presented here enables detection of soft (parametric) faults in analog circuits by the use of classical signals in a practical and simple but novel way. It can be applied with equal success at all levels to analog circuit abstraction, including but not limited to monolithic analog and mixed-signal ICs, PCB assemblies, and possibly analog subsystems. It only uses available (possibly singular) input and output nodes and does not require access to internal circuit nodes. The methodology generates a minimal set of $2 \times N$ test signals for a circuit with N components. This naturally helps to reduce both the time and the resources needed for analog fault detection. Though the technique is primarily focused on fault detection, it can also be used for fault isolation. This method can be classified as a simulation-before-test method for fault detection and the fault dictionary can be generated by determining the values of V_o for different tolerance values obtained by using the same test signal configuration. It can be inferred that the passive components (resistor and capacitor) forming a filtering element produce identical responses when excited by a particular waveform. Hence, in one way, they are susceptible to phenomena of fault masking and/or fault dominance. Equivalently, they can be said to form ambiguity groups. This effect is observable both in the CT filter as well as the LP filter. In addition, some other portions of spectra are observed by using this technique where fault masking and/or fault dominance is likely to occur. Hence, this methodology helps to identify the ambiguity groups of the components and the parts of spectra that can cause fault dominance/masking; thus, effective and efficient test vectors can be selected by avoiding such spectral regions.

As the test procedure adopts usual sine waves and sawtooth and square waves with common saw tooth and duty cycle configurations, commonly used signal generators can be used during the testing and use of more complex, intricate, and expensive test pattern generators can be avoided.

It is proposed that the test vectors obtained through application of this technique might be used in addition to functional testing, if so desired. Functional testing is usually complex and costly, both in terms of time and material resources. It is quite possible that some incipient fault might be present and/or that some component might have a parameter value outside of the permissible tolerance limit, yet not manifest its effect during the functional testing. The proposed algorithm, in addition to being used in specification-based testing techniques, can be used by original equipment manufacturers that produce a generic product with a number of various divergent end-use applications. By employing this technique in addition to functional testing, original equipment manufacturers can be more confident in their product by being able to screen out the components with parameter values outside of the permissible tolerance limits.

References

- [1] B.R. Epstein, M. Czigler, S.R. Miller, "Fault detection and classification in linear integrated circuits: an application of discrimination analysis and hypothesis testing", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, Vol. 12, pp. 102-113, 1993.
- [2] K. Arabi, "Special session 6C: New topic mixed-signal test impact to SoC commercialization", *28th VLSI Test Symposium*, pp. 212-212, 2010.
- [3] S.J. Tsai, "Test vector generation for linear analog devices", *Proceedings of International Test Conference*, p. 592, 1991.
- [4] G. Devarayanadurg, M. Soma, "Analytical fault modeling and static test generation for analog ICs", *IEEE/ACM International Conference on Computer-Aided Design*, pp. 44-47, 1994.
- [5] G. Devarayanadurg, M. Soma, "Dynamic test signal design for analog ICs", *Proceedings of the 1995 IEEE/ACM International Conference on Computer-Aided Design*, pp. 627-630, 1995.
- [6] B. Burdick, "Generation of optimum test stimuli for nonlinear analog circuits using nonlinear programming and time-domain sensitivities", *Proceedings of Design, Automation and Test in Europe Conference and Exhibition*, pp. 603-608, 2001.
- [7] P. Kalpana, K. Gunavathi, "Test-generation-based fault detection in analog VLSI circuits using neural networks", *ETRI Journal*, Vol. 31, pp. 209-214, 2009.
- [8] C. Patel, A. Singh, J. Plusquellic, "Defect detection using quiescent signal analysis", *Journal of Electronic Testing*, Vol. 21, pp. 463-483, 2005.
- [9] J.P. de Gyvez, G. Gronthoud, R. Amine, "Multi-VDD testing for analog circuits", *Journal of Electronic Testing*, Vol. 21, pp. 311-322, 2005.
- [10] S. Bernard, F. Azaïs, Y. Bertrand, M. Renovell, "On-chip generation of ramp and triangle-wave stimuli for ADC BIST", *Journal of Electronic Testing*, Vol. 19, pp. 469-479, 2003.
- [11] C.E. Stroud, E.B. Bradley, *Mixed Signal Built-In Test for Analog Circuits*, AFRL-IF-RS-TR-1999-189 Final Technical Report, Rome, NY, USA, Air Force Research Laboratory, 1999.
- [12] A. Abderrahman, Y. Savaria, A. Khouas, M. Sawan, "Accurate testability analysis based-on multi-frequency test generation and a new testability metric", *IEEE Northeast Workshop on Circuits and Systems*, pp. 1356-1359, 2007.
- [13] E. Korhonen, C. Wegener, J. Kostamovaara, "Combining the standard histogram method and a stimulus identification algorithm for A/D converter INL testing with a low-quality sine wave stimulus", *IEEE Transactions on Circuits and Systems I: Regular Papers*, Vol. 57, pp. 1166-1174, 2010.
- [14] A. Bounceur, S. Mir, E. Simeu, L. Rolíndez, "Estimation of test metrics for the optimisation of analogue circuit testing", *Journal of Electronic Testing*, Vol. 23, pp. 471-484, 2007.
- [15] S.J. Spinks, C.D. Chalk, I.M. Bell, M. Zwolinski, "Generation and verification of tests for analog circuits subject to process parameter deviations", *Journal of Electronic Testing*, Vol. 20, pp. 11-23, 2004.
- [16] P. Jantos, D. Gzechca, T. Golonek, J. Rutkowski, "Heuristic methods to test frequencies optimization for analogue circuit diagnosis", *Bulletin of the Polish Academy of Sciences - Technical Sciences*, Vol. 56, pp. 29-38, 2008.

- [17] J. Brenkus, V. Stopjakova, R. Vanhooren, A. Chichkov, "Efficiency evaluation of various test strategies on mixed-signal circuit", *Journal of Electrical Engineering*, Vol. 60, pp. 261-267, 2009.
- [18] B. Kaminska, K. Arabi, I. Bell, P. Goteti, J.L. Huertas, B. Kim, A. Rueda, M. Soma, "Analog and mixed-signal benchmark circuits-first release", *International Proceedings of Test Conference*, pp. 183-190, 1997.
- [19] R. Kondagunturi, E. Bradley, K. Maggard, C. Stroud, "Benchmark circuits for analog and mixed-signal testing", *IEEE Proceedings of Southeastcon '99*, pp. 217-220, 1999.
- [20] M. Renovell, F. Azaïs, Y. Bertrand, "Detection of defects using fault model oriented test sequences", *Journal of Electronic Testing*, Vol. 14, pp. 13-22, 1999.