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Voltage- and current-controlled high CMRR instrumentation amplifier using CMOS current conveyors

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Abstract

A new approach to the design of an instrumentation amplifier using only 2 CMOS current-controlled conveyors and an active resistor is introduced. The new approach, which has no passive components, offers a wide bandwidth and a high common-mode rejection ratio (CMRR). Electronically controllable gain by voltage and current is also obtained by this new circuit. The circuit is simulated using the parameters of a 0.35-μm TSMC CMOS technology. Theoretical analysis of the circuits was carried out, and the performance of the block circuit was confirmed through PSpice simulation results.

Key Words: *Current-mode circuits, Instrumentation amplifier, CMOS current conveyor, Common-mode rejection ratio (CMRR)*

1. Introduction

Instrumentation amplifiers are used in analog signal processing applications, which have often been used in voltage-mode measurement as an important block. Voltage-mode instrumentation amplifiers implemented by using operational amplifiers actually have high transfer function accuracy [1]. However, an important problem of these circuits is that the common-mode rejection ratio (CMRR) becomes greatly sensitive to resistor mismatching [2-4]. The CMRR is usually considered to be the most important parameter for instrumentation amplifiers. The major drawbacks of these circuits are that several matched resistors are needed in order to achieve a high CMRR, and that the circuit's wide bandwidth is gain-independent. Additionally, the voltage gain produced by voltage-mode amplifiers is the gain-bandwidth product parameter, which is limited. On the contrary, in the current-mode version of these amplifiers, the CMRR is independent of resistor mismatch, and the voltage gain of these circuits is not limited by the gain-bandwidth product [3].

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The second-generation current conveyor (CCII) has become popular as this device can be used to implement and provide electronic tunability and a broad frequency of operation in numerous high-frequency analog signal applications [5-8]. The second-generation current controlled conveyor (CCCII), which is electronically controllable by a biasing current, has been employed in many applications [9,10]. The CCCII has been used as a part of filters, oscillators, multipliers, and many current-mode applications [10-12]. The parasitic resistance of current conveyors mentioned in the next section is essentially a disadvantage in electronic circuits. However, it is used as an advantage in current-controlled conveyor circuits because it can be easily controlled by a biasing current. This resistance is directly proportional to surface mobility (μ), oxide capacitance (C_{ox}), and its relation with channel width and length (W/L) for complementary metal oxide semiconductor (CMOS) technology [13].

In the literature, some topologies using the CCII have been presented. A current-mode instrumentation amplifier based on current conveyors was introduced in 1989 [3]. Some current-mode instrumentation amplifier-based CCIIs and passive resistors have been reported [14-19]. These studies usually have small bandwidth and passive components. A more detailed explanation and comparison of these references is given in Section 4.

This paper introduces a new approach to the design of an instrumentation amplifier that consists of 2 CMOS CCCIIs and an active resistor. The proposed circuit has no passive component and was designed in standard Taiwan Semiconductor Manufacturing Company (TSMC) 0.35-μm CMOS technology. If a circuit that has CCCIIs implemented with a CMOS transistor is compared to its counterparts, it seems that the proposed circuit is well suited for biomedical applications due to its high CMRR. In addition, the proposed circuit has wide bandwidth, controllable gain by voltage and current, and low power dissipation in accordance with its CMOS structure.

2. CMOS CCCII

Second-generation current conveyors are among the most well-known current-mode analog blocks [20]. The CCCII consists of 3 terminal active circuit blocks. Its general representation is shown in Figure 1 [21].

The port characteristics of the current controlled conveyor are given in Eq. (1).

$$\begin{pmatrix} I_y \\ V_y \\ I_z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & 1 & 0 \end{pmatrix} . \begin{pmatrix} V_x \\ I_x \\ V_z \end{pmatrix} \tag{1}$$

Figure 1 shows a translinear loop consisting of M_1, M_2, M_5, and M_6 MOS transistors. When port Y of the CCCII is grounded and port X constitutes the input of the circuit (Figure 1), the parasitic resistance R_x on this terminal is described and given by:

$$R_x = \frac{1}{g_{m6} + g_{m2}} - \frac{I_{SS}}{I_x(g_{m6} + g_{m2})} \left(\frac{g_{m6}}{g_{m5}} - \frac{g_{m2}}{g_{m1}} \right). \tag{2}$$

From Eq. (2), if $g_{m5} = g_{m1}$ and $g_{m6} = g_{m2} = g_m$, R_x can be written as follows:

$$R_x = \frac{1}{2g_m} = \frac{1}{\sqrt{8k_n I_{SS}}}, \tag{3}$$

where g_m is the transconductance of the CMOS transistor and k_n is the physical parameter of the metal-oxide-semiconductor (MOS) transistor. They can be expressed as:

$$g_m = \sqrt{2k_n I_{SS}}, \tag{4a}$$

$$k_n = \mu_n C_{ox}(W/L), \tag{4b}$$

where C_{ox} is the gate capacitance per unit area and μ_n is the electron mobility of the MOS transistor. Parasitic resistance R_x also depends on the matching of the g_m values, but this parasitic resistance is available and is also tunable even if the values mismatch due to process variations.

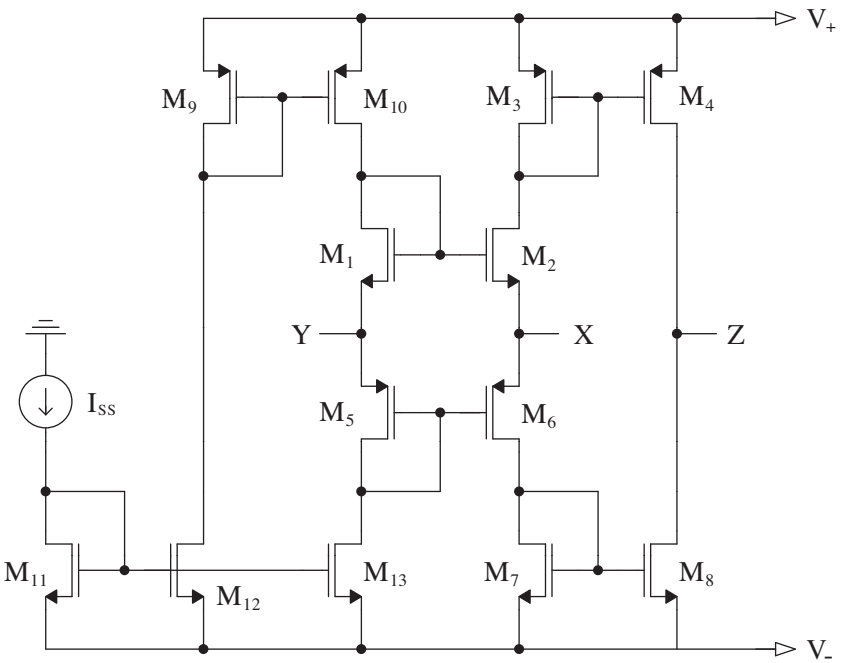

Figure 1. CMOS CCCII.

In CCCII-based circuits, realization methods take advantage of the parasitic resistance, R_x, which appears at port X of the conveyor. In these circuits, parasitic resistance is used instead of passive resistors. Resistance R_x can also be varied by means of an external bias current, I_{SS}.

3. Proposed instrumentation amplifier

Figure 2 shows the schematic diagram for the proposed instrumentation amplifier circuit.

The instrumentation amplifier consists of 2 current conveyors and an active resistor structure based on MOS transistors. The active resistor structure is realized by a parallel connected matched pair of MOS transistors, M_{R1} and M_{R2}, with the control voltage applied to the gate of M_{R2} for resistance trimming and with the gate of M_{R1} connected to the input terminal as shown in Figure 3 [22].

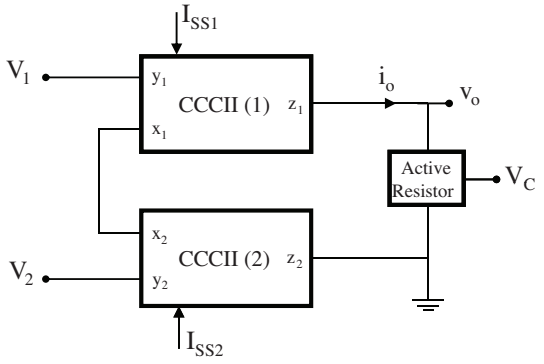

Figure 2. Proposed instrumentation amplifier.

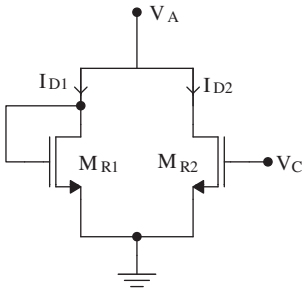

Figure 3. Active resistor.

Voltage V_C denotes the control voltage for the active resistor. The M_{R1} and M_{R2} MOS transistors are always in the triode region since $V_A < |V_{th}|$ [22]. In this case, the drain current relation can be obtained from the circuit. It can be expressed as:

$$I_{D1} = \mu_n C_{ox}(W/L)\left[(V_A - V_{th})\,V_A - \frac{V_A^2}{2}\right], \tag{5a}$$

$$I_{D2} = \mu_n C_{ox}(W/L)\left[(V_C - V_{th})\,V_A - \frac{V_A^2}{2}\right], \tag{5b}$$

where V_{th} is the threshold voltage. Thus, the total current, $I_A = I_{D1} + I_{D2}$, also shown in Figure 3, will be:

$$I_A = \mu_n C_{ox}(W/L)\,(V_C - 2V_{th})\,V_A. \tag{6}$$

From this, we can see that the resistance of active resistor R_A can be expressed as:

$$R_A = \frac{1}{\mu_n C_{ox}(W/L)\,(V_C - 2V_{th})}. \tag{7}$$

Active resistance R_A can be easily adjusted by the control voltage, V_C. As shown in Eq. (1), the current at port Z of the conveyor is equal to the current at port X. The proposed instrumentation amplifier provides a current output given by the expression:

$$i_o = \frac{v_1 - v_2}{R_{x1} + R_{x2}}. \tag{8}$$

As shown in Figure 4, R_{x1} and R_{x2} are the parasitic resistances of the first and second conveyors, respectively.

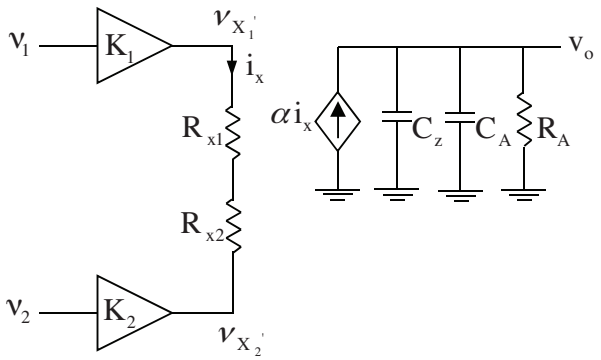

Figure 4. Error equivalent circuit of the instrumentation amplifier.

From Eq. (8), the output voltage will be:

$$\nu_o = \frac{R_A}{R_{x1} + R_{x2}}(v_1 - v_2). \tag{9}$$

It can be approximated as $R_{x1} = R_{x2}$ if I_{SS1} and I_{SS2} are assumed equal ($=I_{SS}$) for both of the current conveyors. Therefore, the low-frequency gain of instrumentation amplifier A_{dm} can be expressed as:

$$A_{dm} = \frac{R_A}{2R_x}. \tag{10}$$

It is shown that the differential gain of the instrumentation amplifier is electronically controllable by varying the bias current of the conveyors and the control voltage of the active resistor. It is known that parasitic resistance can be adjusted by a bias current and that the active resistor can be adjusted by control voltage, as well. These adjusting systems can be seen from Eqs. (3) and (7), respectively.

Taking into consideration both the current and voltage tracking errors of the current conveyors, the current and voltage tracking error between ports X-Z and ports X-Y can be expressed as follows:

$$\alpha = 1 - \varepsilon_I, \tag{11a}$$

$$K = 1 - \varepsilon_V, \tag{11b}$$

where α and K are the current and voltage transfer gains, respectively, and, ε_I and ε_V are the current and voltage transfer errors of the conveyors, respectively. Thus, at port Z, the current may be expressed as $\mathrm{i}_z = \alpha i_x$.

The voltage at port X, as shown in Figure 4, can be expressed as:

$$\nu_{X_1'} = K_1 v_1, \tag{12a}$$

$$\nu_{X_2'} = K_2 v_2. \tag{12b}$$

The resulting current, i_x, can be calculated as

$$i_x = \frac{\nu_{X_1'} - \nu_{X_2'}}{2R_X}. \tag{13}$$

We can combine Eqs. (12) and (13) to obtain:

$$i_o = \alpha i_x = \alpha \frac{K_1 v_1 - K_2 v_2}{2R_X}. \tag{14}$$

For the high-frequency operation, output voltage $\nu_o(\mathrm{s})$ can be written as follows:

$$\nu_o(s) = i_o \left(R_A // \frac{1}{sC_b} \right), \tag{15}$$

where $C_b = C_A + C_{Z1}$ is the output node capacitance, which is in parallel to the R_A resistor. We can use Eqs. (18) and (**??**) since calculation of the output voltage is given by:

$$\nu_o(s) = \alpha \frac{(K_1 v_1 - K_2 v_2)\, R_A}{2R_x\,(1 + sC_b R_A)}. \tag{16}$$

To calculate the common-mode gain, it can be assumed that $\nu_1 = \nu_2 = \nu_{cm}$, from which the common-mode gain can be obtained as:

$$A_{cm} = \frac{\nu_o}{\nu_{cm}} = \frac{\alpha\,(K_1 - K_2)\,R_A}{2R_x\,(1 + sC_bR_A)}. \tag{17}$$

For ideal current conveyors, $\alpha = K_1 = K_2 = 1$, and from Eq. (16), output differential gain A_{dm} can be written as:

$$A_{dm} = \frac{R_A}{2R_x}\left(\frac{1}{(1 + sC_bR_A)}\right). \tag{18}$$

We can see from the equations that voltage gain is controllable by $R_A\ /2R_x$ and that bandwidth is strongly dependent on C_bR_A.

4. Simulation results

To verify the validity of the theory, the circuit in Figure 2 was simulated by using the parameters of a 0.35-μm TSMC CMOS technology. A wide range of different CMOS technologies were tested to identify the most appropriate one in terms of CMRR and amplifier gain. Among these technologies, the best solution was obtained with the TSMC 0.35-μm CMOS technology, which has relatively high voltage operation and lower leakage current. The performance of the proposed circuit was verified by performing PSpice simulations with supply voltages of ± 3.3 V. Simulations were carried out using balanced input voltages with the transistor aspect ratios of PMOS and NMOS given in Table 1.

Table 1. Dimensions of the MOS transistors.

CMOS transistors	W (μm)	L (μm)
M_1-M_2	60	0.7
M_3-M_4	2	0.6
M_5-M_6	140	0.6
M_7-M_8	2	0.7
M_9-M_{10}	18	0.6
M_{11}-M_{13}	7	0.7
M_{12}	5	0.7
M_{R1}-M_{R2}	2	7

A simulation of the instrumentation amplifier shown in Figure 2 was realized using a PSpice simulation program. The simulation was operated under varying control voltages (V_C = 1.5 V, 2.5 V, and 3.5 V). The circuit parameters were chosen as $I_{SS} = 90$ μA and $\nu_1 - \nu_2 = 100$ μV. I_{SS} was chosen as 90 μA because amplifier gain is almost constant even if I_{SS} is used with values over 90 μA [13]. The frequency response of the instrumentation amplifier under different control voltages is shown in Figure 5.

As shown in Figure 5, the bandwidth of the proposed circuit is strongly dependent on control voltage V_C, and differential gain is adjustable by the control voltage. The active resistor, R_A, can be approximately tuned from 7.4 KΩ to 33.2 KΩ for different control voltages. The simulated gains obtained for the above control voltages were 28.7 dB, 24.2 dB, and 22.2 dB, respectively.

Variation of parasitic resistance versus biasing current for the CCCII can be seen in Figure 6, which depicts the theoretical and simulation results. The theoretical calculation was performed using Eq. (3).

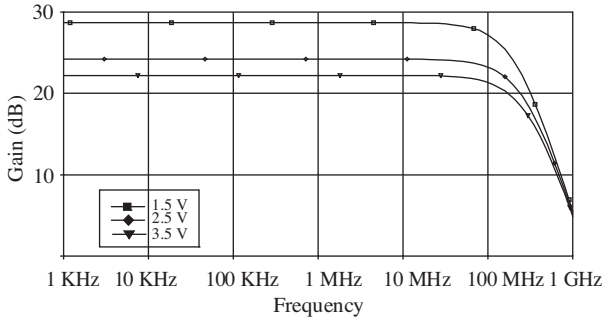

Figure 5. Frequency response of the instrumentation amplifier under different control voltages.

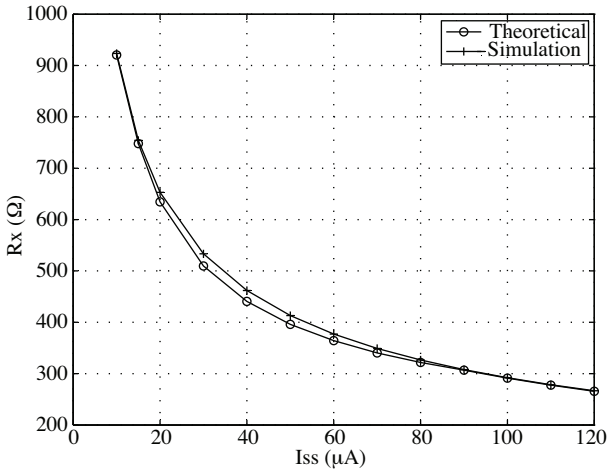

Figure 6. Variation of parasitic resistance versus biasing current for CCCII.

As shown in Figure 6, the simulation results approximately verified the theoretical consideration. The small difference between the curves was caused by a mismatch between the CMOS transistors. Parasitic resistance can be approximately tuned from 265 Ω to 920 Ω for different biasing currents.

Later, a simulation was operated under varying biasing currents, namely I_{SS1} and I_{SS2}. The circuit parameters were chosen as $V_C = 1.5$ V and $\nu_1 - \nu_2 = 100$ μV. The frequency response of the instrumentation amplifier under different biasing currents is shown in Figure 7.

The simulated gains obtained for the above bias currents were 16.7 dB, 21 dB, 25.4 dB, and 28.7 dB, respectively.

From Eq. (3), it is seen that the biasing current is inversely proportional to the square of parasitic resistance. As seen from Figure 6, as the biasing current increases, the bandwidth also increases [23]. The bandwidth is 70.1 MHz for a 16.7-dB gain.

The CMRR of the proposed circuit was investigated, and it was seen that it is dependent on both voltage transfer error ε_v and current transfer error ε_I. Eq. (17) indicates that the mismatch between the current conveyors should be reduced due to the fact that a high CMRR is generally obtained. To simulate the CMRR of the proposed circuit in Figure 2, it is applied to the same input voltage (100 μV).

The CMRR frequency response of the instrumentation amplifier is shown in Figure 8.

In Figure 8, it is seen that the CMRR of the instrumentation amplifier has a high value. The CMRR magnitude obtained by the simulation was 142 dB for low frequency and remained as high as 51 dB at 8 MHz. The CMRR was obtained as a function of frequency for differential voltage gains of 16.7 dB, 21 dB, 25.4 dB, and 28.7 dB, respectively. A comparison between the proposed circuit and those of different studies is given in Table 2.

As shown in Table 2, for some circuits in the literature, the CMRR and bandwidth, which are 2 important characteristics of instrumentation amplifiers, can be considered poor. If the proposed circuit is compared with [17], Bruun's amplifier has many passive resistors with a complex circuit structure. Bruun's circuit was also designed using bipolar junction transistors. It is shown in [18] that the small bandwidth of Azhari's amplifier may be taken as a drawback. It should also be mentioned that our topology exhibits a larger CMRR than Azhari's amplifier throughout the frequency response, although Azhari also investigated the circuit experimentally. If

our circuit is compared with that of Tekin et al. [19], it can be seen that our amplifier has a larger CMRR and CMOS technology. Additionally, the proposed amplifier is controllable by both voltage and current, while the amplifier designed by Tekin et al. is only controllable by current. The proposed circuit, shown in the last line Table 2, offers a considerable improvement in some requirements of the instrumentation amplifier.

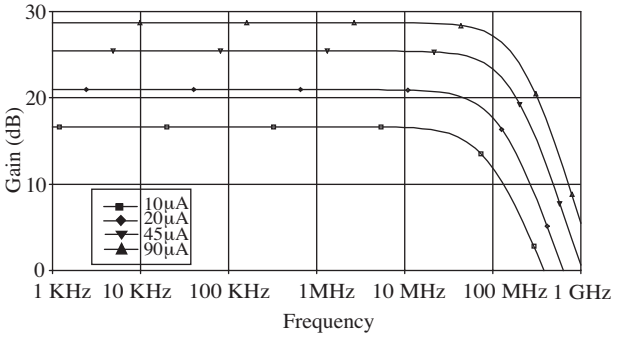

Figure 7. Frequency response of the instrumentation amplifier under different biasing currents.

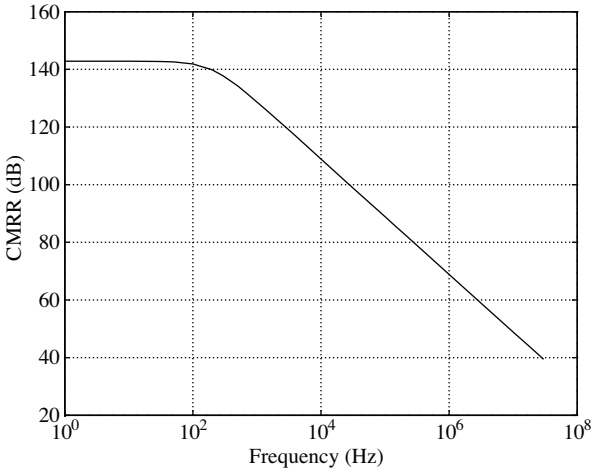

Figure 8. CMRR frequency response of the instrumentation amplifier.

Table 2. Comparison between some instrumentation amplifier characteristics.

Study	V_S (V)	CMRR (dB)	Bandwidth (MHz)	**Gain**	TPD (μW)	Control function	Structure	Passive component
[4]	±2.5	147	11	-	-	Current	BJT*	No
[15]	-	76	1.2	10	-	Passive resistor	BJT	Yes
[18]	-	95	592×10^{-3}	29	-	Passive resistor	BJT	Yes
[19]	±2.5	102	70	-	-	Current	BJT	No
[24]	±2.5	127	110×10^{-6}	1778	110	-	CMOS	Yes
[25]	±3	93.2	740×10^{-3}	200	285	-	CMOS	Yes
[16]	±1.5	-	8	-	1740	Passive resistor	CMOS	Yes
This study	±3.3	142	70	45	519	Voltage or current	CMOS	No

*BJT: bipolar junction transistor

5. Conclusion

In this study, a new approach to the design of an instrumentation amplifier, which consists of 2 CMOS CCCIIs and an active resistor, was introduced. The proposed circuit was implemented in standard 0.35-μm CMOS technology and has no passive component, which is attractive for integrated circuit implementations. The proposed circuit was simulated using a PSpice simulation program. Theoretical analysis was carried out, and the performance of the block circuit was confirmed through PSpice simulation results. The simulation results were compared with characteristics of some other instrumentation amplifiers in the literature. The circuit has a higher CMRR and wider bandwidth than other topologies. The gain of the circuit is electronically adjustable in current or voltage form. Finally, the proposed circuit, which is controllable by biasing current and control

voltage, could be used as a part of many sensitive biomedical applications that particularly require a high CMRR.

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