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Microelectronic interconnect modeling with a periodical lumped RLC-network

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Abstract: A modeling of high-speed microelectronic interconnections based on periodical resistor-inductor-capacitor (RLC) cells is presented in this paper. A theoretical investigation enabling one to determine the interconnect structure transfer function is established. The proposed theory is based on the use of the ABCD matrix product of elementary cells, constituting the whole interconnect structure. After extracting the constituting lumped elements R, L, and C, which model the considered interconnection, examples of the numerical validations were proposed, both in the frequency and time domains. It was demonstrated that by considering a structure comprised of 10 elementary segments in cascade, S-parameters and time-domain results were perfectly well correlated with the microstrip interconnection electromagnetic/circuit cosimulations performed with SPICE. It was verified that by considering input square wave data with several Gigasymbols/s rates, the introduced method enables the achieving of relative errors lower than 1% when the number of used cells is higher than 10. In addition, the sensitivity of the model in the function of the interconnect line length is investigated. The proposed model permits one to accurately predict the behavior of radio frequency/microelectronic interconnection responses for different signal integrity parameters of the interconnection line load values.

Key words: Discrete modeling method, high-speed interconnections, microelectronic application, RLC-model, signal integrity

1. Introduction

Mankind's society and way of life have become more and more dependent on electronic equipment. This technological dependence manifests in particular with the strong needs of personal computers at work, mobile phones (2.5 G, 3 G, and 4 G) anytime and anywhere around the world, and the boom of video games [1,2]. This modern daily habit change creates a motivation source for microelectronic industries to improve without limit the technical performances of their products. According to the International Technology Roadmap for Semiconductors reports [3,4], this development can be evaluated mainly by the decrease of device feature sizes and the increase of the operating data speed. This renders the microelectronic system interconnections to be more and more complex.

With several Gigasymbols/s (Gsps) rates of operating data in modern microelectronic systems [5–9], interconnection influences can create severe malfunctioning of electronic systems. In fact, interconnection lines are susceptible to generating significant delays and losses, which can be a source of signal desynchronization at different stages of microelectronic systems, such as in clock tree networks [10–12]. To overcome this problem,

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deep investigations on signal integrity (SI) propagating in interconnection networks have been conducted [13–18]. Moreover, methods enabling the improvement of the performance optimization were also proposed [19,20]. Until now, most of the existing methods have been based on first-order [10,21,22] or second-order [23–27] polynomial approximations of the interconnection transfer functions. In order to enhance the signal quality, an equalization method based on the use of negative group delay circuits was also introduced [28–30]. The interconnect models are generally considered and implemented for the approximation of the SI parameters, such as signal delays, rise-time, and over-/under-shoots, as well as the attenuation. However, in certain use cases, because of the increase of the operating signal bandwidth, the second-order models of the interconnection networks are not sufficient. To alleviate this limitation, further technique solutions are necessary. As an illustration, let us consider the interconnection system comprising a transmission line (TL) with a characteristic impedance Z_c, propagation constant γ, and physical length d, driven by a voltage source v_i and loaded by an impedance Z_L, represented in Figure 1. The voltage across the output load of this circuit is denoted as v_o.

In order to investigate the integrity of mixed or analog digital signals propagating through the interconnection system, authentic and confident knowledge about the analytical behavior of the equivalent transfer function is indispensable. This allows for the extraction of different time-domain parameters and, in particular, the mathematical expression appropriated to the interconnection system unit step response. For that, in this paper, it is proposed to proceed with the theoretical analysis based on the exploitation of the equivalent ABCD matrix of each elementary block (TL in cascade with a shunt impedance Z_L) constituting the overall system shown in Figure 1a. The equivalent model of the TL, including the distributed infinite cells in cascade with an infinitesimal small length δx, is depicted in Figure 1b (here the integer $k < n$).

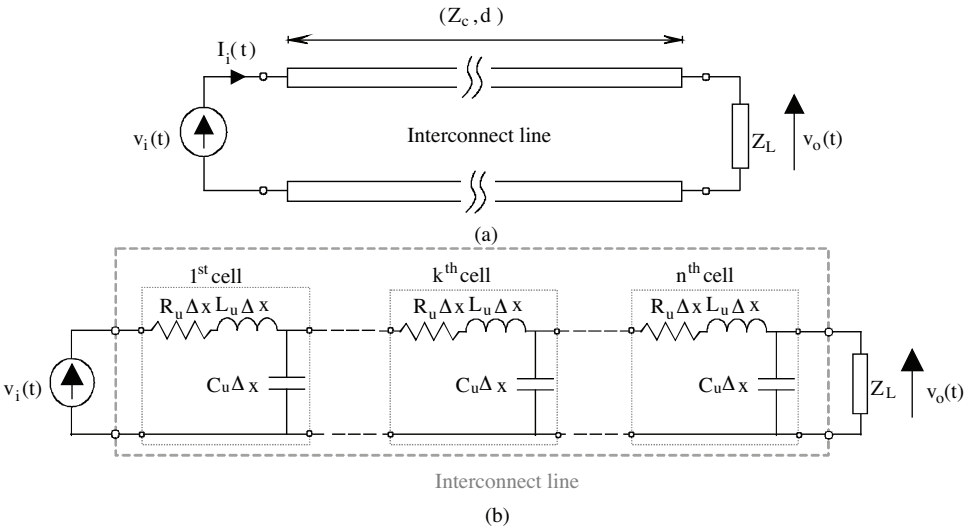

Figure 1. Interconnect line with characteristic impedance Z_c and physical length d, driven by a voltage source v_i and loaded by Z_L: a) overall system, b) equivalent model of TL.

In fact, the elaboration of the SI parameters of the distributed interconnect system under study, from its own transfer function expressed in Eq. (1) [31], is mathematically very complicated.

$$T(s) = \frac{V_o(s)}{V_i(s)} = \frac{Z_L}{Z_L \cosh(\gamma \cdot d) + Z_c \sinh(\gamma \cdot d)}, \tag{1}$$

where $\gamma = \alpha + j.\beta$ represents the propagation constant of the TL as defined in [31]. For this reason, a characterization method based on the discrete model of the interconnection line constituted by periodical lumped resistor-inductor-capacitor (RLC) cells is introduced in this article. For clarity, this paper is organized into 3 different sections. Section 2 develops the theoretical analysis of the periodical structure composed of lumped RLC-network. In this case, the formulations enabling extraction of the parameters R, L, and C of the interconnection lines, which can be assumed as a microstrip interconnection introduced in [32], are used. To verify the effectiveness of the proposed theoretic concepts, validation results are presented in Section 3. The last section is the conclusion of the paper.

2. Theoretical investigation

According to the current microelectronic applications with the operating data of certain Gsps rates [3,4,6,27,31,32], the per unit length conductance parameter G_u of the interconnect TL is usually negligible. For this reason, in this paper, we propose to exploit the discrete modeling method limited to the periodical RLC network shown in Figure 2. This circuit is formed by n elements of identical discrete RLC cells in cascade, which are constituted by lumped circuits with total resistance $R = R_u\Delta x$, inductance $L = L_u\Delta x$, and capacitance$C = C_u\Delta x$ for the piece physical length $\Delta x = d/n$. R_u, L_u, and $C_u$are the per unit length parameters of the interconnect TL. Logically, the higher the integer of the number of cells n, the more accurate the discrete model is.

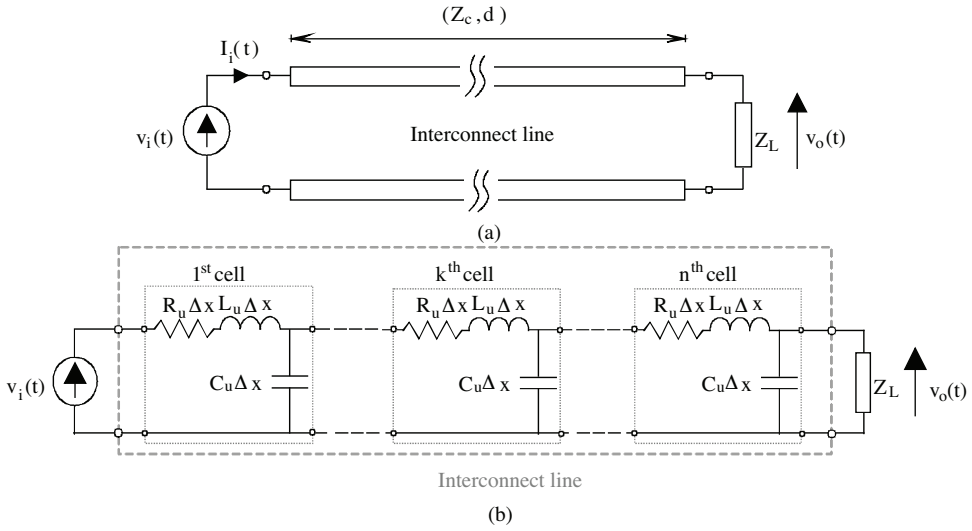

Figure 2. The proposed discrete model formed by n segment element cells of a periodical lumped RLC cell with total resistance $R = R_u\Delta x$, inductance $L = L_u\Delta x$, and capacitance $C = C_u\Delta x$.

To strategically analyze the network introduced in Figure 2, let us consider the periodical network comprising n identical L-cells in cascade having an ABCD matrix written as shown below.

$$[M_{RLC}] = \begin{bmatrix} 1 + (R + L \cdot s) \cdot C \cdot s & R + L \cdot s \\ C \cdot s & 1 \end{bmatrix} = \begin{bmatrix} 1 + (R_u + L_u \cdot s) \cdot C_u \cdot (\Delta x)^2 \cdot s & (R_u + L_u \cdot s) \cdot \Delta x \\ C_u \cdot \Delta x \cdot s & 1 \end{bmatrix} \tag{2}$$

Here, s is the Laplace variable. According to the circuit and system theory, the ABCD matrix of the circuit, consisting of n RLC cells in cascade, can be written as the following matrix product:

$$[M(n)] = \prod_{k=1}^{n} [M_{RLC}] = \prod_{k=1}^{n} \begin{bmatrix} 1 + (R + L \cdot s) \cdot C \cdot s & R + L \cdot s \\ C \cdot s & 1 \end{bmatrix}. \tag{3}$$

It is important to note that the expression of $[M_{RLC}]$ does not depend on parameter k because the elementary RLC cells constituting the TL are identical. For simplification, we denote:

$$[M(n)] = \begin{bmatrix} M_{11}(n) & M_{12}(n) \\ M_{21}(n) & M_{22}(n) \end{bmatrix}. \tag{4}$$

Hence, it can be demonstrated that the recursive expressions connecting the 4 elements comprising the consecutive matrices $[M(n)]$ and $[M(n+1)]$ are expressed by:

$$M_{11}(n+1) = [1 + (R + L \cdot s) \cdot C \cdot s]\, M_{11}(n) + C \cdot s \cdot M_{12}(n), \tag{5}$$

$$M_{12}(n+1) = (R + L \cdot s) \cdot M_{11}(n) + M_{12}(n), \tag{6}$$

$$M_{21}(n+1) = [1 + (R + L \cdot s) \cdot C \cdot s]\, M_{21}(n) + C \cdot s \cdot M_{22}(n), \tag{7}$$

$$M_{22}(n+1) = (R + L \cdot s) \cdot M_{21}(n) + M_{22}(n), \tag{8}$$

where the 4 elements constituting the initial matrix $[M_1]$ are also the ABCD matrix of the elementary RLC cell:

$$\begin{cases} M_{11}(1) = 1 + (R + L \cdot s) \cdot C \cdot s \\ M_{12}(1) = R + L \cdot s \\ M_{21}(1) = C \cdot s \\ M_{22}(1) = 1 \end{cases}. \tag{9}$$

In this case, the total ABCD matrix of the whole RLC-network shown in Figure 2 should be calculated analytically from the following matrix product:

$$[M_T(n)] = \prod_{k=1}^{n} [M_{RLC}] \times \begin{bmatrix} 1 & 0 \\ \frac{1}{Z_L} & 1 \end{bmatrix} = \begin{bmatrix} M_{T11}(n) & M_{T12}(n) \\ M_{T21}(n) & M_{T22}(n) \end{bmatrix}. \tag{10}$$

Substituting the expression in Eq. (3) into the latter matrix relation, one gets the relations between the elements of the whole matrix $[M_T(n)]$ and those of the ABCD matrix $[M(n)] = \prod_{k=1}^{n} [M_{RLC}]$ are defined as:

$$M_{T11}(n) = M_{11}(n) + \frac{M_{12}(n)}{Z_L}, \tag{11}$$

$$M_{T12}(n) = M_{12}(n), \tag{12}$$

$$M_{T21}(n) = M_{21}(n) + \frac{M_{22}(n)}{Z_L}, \tag{13}$$

$$M_{T22}(n) = M_{22}(n). \tag{14}$$

According to the circuit and system theory, the transfer function is the inverse of the first element of the ABCD matrix. This means that the transfer function of the system under study can be written as:

$$T_n(s) = \frac{1}{\frac{1}{T_{0n}(s)} + \frac{M_{12}(n)}{Z_L}}, \tag{15}$$

where $T_{0n}(n)$ is the transfer function of the open-ended periodical RLC network, comprising n elements in cascade. The recursive relation of the transfer function of the open-ended discrete RLC-line is given by:

$$T_{0(n+1)}(s) = \frac{1}{\frac{1+(R+L\cdot s)\cdot C\cdot s}{T_{0n}(s)} + C\cdot s\cdot M_{12}(n)}. \tag{16}$$

For example, by assuming the load as a resistance R_L in parallel with a capacitance C_L, analytically expressed as $Z_L(s) = R_L/(1 + R_L \cdot C_L \cdot s)$, the global transfer function of the circuit introduced in Figure 1 will become:

$$T_{n+1}(s) = \frac{1}{\frac{1+(R+L\cdot s)[C\cdot s+(1+R_L\cdot C_L\cdot s)/R_L]}{T_n(s)} - \frac{(R+L\cdot s)(1+R_L\cdot C_L\cdot s)[1+R_L\cdot(C+C_L)\cdot s]}{R_L^2}M_{12}(n)}, \tag{17}$$

where the initial value is:

$$T_1(s) = \frac{1}{1 + \frac{R}{R_L} + (C + C_L)\cdot R\cdot s + (C + C_L)\cdot L\cdot s^2}. \tag{18}$$

As the interconnect circuit under study is constituted by elementary R-, L-, and C-linear passive networks, the global transfer function must behave as a linear polynomial function written as:

$$T_{n0}(s) = \frac{1}{c_0(n) + c_1(n)s + c_2(n)s^2 + ... + c_n(n)s^n}, \tag{19}$$

where $c_k(n)$ $(k = \{1\ldots n\})$ are real coefficients depending on the periodical RLC network parameters. We can remark that this interconnect system transfer function can be considered for determining the frequency- and time-domain responses of the system in a simple way compared to the relation introduced in Eq. (1). One can establish the recursive relations between the element coefficients of the ABCD matrix $[M(n)]$ using this polynomial relation:

$$M_{pq}(n) = \sum_{k=0}^{n} c_{pq,k}(n)\cdot s^k, \tag{20}$$

where $c_{pq,k}(n)$ with $(p,q) = \{(1,1), (1,2), (2,1), (2,2)\}$ and $k = \{1\ldots n\}$. For example, the first 2 coefficients are given by the recursive formulae:

$$c_{11,2}(n) = c_{11,2}(n-1) + R\cdot C\cdot c_{11,1}(n-1) + L\cdot C\cdot c_{11,0}(n-1) + C\cdot c_{12,1}(n-1), \tag{21}$$

$$c_{12,1}(n) = R\cdot c_{11,1}(n-1) + L\cdot c_{11,0}(n-1) + c_{12,1}(n-1), \tag{22}$$

$$c_{12,2}(n) = R\cdot c_{11,2}(n-1) + L\cdot c_{11,1}(n-1) + c_{12,2}(n-1), \tag{23}$$

$$c_{21,2}(n) = c_{21,2}(n-1) + R\cdot C\cdot c_{21,1}(n-1) + L\cdot C\cdot c_{21,0}(n-1) + C\cdot c_{22,1}(n-1), \tag{24}$$

$$c_{22,1}(n) = R \cdot c_{21,1}(n-1) + L \cdot c_{21,0}(n-1) + c_{22,1}(n-1), \tag{25}$$

$$c_{22,2}(n) = R \cdot c_{21,2}(n-1) + L \cdot c_{21,1}(n-1) + c_{22,2}(n-1). \tag{26}$$

By identification with the matrix expression shown in Eq. (2), we obtain the following definition of the initial parameters:

$$\begin{cases} c_{11,0}(1) = 1, c_{11,1}(1) = R \cdot C, c_{11,2}(1) = L \cdot C \\ c_{12,0}(1) = R, c_{12,1}(1) = L, c_{12,2}(1) = 0 \\ c_{21,0}(1) = 0, c_{21,1}(1) = C, c_{21,2}(1) = 0 \\ c_{22,0}(1) = 1, c_{22,1}(1) = 0, c_{22,2}(1) = 0 \end{cases} . \tag{27}$$

In order to confirm the relevance of this theoretic concept, in Section 3, analysis of an example of the application based on the numerical experiment of the microstrip interconnection line is proposed.

3. Verification results

Figures 3a and 3b represent the circuit diagram of the interconnection system under study. It is essentially composed of a microstrip line printed on FR4-epoxy substrate characterized by a relative permittivity of $\varepsilon_r = 4.4$ and thickness of 0.8 mm. The metallization consists of a copper conductor with a thickness of 35 μm and a geometrical width defined in the next part, denoted w, and physical length equal to $d = 3$ mm. This interconnection line is driven by a high rate voltage source representing the mixed data and is loaded with an impedance formed by resistance R_L and capacitance C_L connected in parallel.

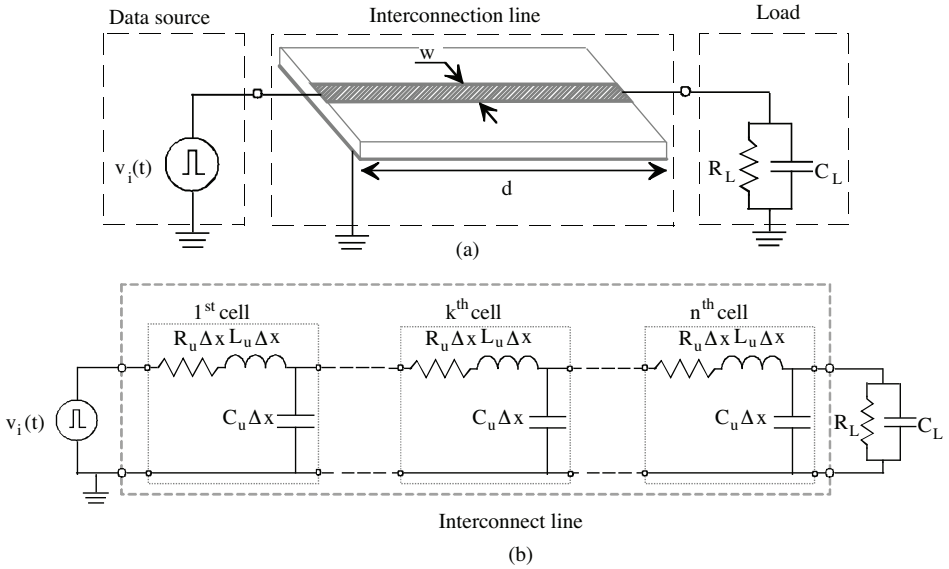

Figure 3. a) Diagram of the interconnection circuit under study, comprising a microstrip line driven by a square wave source and loaded by RC parallel impedance, and b) the considered equivalent circuit.

By applying the calculation method reported in [31,32], with various values of width $w = \{50\ \mu$m, 100 μm, 150 μm, and 200 μm$\}$, we determined the per unit length parameters R_u, L_u, and C_u. Therefore, one gets the results summarized in the Table [31,32]. The resistance and inductance TL per unit length parameters increase with the interconnect metallization width and inversely for the capacitance.

Table. Per unit length parameters extracted from the tested microstrip line for various values of the width w.

w	R_u	L_u	C_u
50 μm	111.8 Ω/m	1.00 μH/m	30.7 pF/m
100 μm	74.6 Ω/m	0.90 μH/m	34.6 pF/m
150 μm	57.6 Ω/m	0.83 μH/m	37.7 pF/m
200 μm	47.4 Ω/m	0.79 μH/m	40.3 pF/m

By employing these extracted parameters, comparisons were made between the frequency- and time-domain computations with the ADS SPICE and Momentum environments from Agilent^{TM}. Hence, the interesting results exposed in the next paragraphs are obtained.

3.1. Frequency verifications

It is worth noting that the microstrip line under study is supposed to be used in the context of high-speed mixed or digital-analog data. In this case, the digital data exciting the interconnect line under study can be assumed as an analog baseband signal delimited by the frequency f_{lim} inversely proportional to its rise/fall times t_r, expressed as [32]:

$$f_{\lim} = \frac{0.35}{t_r}. \tag{28}$$

Analytically, this means that for the microelectronic applications operating around some Gsps, the considerable analog bandwidth of the input signals is limited to about 6 GHz. In other words, the effectiveness of the model proposed can be validated up to the frequency given by f_{lim}.

Hence, the relevance of the proposed discrete model can be evaluated via S-parameter simulations in baseband frequencies of up to 6 GHz for different values of the metallization width w. The TL was tested with electromagnetic (EM)/circuit cosimulations. These simulations consist of the global simulation of the structure shown in Figure 3 using the full-wave EM S-parameters model of the microstrip line computed in the Momentum environment of ADS. As a consequence, by considering a discrete model comprising $n = 10$ RLC cells in cascade, a very good agreement between the return loss S_{11} and the transmission loss S_{21} of the tested TL displayed in Figure 4 is realized. One can see that the TL loss is inversely proportional to the interconnect width w.

3.2. Time-domain analysis

To carry out this transient analysis, the interconnection network depicted in Figure 3 was excited by a square waveform pulse voltage having a normalized amplitude and time symbol duration $T = 200$ ps, which corresponds to a 5 Gsps rate. To take into account the practical imperfections of this high-speed signal generation, the rise/fall time of this data source was set at 20 ps. Next, comparisons were made between the transient responses from the EM/circuit cosimulation of the TL for $w = 100$ μm presented in Figure 3 and the lumped RLC networks comprising $n = 10$ RLC segments in cascade. After transient simulations were run from $t_{min} = 0$ to $t_{max} = 1$ ns, by varying the load resistance $R_L = \{100\ \Omega,\ 200\ \Omega,$ and $300\ \Omega\}$ via sweep cosimulations, the results are displayed in Figure 5.

The responses from the reference SPICE computation are plotted with a black dashed line and those computed from the proposed discrete RLC model are plotted in a gray solid line. Hence, once again, the transient responses from the transfer function model introduced in Section 2 are very well correlated to the EM/circuit cosimulations of the piece of microstrip interconnect TL.

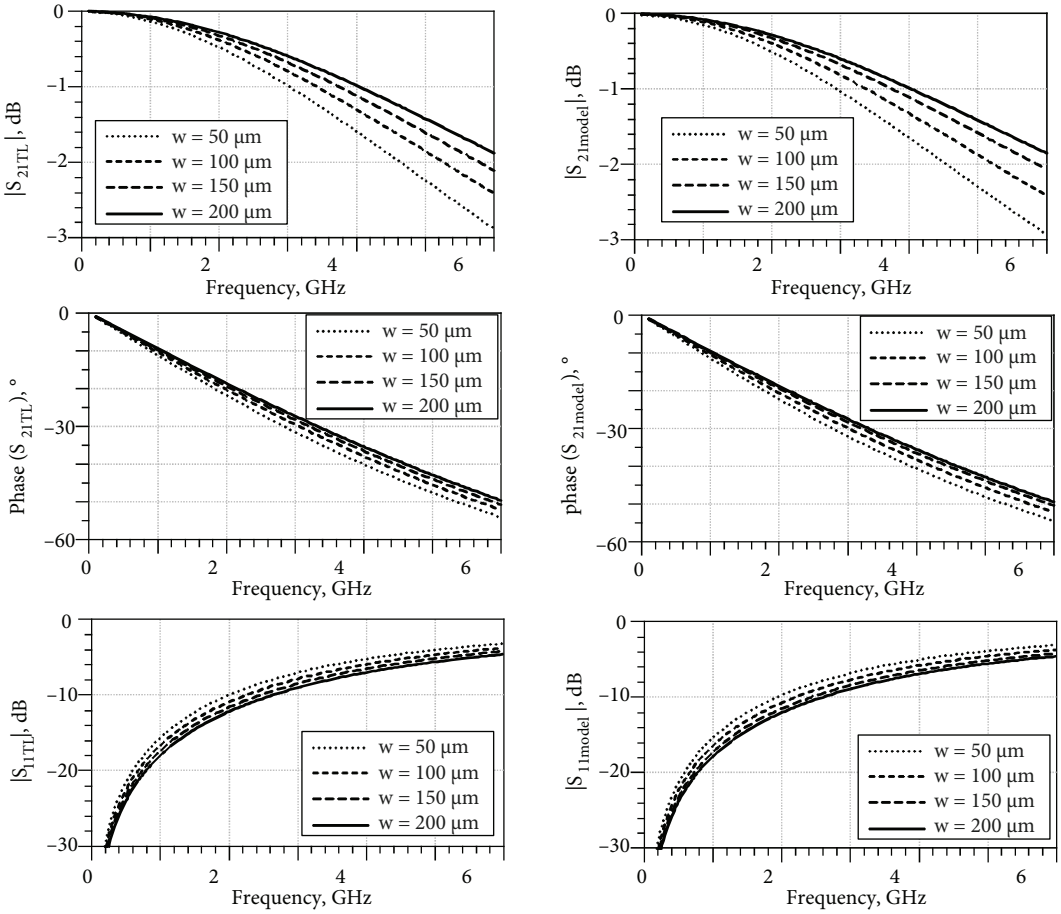

Figure 4. Comparison of the proposed model's S-parameters and those of the TL, depicted in Figure 3, for $w = \{50\ \mu\text{m}, 100\ \mu\text{m}, 150\ \mu\text{m}, \text{and } 200\ \mu\text{m}\}$.

One can remark that, as predicted in theory due the interconnection effects, the operating signal is completely degraded. One evaluates here relative errors of about 1%, which are, in fact, mainly due to the numerical inaccuracy. The same numerical investigations performed with various load capacitance values $C_L = \{0.5\text{ pF}, 2.5\text{ pF}, \text{and } 4.5\text{ pF}\}$ generate the transient results displayed in Figure 6. One can see that the obtained computation results are in very good agreement with the model proposed and the EM/circuit SPICE simulations. It is noteworthy that with the circuit under study, the quality of the analog/digital signal propagating through the interconnect line is more and more degraded when C_L increases.

According to this numerical test, we point out that the main novelty of the modeling method presented in this paper is based on its flexibility to operate in the frequency- and time-domains. It is shown with this realistic structure, composed of 3-dimensional interconnect, that compared to the full wave simulators, as in Momentum-ADS, the model developed is simpler and can be executed with 10 times less computation time.

3.3. Sensitivity of the proposed model in the function of the model segment number and the tested interconnect length

To achieve more conclusive numerical experiments about the accuracy of the proposed model, relative error analysis of the transient voltage responses in the function of the proposed model segment number for the

various values of w is proposed in this paragraph. For that, unit step source data with a rise time of about 10 ps were injected into the circuit under study. By taking arbitrary values of the load impedance (R_L = 100 Ω and C_L = 1 pF), and for the physical length d = 5 mm, the results plotted in Figure 7 are obtained. It is worth noting that the transient responses from the proposed model converge rapidly to the reference results, which is considered as absolutely achieved for an infinity of cells in cascade when n = 15.

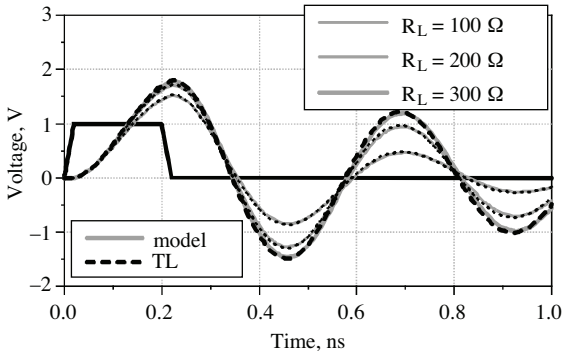

Figure 5. Transient responses for the input data: R_L = {100 Ω, 200 Ω, and 300 Ω}, C_L = 2 pF, and w = 100 μm.

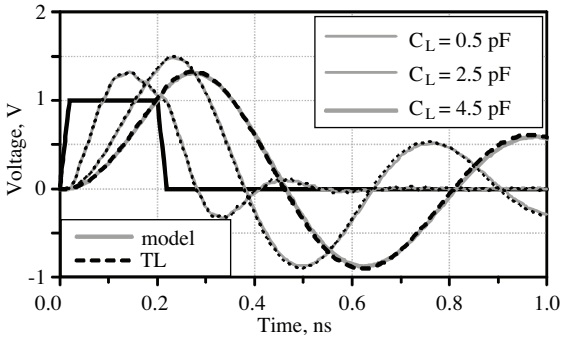

Figure 6. Transient responses for T = 0.2 ns, R_L = 100 Ω, C_L = {0.5 pF, 2.5 pF, and 4.5 pF}, and w = 100 μm.

For different values of the metallization width w, the transient results present relative errors lower than 1% when n is higher than 10. As illustrated in Figure 8, it can be underlined that the proposed model presents relative errors lower than 4% when the TL length d is varied between 1.5 mm and 17 mm.

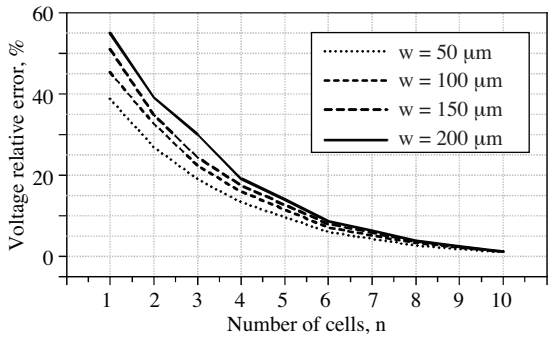

Figure 7. Relative errors of the unit step transient responses for n varied from 1 to 10.

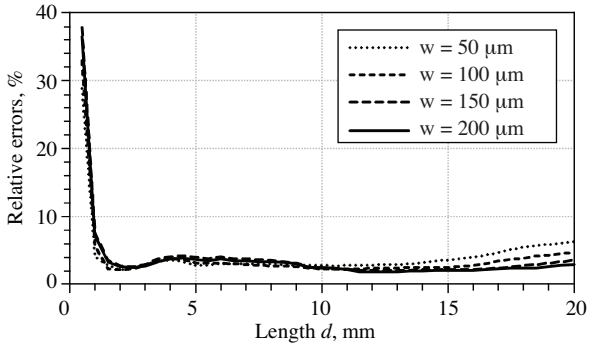

Figure 8. Relative errors of unit step transient responses for d varied from 0.5 mm to 20 mm.

Moreover, one can see that the sensitivity is higher when the width w is lower. It is interesting to note that the accuracy of the model versus d depends also on the rise time of the operated signal data.

4. Conclusion

An efficient modeling technique of the microelectronic interconnection lines dedicated to high-speed operating data processing up to the microwave frequencies is presented. Due to the complexity growth of the TL transfer function expressions, it becomes very difficult to determine the exact formulation of the transient responses of the interconnection networks in integrated microelectronic systems. To pass this technical limitation, a discrete model composed of periodical lumped RLC cells in cascade is introduced, investigated analytically, and validated

numerically in this paper. Theoretic analysis enabling one to establish the equivalent polynomial formula of the transfer function in the function of the considered RLC cell number, connected in cascade, is developed. To verify the relevance of the theory, validations with EM/circuit cosimulations regarding a millimeter microstrip line were performed. As a result, very good agreement between the S-parameters of the proposed model and the tested millimeter microstrip line is found in baseband frequencies of up to 6 GHz. In addition, transient analyses with various parameters of the considered interconnection load are realized. Therefore, results presenting almost negligible relative errors are obtained when the number of cells is very high. The presented numerical analysis also shows that the precision of the method in the function of the cell numbers in cascade is better than 1% when the number of discrete RLC cells is higher than 10. These numerical results confirm the method's usefulness notable for the SI prediction.

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