

## A 5-bit 5 Gs/s flash ADC using multiplexer-based decoder

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**Abstract:** This paper presents a 5-bit flash analog-to-digital converter design using the 0.18- $\mu$ m Taiwan Semiconductor Manufacturing Company's CMOS technology library. The designed system consists of 2 main blocks, a comparator array, and a digital decoder. The digital decoder contains a latch, 1-of-N decoder, and fat-tree encoder units. The 1-of-N decoder is implemented using  $2 \times 1$  multiplexers. As a result, the active die area and the power consumption are reduced, in addition to an increase in the sampling frequency. The power supply voltage range for the overall system is  $\pm 0.9$  V. For testing purposes, a ramp signal of between  $-0.45$  V and  $0.7$  V is applied to the converter input. The sampling frequency is 5 Gs/s. The simulation results include a maximum power consumption of 28 mW, integral nonlinearity values of between  $-0.65$  least significant bits (LSB) and  $+0.01$  LSB, differential nonlinearity values of between  $-0.3$  LSB and  $+0.13$  LSB, and an active die area of  $0.1$  mm<sup>2</sup>.

**Key words:** Flash ADC, CMOS VLSI, high-speed data converters

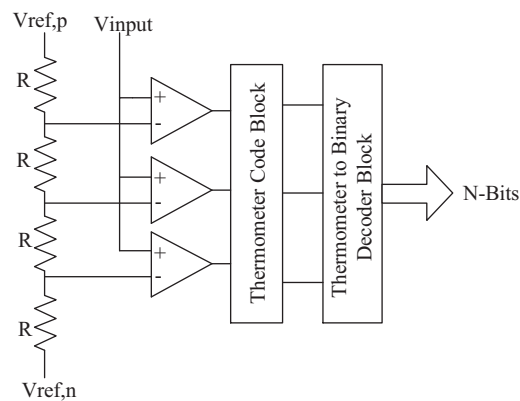
### 1. Introduction

Analog-to-digital converters (ADCs) are the most important core units to convert analog information to corresponding digital forms. This means that they can be considered as bridges between the real world and the digital world. ADCs are commonly used in the application areas of mobile phones, cameras, digital TVs, wireless sensor networks, transmitter and receiver circuits, and the conversion processes of the signals for base-band applications [1–4]. Flash ADC is known as the fastest type of ADC among designers. It has the most important role, especially for magnetic read channel applications, optical data recording, digital communication systems requiring a high data processing rate, and optical communication systems [5–8]. The fully parallel (full-flash) ADC architecture is depicted in Figure 1. In this scheme, the comparison processes, with all quantization levels, correspond to an instant analog input voltage level and are done simultaneously during only 1 cycle of the sampling clock signal. The 1st phase of the sampling clock is for sampling and the 2nd phase is for converting and obtaining output binary data [6]. This property makes the flash ADC the fastest one among the others.

The most effective role for ADC performance is played by analog blocks. The design constraints related to the conversion speed are mostly defined by the performances of these blocks, especially by the comparators used in flash designs.

The 2 well-known disadvantages for flash ADCs are their low resolution and higher power consumption due to a larger chip area when compared to other types of ADC architectures.

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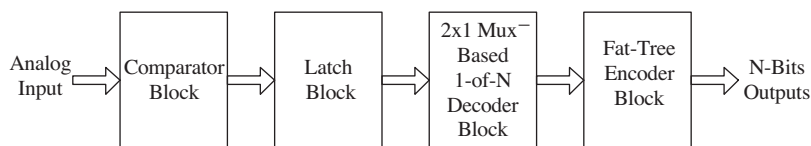
**Figure 1.** Flash ADC general architecture.

There are several flash ADC designs proposed in the literature. However, the 5-bit ADC, which is advertised in this study, is different than the others in terms of the subblocks employed in it. It can be considered as a case study, which employs different design schemes and methods advertised in the literature to be able to obtain a higher performance full-flash ADC. Finally, a fast and highly linear 5-bit flash ADC design implementation is achieved in the 0.18- $\mu\text{m}$  CMOS technology using the Cadence IC design platform. This paper is a revised version of the authors' earlier work [9].

The rest of the paper presents all of the design steps and related simulation results. The conclusion section compares the proposed ADC performance with similar designs from the literature.

**2. The 5-bit CMOS flash ADC design steps**

The block diagram of the proposed flash ADC is shown in Figure 2. It consists of a comparator block, latch block,  $2 \times 1$  MUX-based 1-of-N decoder block, and fat-tree-based encoder block.



**Figure 2.** The proposed flash ADC architecture.

**2.1. The comparator structure**

In the designed ADC system, the comparator schematic shown in Figure 3 is chosen [10]. The transistor aspect ratios and critical DC bias voltages used in the comparator circuit are also given in Figure 3 and Table 1, respectively. In this circuit, M2 and M3 are the N-type metal-oxide-semiconductor (NMOS) input differential pairs driven by the tail current transistor M4. The differential pair is loaded by diode-connected P-type metal-oxide-semiconductor (PMOS) transistors (M5–M6) and cross-coupled PMOS transistors (M0–M1), which serve as a positive feedback loop. The purpose of this feedback loop is to boost the differential voltage gain obtained by M2–M3 and to balance the output resistance. M9 and M10 form a current mirror and its reference current is provided by M5 and M7 together. The comparator's first-stage output is additionally amplified by a common-source PMOS amplifier (M8). The very last stage of the comparator is a basic CMOS inverter circuit (M11–M12). The DC analysis result of the complete comparator is shown in Figure 4, where it can be seen that a nice voltage comparison with almost zero input offset is obtained.

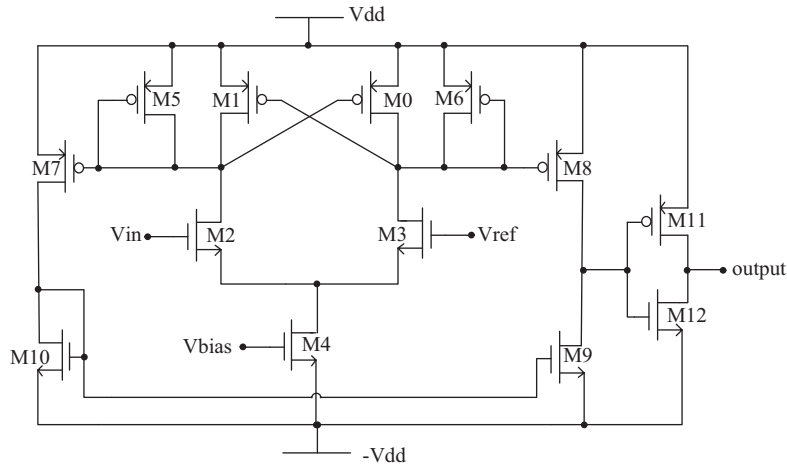


Figure 3. The comparator schematic [10].

Table 1. Transistor aspect ratios of the comparator schematic.

	W/L ( $\mu\text{m}$ )		W/L ( $\mu\text{m}$ )
M0	6/0.2	M6	6/0.2
M1	6/0.2	M7	6/0.2
M2	3/0.2	M8	6/0.2
M3	3/0.2	M9	2/0.2
M4	2/0.2	M10	2/0.2
M5	6/0.2	M11	6/0.2
M12	2/0.2		
Vbias	0.1 V		
Vref	0.9 V		

2.2. The latch circuit

The preferred dynamic latch circuit is depicted in Figure 5. The latch circuit either transfers the input logic level to the output (during which the clock signal is kept at logic ‘1’) or keeps the last output logic level (during which the clock signal is kept at logic ‘0’), depending on the controlling clock signal.

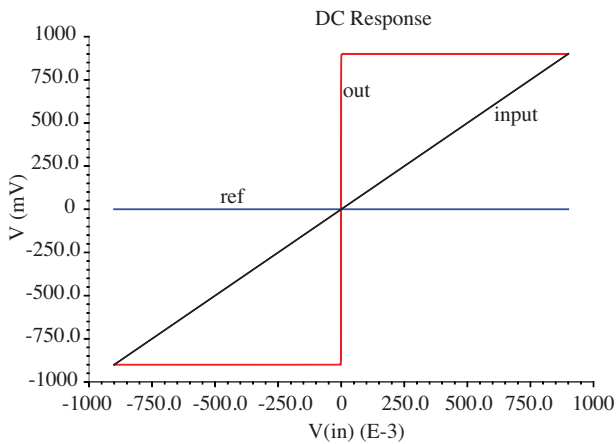


Figure 4. The DC analysis result of the comparator.

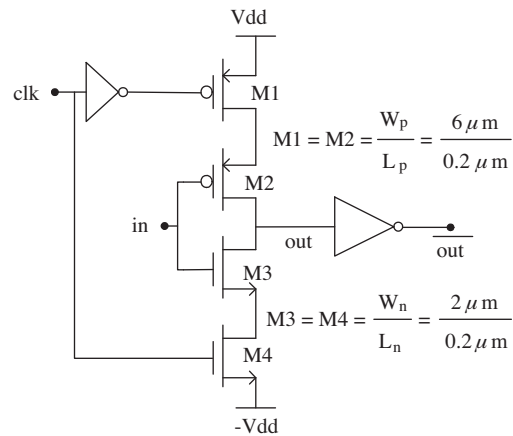


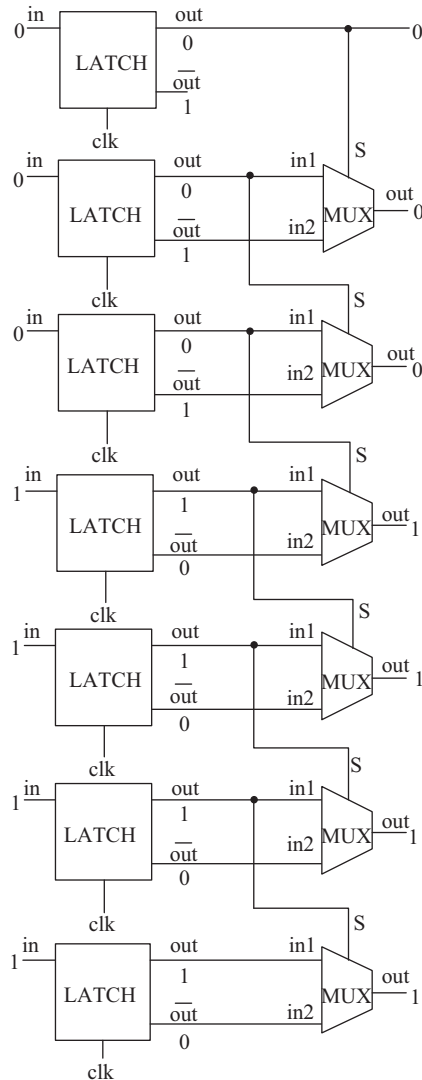
Figure 5. The dynamic latch circuit.

In other words, clock ‘0’ means a conversion phase and clock ‘1’ means a sampling phase. The control between the analog and digital parts of the ADC is obtained in this way [1].

In fact, it is not possible to convert an analog input level to its digital value instantly. A very small time period is necessary for the digital part to complete its job. Therefore, a dynamic latch circuit usage is inevitable for a flash ADC design. This time is called the ‘conversion time’, in general, and it is shortest in full-flash ADCs but is very long for the serial type of ADCs.

**2.3. The 1-of-N decoder block**

This decoder block converts the so-called thermometer code (TC) obtained from the outputs of the dynamic latch array to 1-of-N code. In fact, the TC is a good solution for low-resolution and high-speed converters, but the error rate increases while the resolution and speed increases [11]. The multiplexer-based decoder was also proposed in the literature [11]. The 1-of-N decoder structure used in the design is shown in Figure 6.



**Figure 6.** The conceptual circuit of the 1-of-N decoder block (3-bit case only).

Figure 7 shows the transmission gate-based multiplexer circuit used in the decoder. In the decoder,  $2 \times 1$  multiplexers are used. The multiplexer inputs are tied to their corresponding latch outputs, where both the normal and inverted forms of the TC segments are available at the same time.

Normal latch output terminals are connected to the 1st inputs of the multiplexers, while the inverted outputs are connected to the 2nd inputs. For a specific decoder row, the output of the upper row latch block is also tied to the lower row multiplexer’s select input, as seen in Figure 6. As a result, the TC is converted to 1-of-N code.

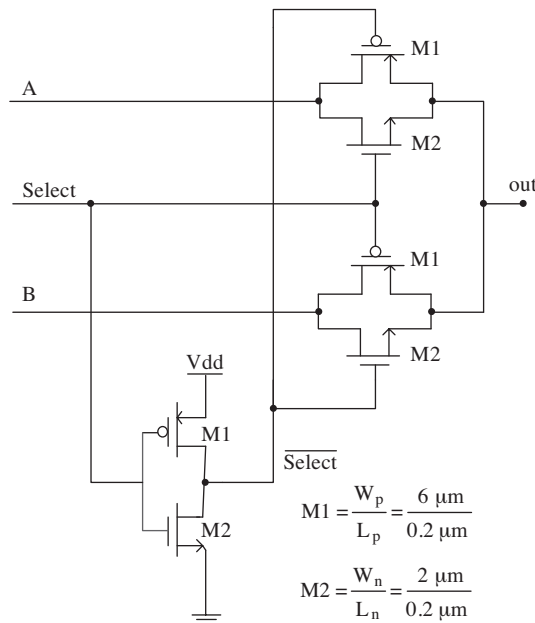


Figure 7. The  $2 \times 1$  multiplexer circuit.

**2.4. Fat-tree encoder structure**

As is known, the TC is obtained from analog comparator array outputs in flash ADC designs. Programmable logic array–read-only memory, exclusive OR encoder, or Wallace-tree encoder structures are generally used to convert TC to binary code [12,13].

The ADC designs advertised in [12–14] suggest the usage of the fat-tree encoder structure instead, which results in a higher sampling rate and lower power consumption due to a reduction in the number of logic gates required for the digital part of ADCs. Therefore, a fat-tree encoder structure is preferred in our case study, as well, which can be seen in Figures 8a, 8b, and 8c. The OR blocks in our encoder are designed using static CMOS technology.

Note that in Figure 8c, the inputs labeled as I0 to I31 are the outputs obtained from the 1-of-N decoder block to be applied to the fat-tree encoder inputs. The inputs in Figures 8a and 8b are connected to the corresponding input/output nodes in Figure 8c. As a result, 5 bits of binary output data from bit0 to bit4 are obtained.

**3. Simulation results**

The Cadence IC5141 design platform and North Carolina State University’s design kit with a 0.18-μm CMOS library are used during the design and simulations. A ramp-shaped analog input signal of between –0.45 V and

0.7 V, at a 10 MHz frequency, is applied to the ADC input for transient analysis. The clock frequency applied to the latch block is 5 Gs/s. Figure 9 shows the DC analysis results and Figure 10 shows the corresponding linearity plots [differential nonlinearity (DNL) and integral nonlinearity (INL)]. To be able to obtain the linearity plots, the DC results are transferred to a MATLAB platform, as used in [15].

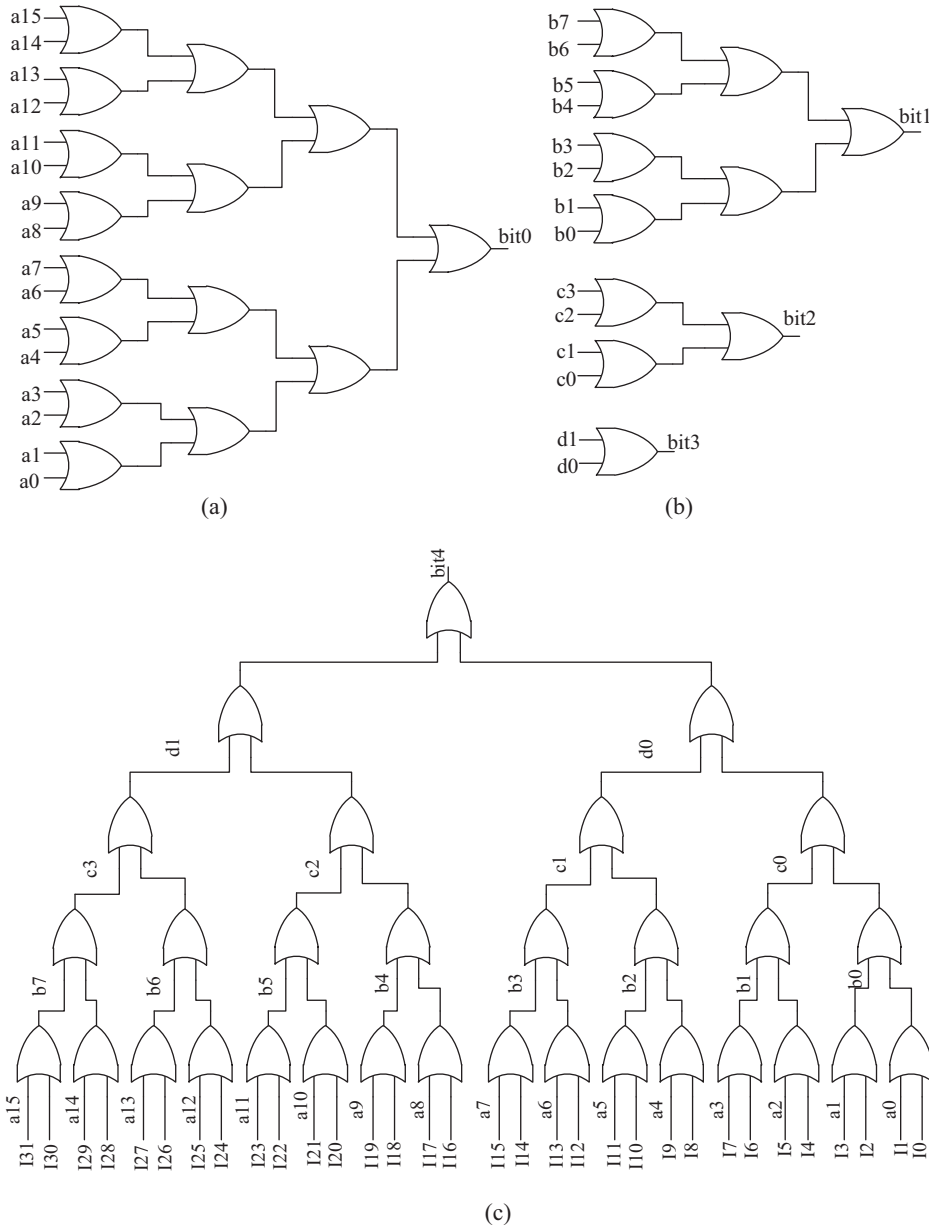


Figure 8. Fat-tree encoder schematic for the 5-bit case.

Figures 11 and 12 show the transient analysis results including DNL and INL plots for a 10-MHz input signal under digital clock frequency of 5 Gs/s. According to the transient simulation results, the worst-case INL is  $-0.65$  least significant bits (LSB) and the worst-case DNL is  $-0.3$  LSB.

Moreover, a 5 Gs/s clock is kept constant but the input frequency is changed. The corresponding DNL and INL plots with respect to the input frequency are also examined. In Figures 13 and 14, only the worst-case

linearity error values are plotted for specific frequency values. Additionally, the average current values drawn by the partial system blocks are tabulated in Table 2. As was expected, the largest current is drawn by the comparator block (a total of 31 comparators), which is about 10 mA. Table 3 shows the transistor count of the designed system blocks. Figure 15 shows the reconstructed output signal for an analog ramp input signal without filtering.

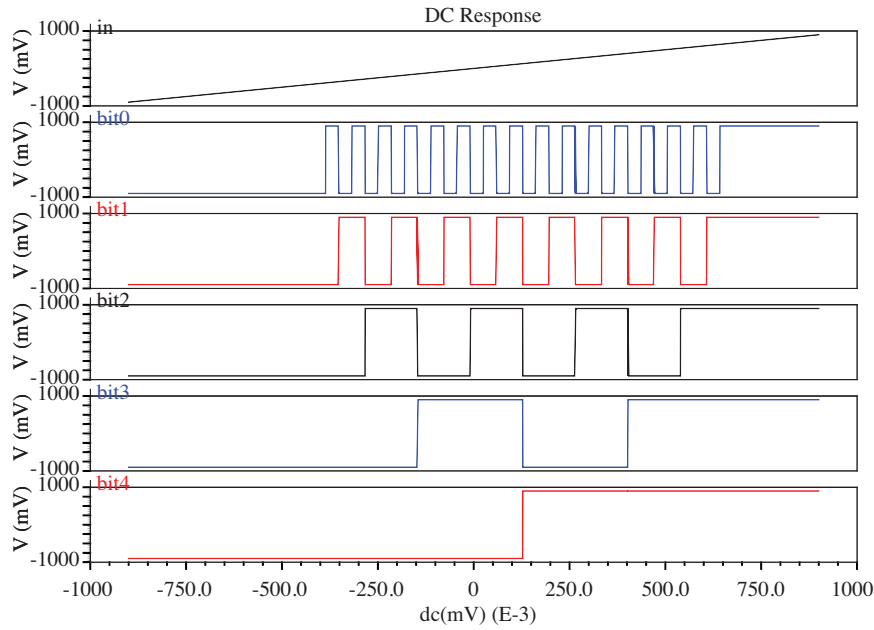


Figure 9. The 5-bit DC simulation results.

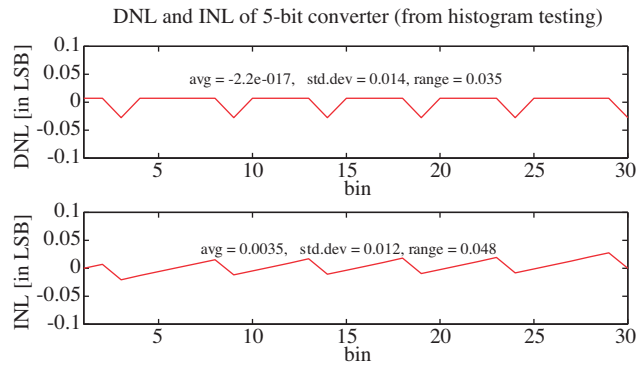


Figure 10. DNL and INL plots based on the DC simulations.

Table 2. The average current values of the partial system blocks.

Block name	Current values
Comparator array	9.927 mA
Latch array plus 1-of-N decoder	5.291 mA
Fat-tree encoder block	430.6 $\mu$ A

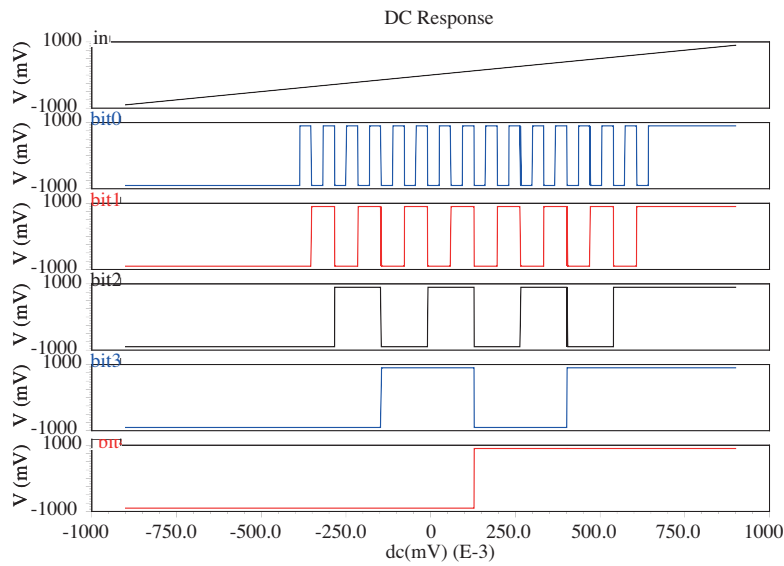


Figure 11. Binary output data waveforms for  $f_{in} = 10$  MHz ramp input signal.

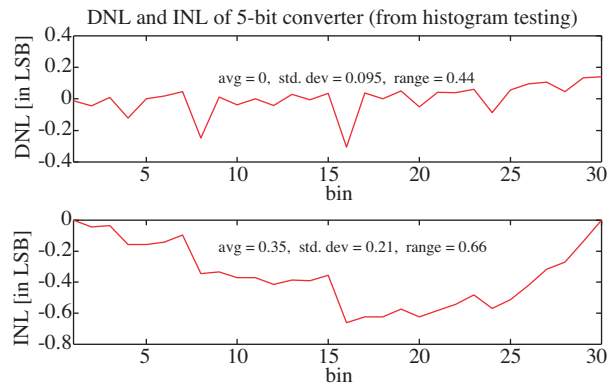


Figure 12. DNL and INL plots for the  $f_{in} = 10$  MHz/ $f_{clk} = 5$  Gs/s.

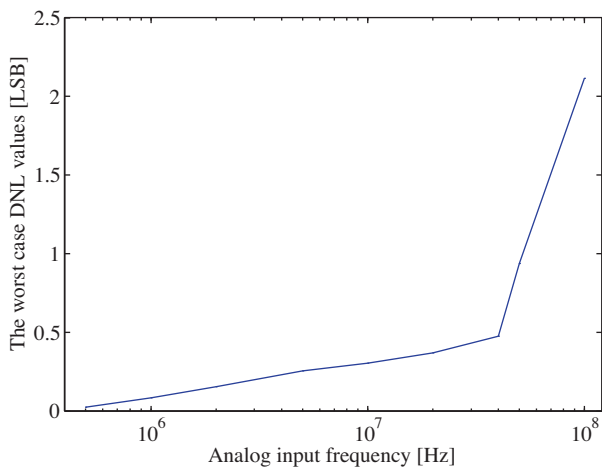


Figure 13. Worst-case DNL errors with respect to the input frequency.

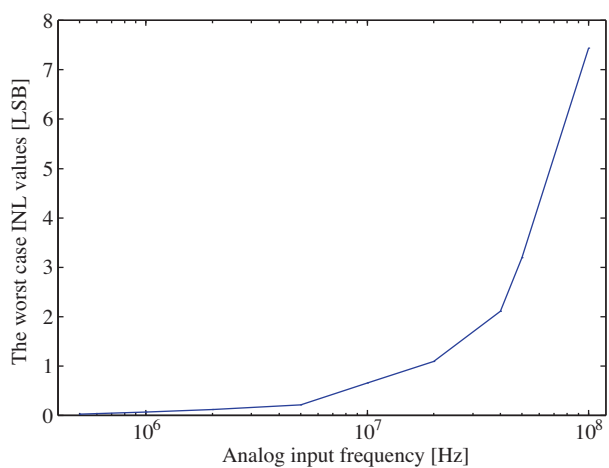
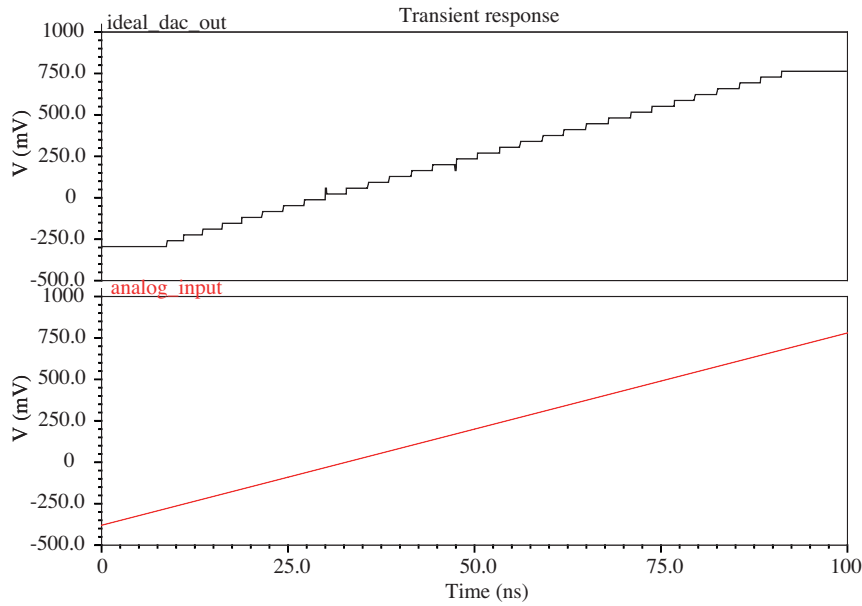


Figure 14. Worst-case INL errors with respect to the input frequency.





**Figure 15.** Reconstructed output signal for an analog ramp input signal.

**Table 3.** Transistor count of the designed system blocks.

Block name	Transistor count
Comparator array	403
Latch array	208
$2 \times 1$ Mux array	180
Fat-tree encoder	336

#### 4. Conclusion

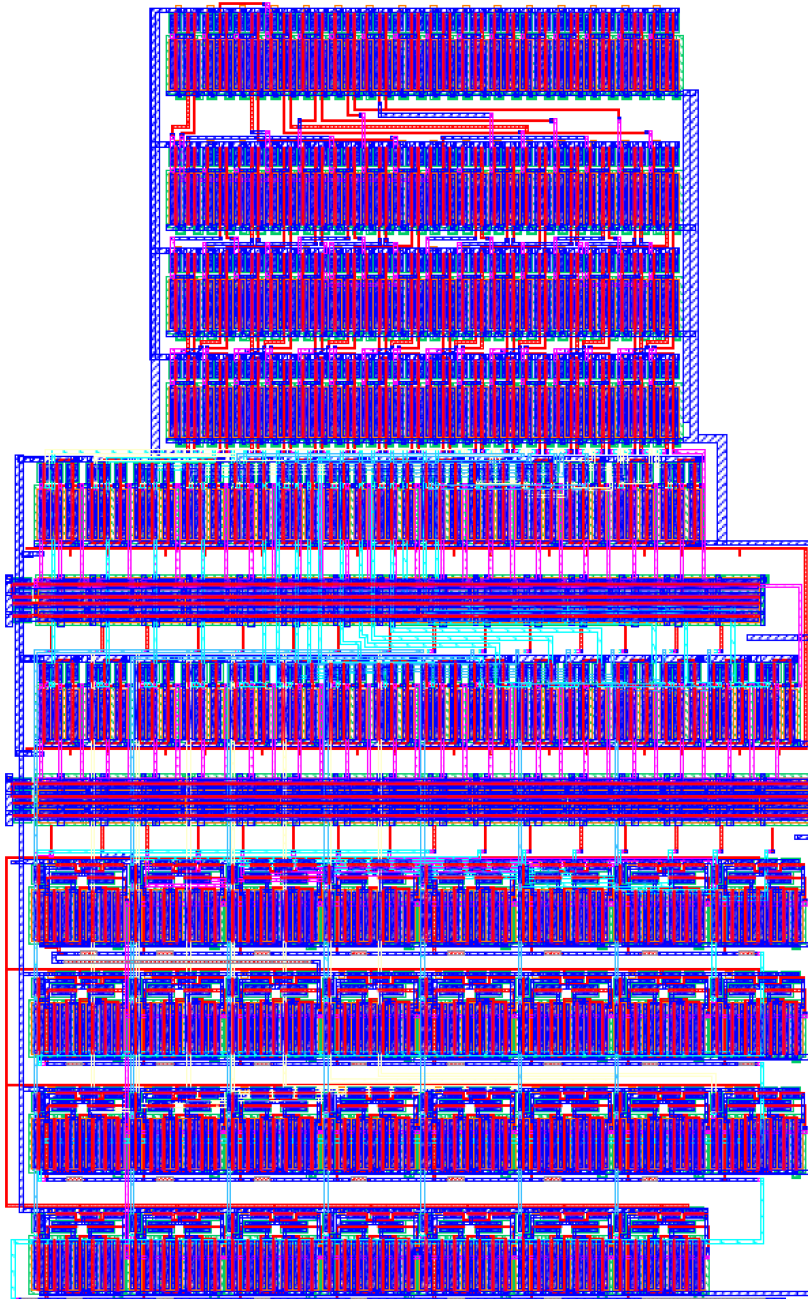
In conclusion, a 5-bit 5 Gs/s full-flash ADC was successfully designed in 0.18- $\mu\text{m}$  CMOS technology using Cadence tools. According to the simulation results, the proposed ADC is highly linear with a worst-case DNL of 0.3 LSB and INL of 0.65 LSB, and it also has a low power consumption value of 28 mW. The performance summary and comparison with similar works in the literature were listed in Table 4. Based on the simulation

**Table 4.** The comparison table.

References	Proposed	[4]	[16]	[17]	[18]
Technology (CMOS)	0.18 $\mu\text{m}$	0.13 $\mu\text{m}$	0.18 $\mu\text{m}$	65 nm	0.18 $\mu\text{m}$
Resolution	5-bit	5-bit	4-bit	5-bit	5-bit
Power supply voltage	$\pm 0.9$ V	1.2 V	1.8 V	1.3 V and 1 V	1.8
Power (mW)	28	120	4.80	28.1	36
Analog input range	-0.45 V to 0.7 V	0.8 $V_{pp}$	-	0.8 $V_{pp}$	1 $V_{pp}$
Sampling frequency (Gs/s)	5	3.2	0.7	5.5	1.056
Max INL (LSB)	-0.65	1.13	0.27	0.33	0.56
Max DNL (LSB)	-0.3	1.12	0.19	-0.3	0.32
Calibration	No	Yes	Yes	Yes	No
Active chip area ( $\text{mm}^2$ )	0.1	0.18	-	0.035	-

results, the  $2 \times 1$  Mux-based decoder structure improves the performance in terms of the speed and power consumption. Moreover, it is also thought that the proposed ADC architecture is attractive for designers from a design complexity point of view. The layout photo of the complete converter is shown in Figure 16.

As a future work, the performance of the proposed 1-of-N decoder structure will be compared to alternative types of 1-of-N decoder performances. In addition, further improvements are planned in the encoder architecture.



**Figure 16.** The layout photo of the complete converter.

## Acknowledgment

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