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Power efficient linear transmitters using sigma-delta modulation with switching amplifiers

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Abstract: In conventional envelope elimination and restoration transmitters, the envelope information of the carrier is reconstructed by modulating the supply voltage of the switching amplifier. In this paper, it is shown that the supply voltage modulation introduces nonlinearity and reduces the average power efficiency of the transmitter. Here, novel transmitter architectures using sigma-delta–modulated carrier signals are proposed to overcome these shortcomings. The proposed architecture's and conventional envelope elimination and restoration transmitter's linearity and efficiency performances are compared at various oversampling rates and signal bandwidths. It is demonstrated that the proposed architectures may provide better linearity and efficiency than conventional envelope elimination and restoration transmitters.

Key words: Envelope elimination and restoration, power amplifier, switching amplifier, nonlinear distortion, intermodulation distortion, sigma-delta modulation, transmitter design

1. Introduction

The envelope elimination and restoration (EER) transmitter topology was proposed in the 1950s as a method for implementing efficient, high-power, single-sideband (SSB) transmitters [1]. In SSB modulation, information is carried in the phase as well as the amplitude of the modulated radio frequency (RF) carrier, similar to modern digital communication systems. Using a double envelope-feedback loop with EER, up to 56% transmitter efficiency was achieved [2]. A monolithic complementary metal oxide semiconductor (CMOS) implementation of the technique was presented in [3] that improved the overall efficiency of the transmitter from 36% to 49%. It was shown in [4] and [5] that phase-feedback EER architecture may achieve an average power-added efficiency (PAE) of up to 70%, while satisfying the spectral mask of an IEEE 802.11n wireless local area network system with only a small degradation in link level performance.

In this paper, the performance limiting factors of conventional EER are explained and demonstrated by Agilent EESof Advanced Design System (ADS) simulations [6,7]. Novel transmitter architectures based on EER are proposed that may achieve higher linearity and efficiency than a conventional EER transmitter. The subject matter of this paper is protected by a number of patents [8–12].

2. Design challenges

2.1. Oversampling, envelope bandwidth, and delay matching requirements

The block diagram representation of a conventional EER transmitter is shown in Figure 1. A modulated RF signal ($V_{RF}(t)$) is split into envelope ($E(t)$) and phase ($\phi(t)$) signals by an envelope detector and a limiter,

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respectively. This process is mathematically represented by Eq. (1), where $V_I(t)$ and $V_Q(t)$ denote the in-phase and quadrature components of the RF signal, respectively.

$$V_{RF}(t) \;=\; E(t)\;\cos\left[\omega_c t \;+\; \varphi(t)\right] = \;V_I(t)\;\cos\left(\omega_c(t)\right) \;+\; V_Q(t)\;\sin\left(\omega_c(t)\right)$$
$$E(t) \;=\; \sqrt{V_I(t)^2 \;+\; V_Q(t)^2}\;\;\varphi(t) \;=\; \tan^{-1}\left(\tfrac{V_Q(t)}{V_I(t)}\right) \tag{1}$$

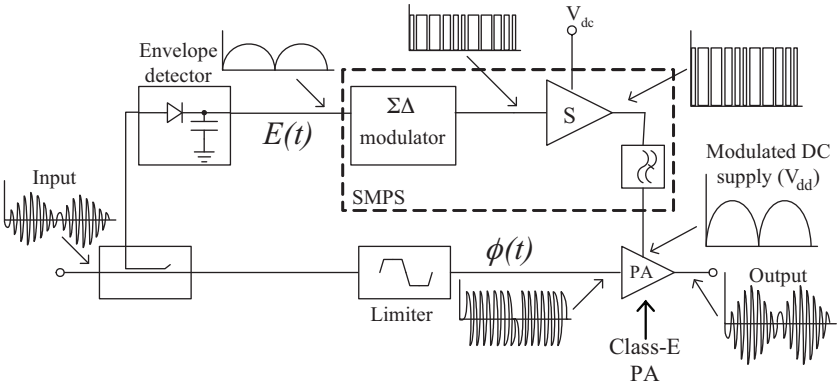


Figure 1. A conventional envelope elimination and restoration transmitter.

The limiter output, $\phi(t)$, is a constant-envelope phase-modulated signal that can be amplified by a power-efficient but very nonlinear switching power amplifier (PA), ideally without adding significant amplitude and phase distortion. In theory, a saturated amplifier can be approximated as a RF voltage generator whose output amplitude (V_{out}) is proportional to the DC supply voltage (V_{dd}), i.e. $V_{out}\;\alpha\;V_{dd}^2$. EER architecture uses this property and restores the envelope information, $E(t)$, by modulating the supply voltage, V_{dd}, of the switching amplifier.

The PAE of an EER transmitter depends on the efficiency of the PA, envelope signal path, and losses through the other components (coupler, detectors, delay lines, etc.) in the system. If an ideal switching PA with 100% PAE is assumed and the other losses in the system are ignored, the PAE of the EER is critically dependent on the efficiency of the envelope signal path, i.e. on the PAE of the switched mode power supply (SMPS).

The square-wave signals drive the switching-type amplifiers in a more efficient mode of operation compared to sinusoidal input signals. For the SMPS process to be highly efficient, pulse-width modulation (PWM) has been used, combined with a class-S switching amplifier. In PWM, the pulse timing varies with the phase of the signal and the pulse duration varies with the amplitude. It is challenging to generate an accurate pulse waveform using analog circuitry. This has resulted in the use of 1-bit sigma-delta ($\Sigma\Delta$) modulators to digitize the envelope. $\Sigma\Delta$ modulation is a form of PWM, but the binary signal is generated using digital techniques. The pulse density linearly varies with samples of the input signal, and the pulse duration is synchronized with the sampling frequency and kept fixed [13]. The quantization noise associated with digitization can be spectrally shaped so that it lies largely outside of the band of interest. This is determined by the order of the modulator and the characteristics of the resonator within the modulator.

Usually, for satisfactory linearity, a sampling rate at 10 times the RF bandwidth (B_{RF}) is chosen. High oversampling rates present the envelope with good accuracy and thus provide lower intermodulation distortion

(IMD) from the EER transmitter. ΣΔ/PWM generates a strong distortion, and thus a low-pass filter is required at the output of the class-S modulator to suppress the out-of-band IMD, harmonic distortion, and the quantization noise generated by the ΣΔ/PWM. The envelope filter bandwidth (B_E) should be at least twice the RF signal bandwidth ($B_E > 2 \times B_{RF}$). The selection of this filter is a compromise between passing the infinite bandwidth ΣΔ/PWM-modulated envelope signal and rejecting the spurious components that are inherent in the ΣΔ/PWM process.

Another important factor degrading the linearity performance is the delay matching between the 2 paths, i.e. the supply voltage modulation path and constant-envelope phase-modulated signal amplification path. The misalignment (Δt) must not exceed one-tenth of the inverse of the RF bandwidth ($\Delta t < 0.1/B_{RF}$) for a 30 dBc intermodulation distortion (IM3) level [14,15]. The delay matching requirement is related to the bandwidth of the signal, i.e. wideband signals require a more accurate delay match. The IMD introduced by the delay mismatch can be approximated by Eq. (2), which explains this relationship.

$$IMD \approx 2\,\pi\,B_{RF}^2\,\Delta t^2 \tag{2}$$

2.2. Class-E amplifier design and behavior with supply voltage modulation

2.2.1. Class-E amplifier design

In switching amplifiers (class-E and class-F), the transistor operates as an on/off switch and the output load network shapes the output waveforms to prevent simultaneous high voltage and high current, which minimizes the power dissipation in the transistor. A class-E amplifier, as shown in Figure 2, is designed in the ADS using a gallium arsenide field-effect transistor (GaAs FET) (MWT-PH-773, MicroWave Technologies) [16]. Measurement-based ADS models of the lumped surface mount technology (SMT) components are used in the design, where Murata GQM-1885 series capacitors and LQW-18A series inductors are selected on the bias network due to their high Q-factors and low effective series resistances. The mathematical expressions used in the design are shown in Eqs. (3)–(7) [17,18]. These equations include the dependence of the desired output power (P) on the load network's loaded quality factor (Q_L). The desired output power is calculated from Eq. (3) and the corresponding load resistor value (R) is calculated from Eq. (4). In these equations, V_0 is the transistor saturation offset voltage that is zero for FET devices.

$$P = \left(\frac{(V_{dd} - V_o)^2}{R}\right) 0.576801 \left(1.0000086 - \frac{0.414395}{Q_L} - \frac{0.577501}{Q_L^2} + \frac{0.205967}{Q_L^3}\right) \tag{3}$$

$$R = \left(\frac{(V_{dd} - V_o)^2}{P}\right) 0.576801 \left(1.0000086 - \frac{0.414395}{Q_L} - \frac{0.577501}{Q_L^2} + \frac{0.205967}{Q_L^3}\right) \tag{4}$$

In our design, $R = 50\ \Omega$ and $V_0 = 0$ V, since a FET is used. The chosen Q_L is 5, which is a realistic value. As the Q_L increases, the operational bandwidth of the amplifier reduces together with the harmonic distortion, but the power loss in the output resonant circuitry increases. The class-E enabling and matching network (see Figure 2) circuit element values are calculated from Eqs. (5)–(7).

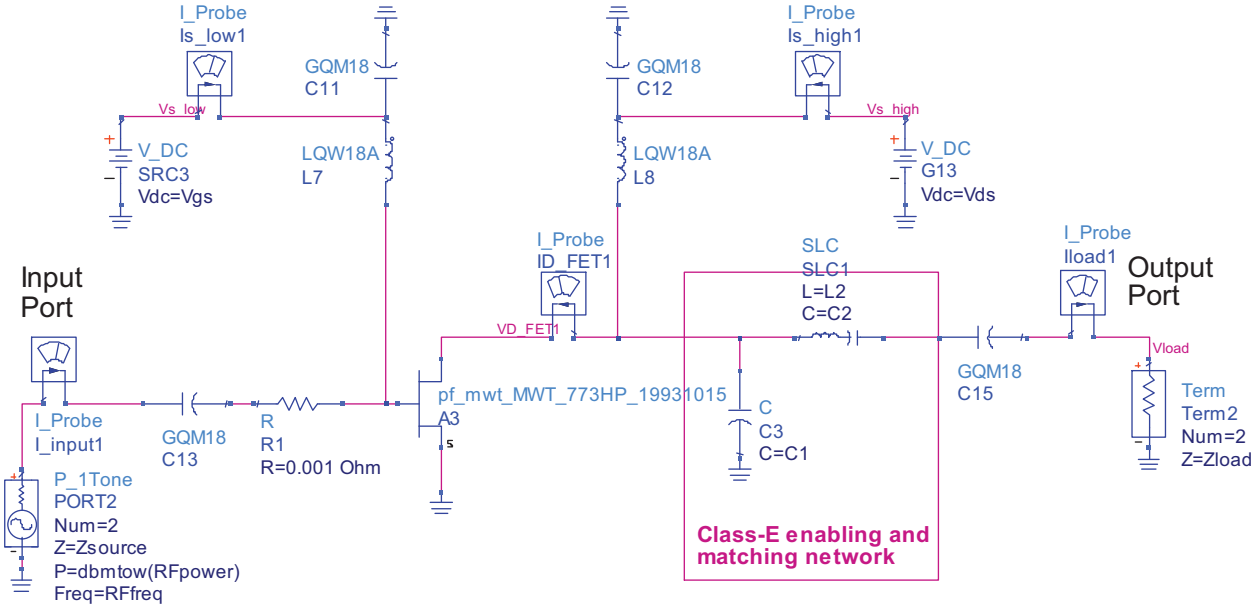


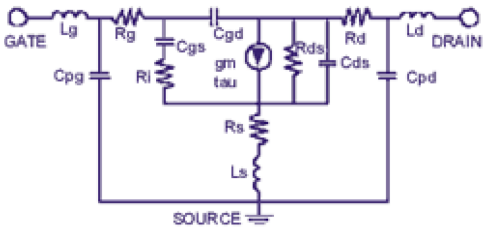
Figure 2. A class-E amplifier.

$$C1 = \frac{1}{34.2219\, f\, R}\left(0.99866 + \frac{0.91424}{Q_L} - \frac{1.03175}{Q_L^2}\right) + \frac{0.6}{(2\pi f)^2\ L1} \tag{5}$$

$$C2 = \frac{1}{2\pi\, f\, R}\left(\frac{1}{Q_L - 0.104823}\right)\left(1.00121 + \frac{1.01468}{Q_L - 1.7879}\right) - \frac{0.2}{(2\pi f)^2\ L1} \tag{6}$$

$$L2 = \frac{Q_L\, R}{2\,\pi\, f} \tag{7}$$

The calculated *C1*, *C2*, and *L2* are around 0.82 pF, 0.81 pF, and 39.78 nH, respectively; these are achievable values with distributed components. The transistor model used in the design includes intrinsic capacitances, inductances, and resistances. The transistor model and the values of these intrinsic elements are shown in Figures 3a and 3b. Due to these intrinsic elements, the theoretically calculated values were optimized in the ADS to achieve the best PAE performance. After optimization, a class-E amplifier using measurement-based models of active and passive components was designed that can provide 55% PAE.



(a)

Source Resistance	Rs	2.60	ohm
Source Inductance	Ls	0.025	nH
Drain-Source Resistance	Rds	400	ohm
Drain-Source Capacitance	Cds	0.070	pF
Drain Resistance	Rd	3.67	ohm
Drain Pad Capacitance	Cpd	0.027	pF
Drain Inductance	Ld	0.159	nH
Gate Bond Wire Inductance	Lg	0.089	nH
Gate Pad Capacitance	Cpg	0.050	pF
Gate Resistance	Rg	0.20	ohm
Gate-Source Capacitance	Cgs	0.50	pF
Channel Resistance	Ri	6.00	ohm
Gate-Drain Capacitance	Cgd	0.03	pF
Transconductance	gm	90.0	mS
Transit Time	tau	3.02	ps

(b)

Figure 3. a) MWT-PH-773 transistor model and b) values of the intrinsic components (taken from the manufacturer's data sheet [16]).

2.2.2. Behavior with supply voltage modulation

The effects of modulating the supply voltage of the amplifier are investigated by sweeping the drain supply voltage (V_{dd}) from 0 to 5.5 V. The output power, gain, and PAE characteristics of the amplifier as a function of the supply voltage are obtained and the results are shown in Figure 4. The gain of the amplifier and thus the output signal power are changing according to the supply voltage level. Indeed, the envelope information can be restored using this feature. PAE degradation is not large up to 2.5 V, but it degrades very quickly for the values below 2.5 V, dropping to only 12% at 1.5 V. This plot shows that, in terms of the PAE, changing the supply voltage of a switching PA within a limited dynamic range is acceptable, but, in our case, V_{dd} values lower than 2.5 V should be avoided. Setting a lower limit for V_{dd} modulation to maintain the PAE at a reasonable level contradicts the idea behind EER, since it will result in partial reconstruction of the envelope information, which means a higher IMD.

In order to predict the average PAE performance of an EER transmitter with signals that have a high peak-to-mean ratio, an orthogonal frequency division multiplexing (OFDM)-modulated test signal (IEEE-802.11a standard at 54 Mbps with 52 carriers) is generated and its envelope is shown in Figure 5 for the first 40 ms. The magnitude spikes, although not very frequent, are much higher than the mean magnitude level. The probability density function (PDF) of the envelope signal is calculated and plotted against the PAE of the amplifier (see Figure 6), and it can be seen that, although the class-E amplifier is capable of providing up to 55% PAE, in the EER transmitter most of the time it will be operating with a V_{dd} of around 1.4 V, ignoring the other losses in the system, which means that the transmitter will be delivering an average PAE of 16%.

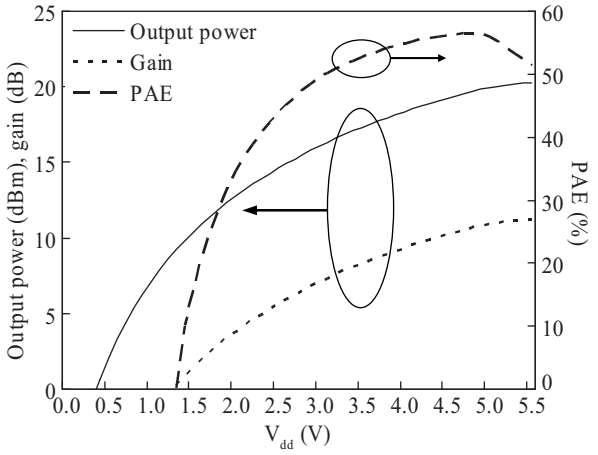


Figure 4. Output power, PAE, and gain characteristics of the class-E amplifier as a function of V_{dd}.

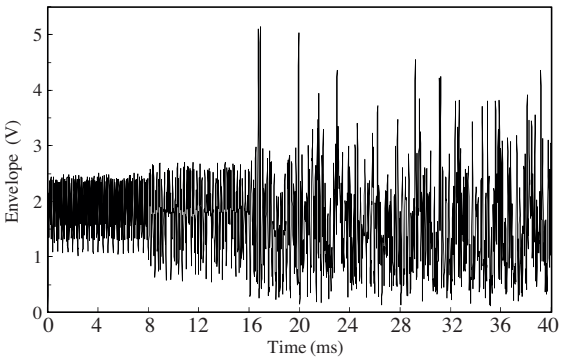


Figure 5. Envelope of an IEEE 802.11a waveform.

The AM/AM and AM/PM characteristics of the switching amplifier are also investigated with a changing supply voltage, as shown in Figure 7. Here, AM/AM and AM/PM vs. V_{dd} characteristics are referred to as V_{dd}/AM and V_{dd}/PM, respectively, since the measured amplitude and phase distortion is due to V_{dd} modulation. When the amplifier deviates from its optimum supply voltage (5 V), the V_{dd}/PM changes linearly down to 1.5 V. Below 1.5 V, the V_{dd}/PM characteristic is highly nonlinear and the resultant phase shift can be up to 60°. The V_{dd}/AM characteristic is nonlinear at high envelope levels as well as at the small signal region, and thus clipping will occur at both regions of operation. The V_{dd}/AM conversion characteristics show

that an RF feed-through is available at $V_{dd} = 0$. This will also restrict the envelope reconstruction, since low envelope levels will not be reconstructed and clipping will occur. This will increase the IMD at the transmitter output.

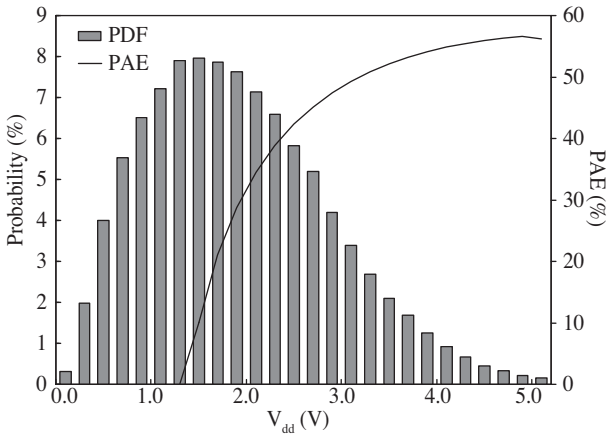


Figure 6. PDF of the IEEE-802.11a waveform and PAE characteristics of the class-E amplifier as a function of V_{dd}.

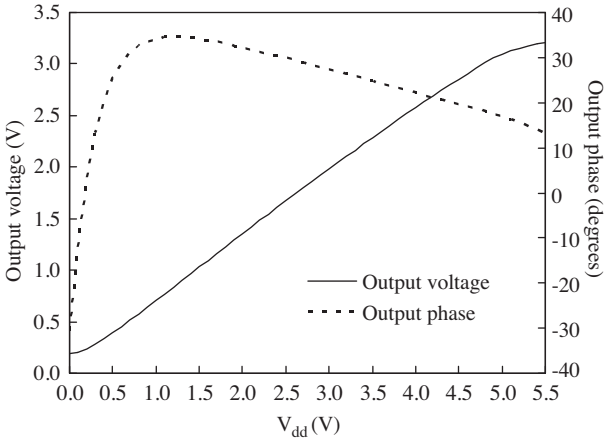


Figure 7. V_{dd}/AM and V_{dd}/PM characteristics of the class-E amplifier.

The results shown in Figures 4, 6, and 7 demonstrate that the envelope restoration process by modulating the supply voltage (V_{dd}) of a switching amplifier is a nonlinear process and introduces nonlinearity to the EER transmitter. This increases the IMD of the transmitter since it prevents the envelope from being reconstructed with 100% accuracy. Moreover, due to the statistical properties of the envelope signal, the class-E amplifier, and thus the EER transmitter, may not deliver the maximum PAE.

3. Proposed linear transmitter architectures

In this paper, it is proposed to digitize the envelope information that is at a low IF frequency using a $\Sigma\Delta$ modulator and then use this $\Sigma\Delta$-modulated envelope to convert the constant-envelope RF carrier to binary as

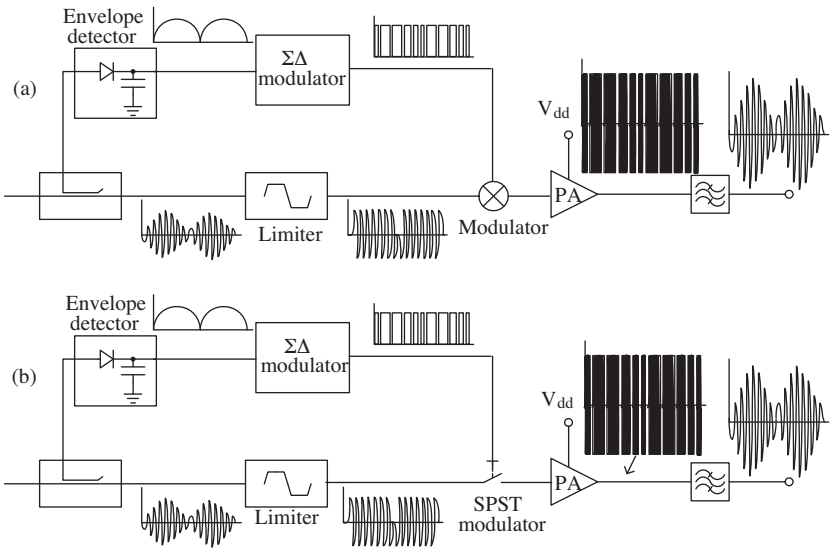


Figure 8. $\Sigma\Delta$-modulated RF carrier-driven switching amplifiers with: a) a double-balanced mixer modulator and b) a SPST modulator.

shown in Figures 8a, 8b, and 9 [19]. This is equivalent to ΣΔ-modulating the RF carrier by undersampling. In the proposed architectures, the constant-envelope ΣΔ-modulated RF carrier is amplified by the class-E amplifier and a band-pass filter at the output of the amplifier is then used to constrain the current flow to the desired carrier frequency, which reconstructs the envelope.

Three methods of implementing this idea are shown in Figures 8a, 8b, and 9. In the architectures shown in Figures 8a and 8b, the supply voltage of the class-E amplifier is not modulated. In Figure 8a, a mixer is used as a modulator to convert the constant-envelope RF carrier to binary, whereas in Figure 8b, a single-pole single-throw (SPST) switch is used for this purpose. In Figure 9, the amplifier is switched on/off according to the ΣΔ-modulated signal envelope. Therefore, all of the intermediate values between the optimum V_{dd} and 0 are eliminated. In the architecture shown in Figure 9, a class-S modulator on the envelope path is employed, since the amplification is needed to bring the ΣΔ-modulated envelope magnitude to a level high enough for biasing the GaAs FET.

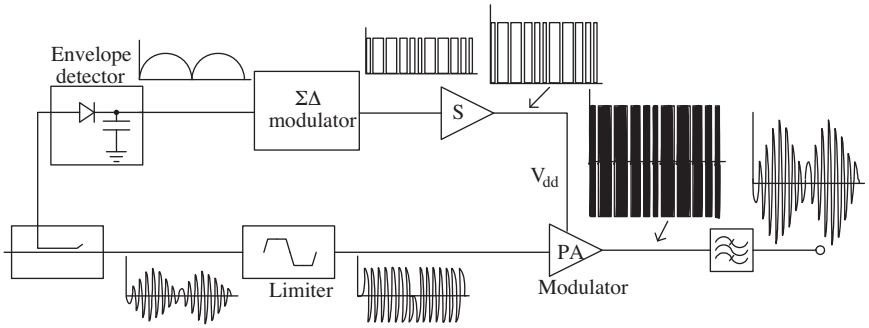


Figure 9. ΣΔ-modulated supply voltage driven switching amplifier.

3.1. ΣΔ modulator

A first-order ΣΔ-modulator with a 1-bit analog-to-digital converter (ADC) is constructed as shown in Figure 10. The input of the modulator is the signal envelope and the output is the ΣΔ-modulated signal, which is used to modulate the RF mixer (Figure 8a), SPST modulator (Figure 8b), or supply voltage of the PA (Figure 9). The sampling rates used in the ΣΔ-modulator are 10 and 15 times the envelope bandwidth; thus, the oversampling requirement of EER is satisfied with this modulator. Here, the low-pass filter that is normally added to the output of the ΣΔ-modulator in a conventional EER transmitter is removed, since in the proposed architectures, envelope reconstruction is achieved by the band-pass filter at the output of the switching amplifier.

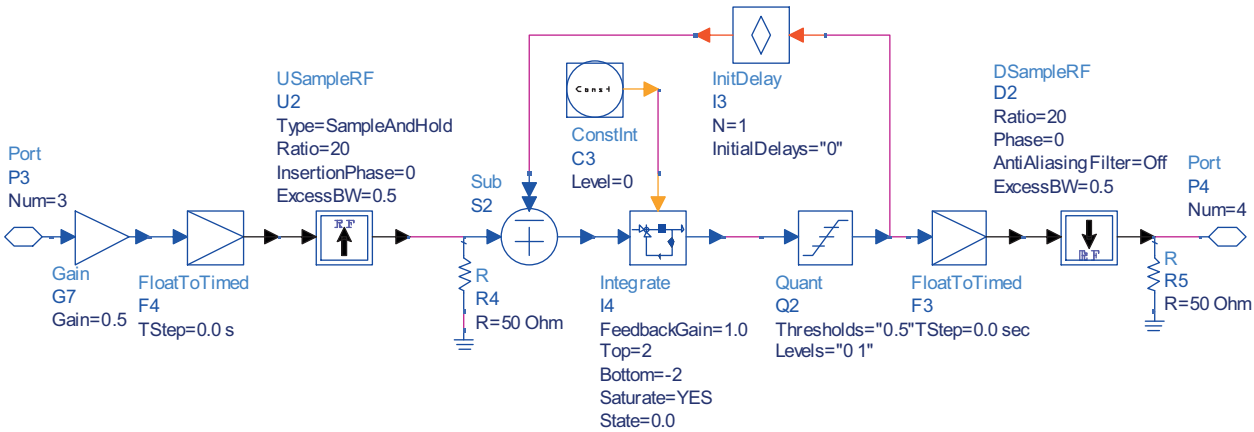


Figure 10. ΣΔ modulator.

3.2. Comparison of transmitter performances

The proposed transmitters and the conventional EER are simulated using input signals having 10- and 20-MHz envelope bandwidths centered at a 1-GHz carrier frequency. The delay matching requirement of each architecture is satisfied by the gradient optimization algorithm of the ADS for achieving the best linearity performance. The input signal power of all of the transmitters is 25 mW.

The architecture shown in Figure 8a ($\Sigma\Delta$-modulated RF carrier-driven switching amplifier using a mixer) is simulated with the settings explained above. A diode-ring double-balanced mixer, as shown in Figure 11, is used with unbalanced transformers and diodes to obtain a realistic mixer model in these simulations. The mixer local oscillator (LO) is driven with the $\Sigma\Delta$-modulated envelope where the IF input is the constant-envelope phase-modulated RF carrier.

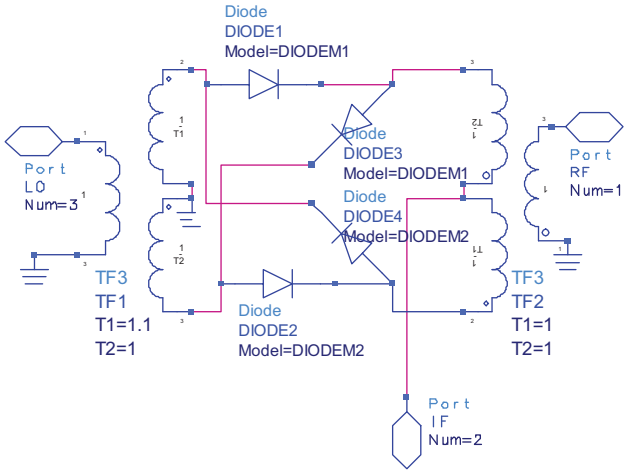


Figure 11. A diode-ring double balanced mixer.

The transmitter's output spectrum and time-domain output waveform are shown in Figures 12a, 12b, 13a, and 13b for 10 and 15 times oversampling ratios and input signals with 10- and 20-MHz envelope bandwidths. In these simulations, a low-gain (3-dB) buffer amplifier is added into the envelope signal path to drive the LO port of the RF mixer.

The architecture shown in Figure 8b ($\Sigma\Delta$-modulated RF carrier-driven switching amplifier using a switch) is simulated using the same input test signals and oversampling rates. There are plenty of SPST GaAs FET switches available at appropriate frequency bands [20,21]. CMOS and transistor-transistor logic (TTL) digital interfaces are also available. Some of these switches, operating at wireless communication standard frequencies of up to 6 GHz, are summarized in Table 2. They offer a 1-dB gain compression point (P_{1dB}) as high as 42 dBm, which is much higher than that of an RF mixer (P_{1dB} between 0 and 18 dBm). Moreover, they offer a much lower insertion loss and higher isolation than a mixer. There are switches with rise and fall times as low as 2–3 ns, which means that they can be switched on/off with a pulse train at 500 MHz, which is equivalent to 25 times oversampling an envelope signal with 20 MHz of bandwidth. In this work, a switching roll-off time of 4 ns was selected for a realistic demonstration of the switch's performance. In these simulations, the SPST switch's insertion loss is set to 1.4 dB and its isolation is set to 40 dB, which agrees with the measured characteristics of the off-the-shelf devices (see Table 2). The transmitter's output spectrum and time-domain output waveform are shown in Figures 14a, 14b, 15a, and 15b.

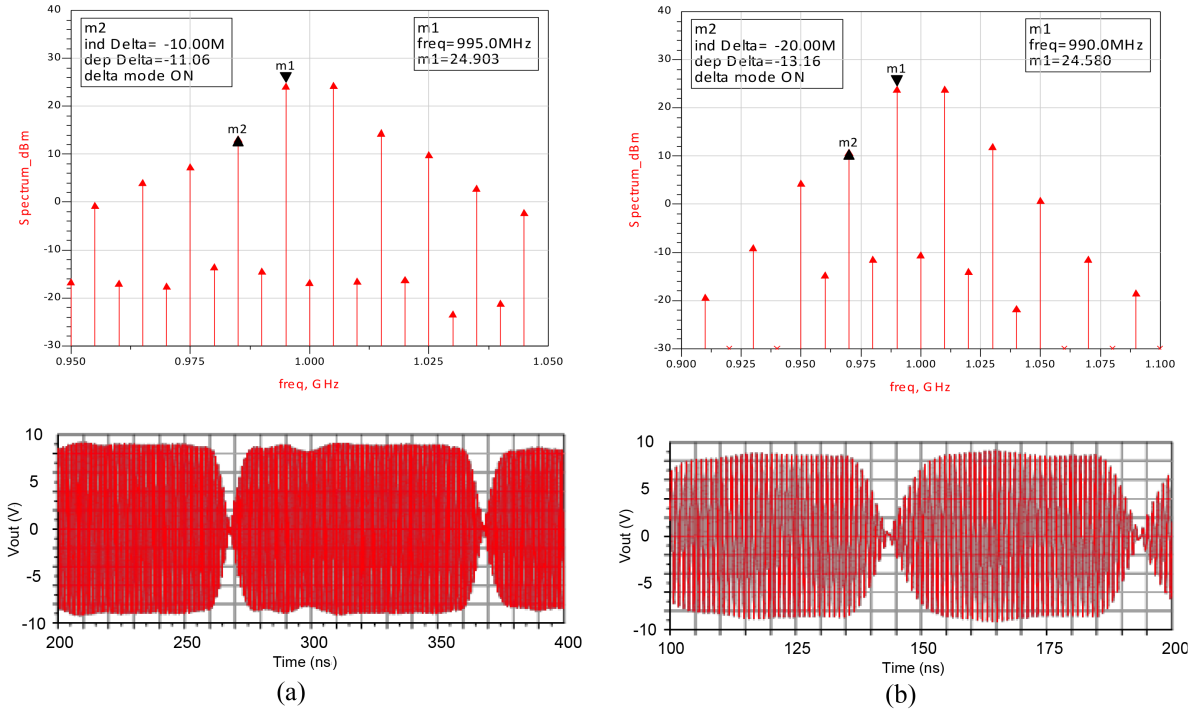


Figure 12. Output spectrum and time-domain output waveform of the ΣΔ-modulated RF carrier-driven switching amplifier using a mixer, 10 times oversampled: a) 10-MHz tone-separation and b) 20-MHz tone-separation.

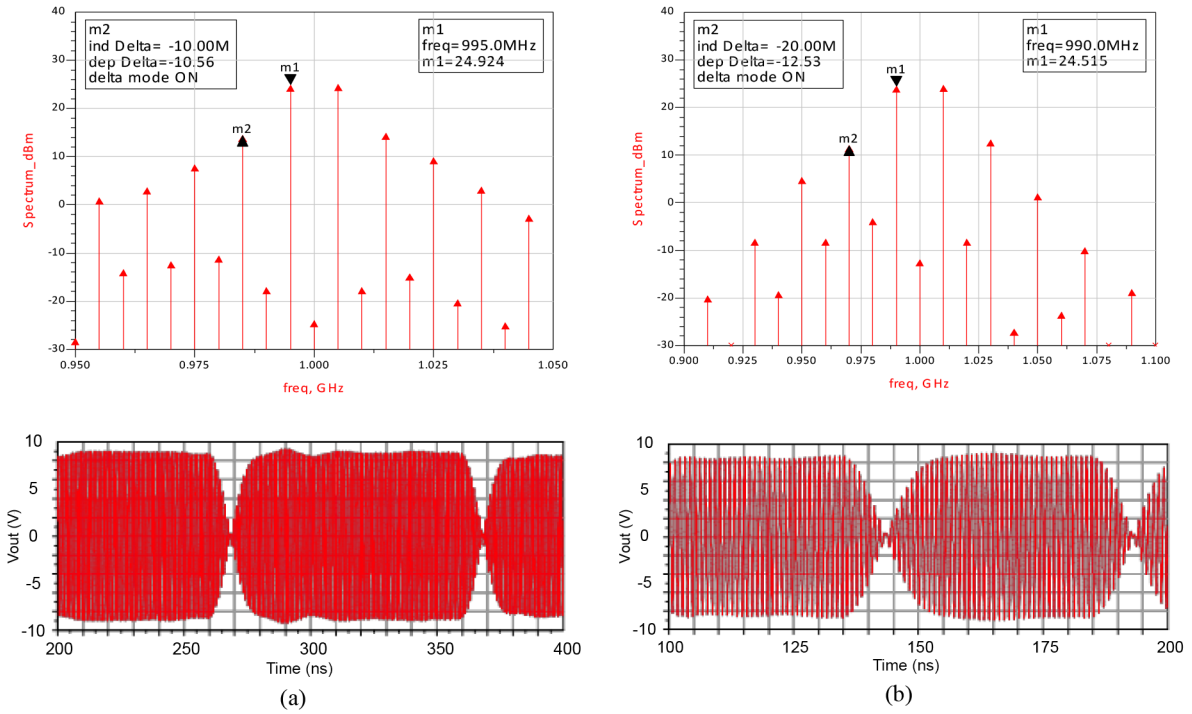


Figure 13. Output spectrum and time-domain output waveform of the ΣΔ-modulated RF carrier-driven switching amplifier using a mixer, 15 times oversampled: a) 10-MHz tone-separation and b) 20-MHz tone-separation.

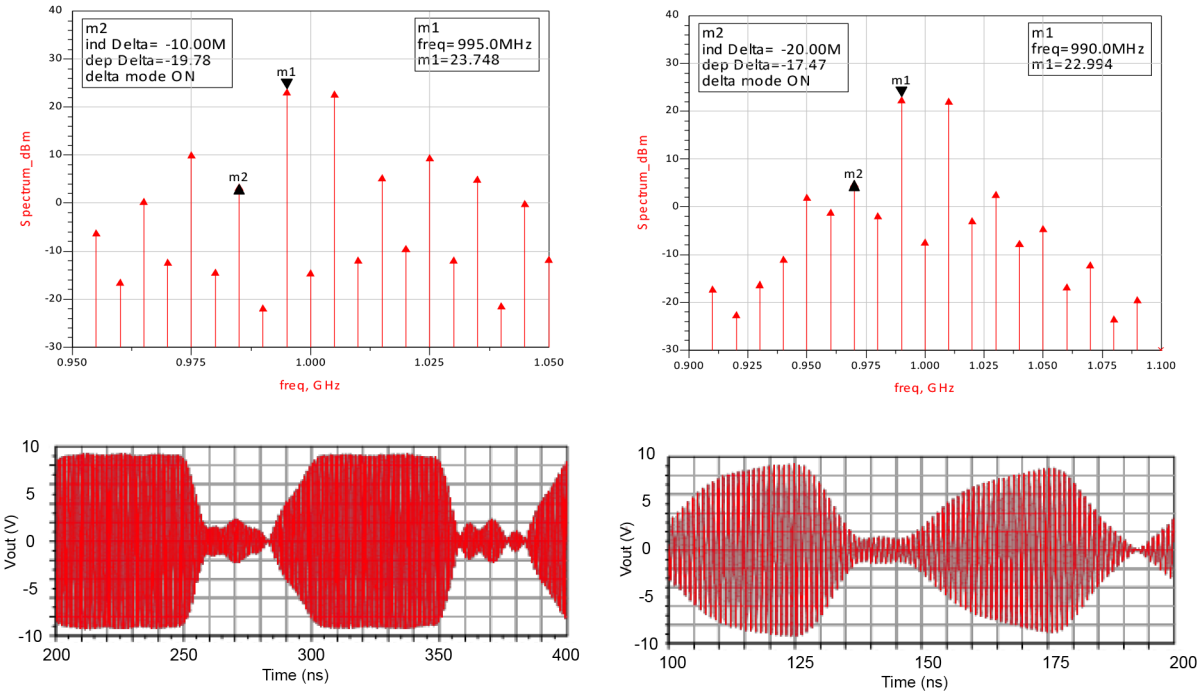


Figure 14. Output spectrum and time-domain output waveform of the ΣΔ-modulated RF carrier-driven switching amplifier using SPST switch, 10 times oversampled: a) 10-MHz tone-separation and b) 20-MHz tone-separation.

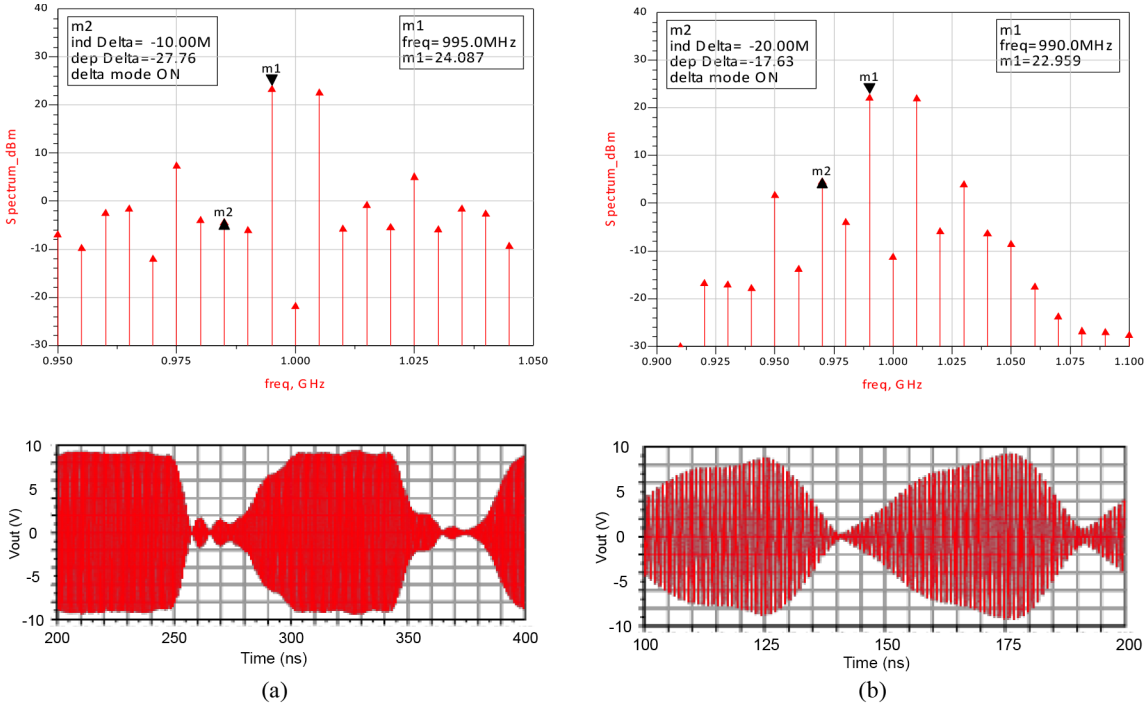


Figure 15. Output spectrum and time-domain output waveform of the ΣΔ-modulated RF carrier-driven switching amplifier using SPST switch, 15 times oversampled: a) 10-MHz tone-separation and b) 20-MHz tone-separation.

The simulation results of the novel architecture shown in Figure 9 (ΣΔ-modulated supply voltage-driven switching amplifier) are presented in Figures 16a, 16b, 17a, and 17b.

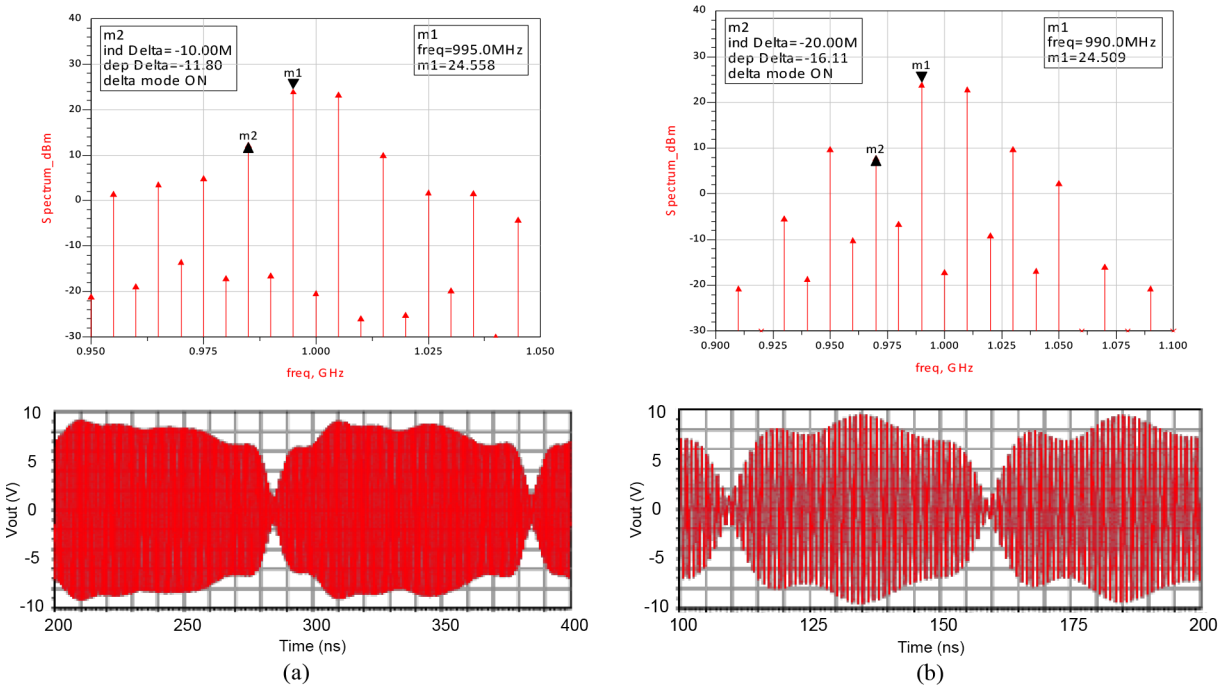


Figure 16. Output spectrum and time-domain output waveform of the ΣΔ-modulated supply voltage-driven switching amplifier, 10 times oversampled: a) 10-MHz tone-separation and b) 20-MHz tone-separation.

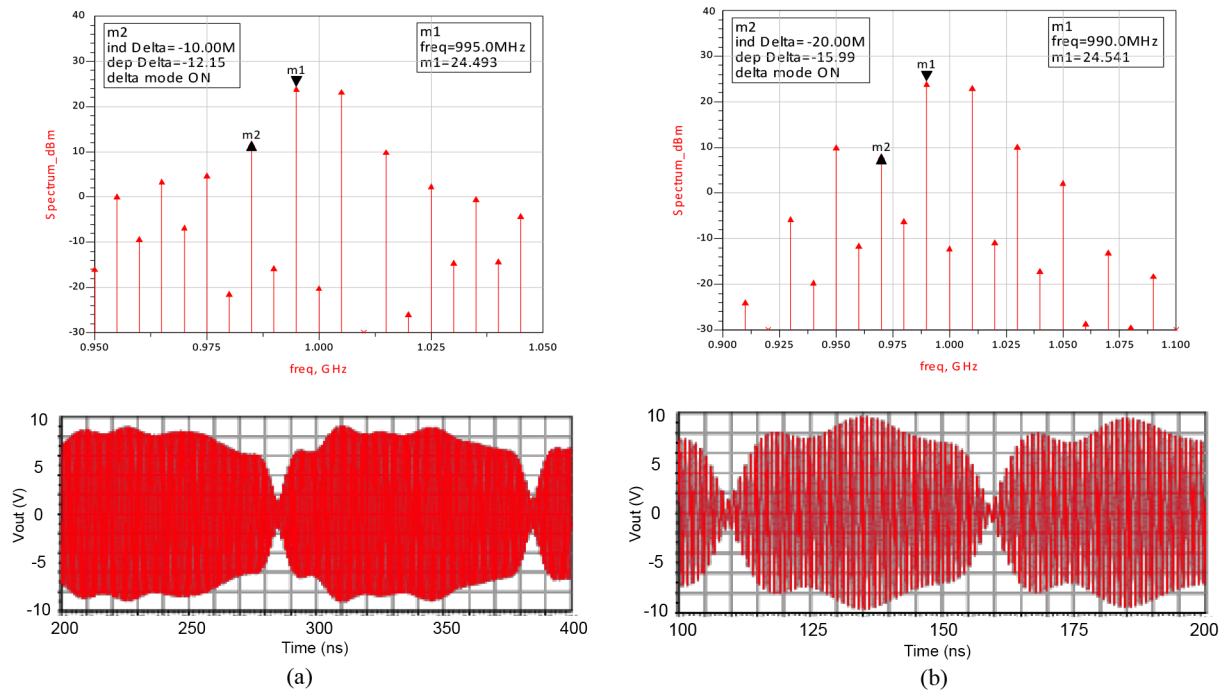


Figure 17. Output spectrum and time-domain output waveform of the ΣΔ-modulated supply voltage-driven switching amplifier, 15 times oversampled: a) 10-MHz tone-separation and b) 20-MHz tone-separation.

Table 1. Off-the-shelf SPST switche's measured performance parameters.

Manufacturer	Device	Frequency (GHz)	Insertion Loss (dB)	P1dB (dBm)	Switching speed (ns)	Isolation (dB)	Control (V)
MA-COM	MASW6010G	0–6	0.5	33	2	38	–8 to 0
Hittite	HMC231G7	0–6	1.4	27	3	52	–5 to 0
Hittite	HMC233G8	0–6	1.4	26	3	43	–5 to 0
Hittite	HMC232G7	0–6	1.4	27	3	50	–5 to 0
Hittite	HMC336MS8G	0–6	1.6	25	8	42	0 to 5
Hittite	HMC224MS8	5–6	1.2	31	10	33	TTL-CMOS

The conventional EER transmitter (Figure 1) is simulated using the same signals and settings as in the novel transmitters for a fair comparison of the linearity, output power, and efficiency performances. The results are shown in Figures 18a, 18b, 19a, and 19b. In Tables 2 and 3, the output power (Pout), PAE, and IM3 provided by the novel architectures and the conventional EER are summarized and compared.

Table 2. Summary of the results for a 10-MHz envelope bandwidth.

	Architecture in Figure 8a		Architecture in Figure 8b		Architecture in Figure 9		Conventional EER in Figure 1	
Oversampling ratio	10	15	10	15	10	15	10	15
PAE (%)	45.51	45.301	49.434	50.412	54.73	54.414	50.725	51.436
Pout (W)	0.63	0.629	0.456	0.472	0.527	0.521	0.5	0.511
IM3 (dBc)	11.06	10.56	19.78	27.76	11.80	12.15	10.02	10.13

Table 3. Summary of the results for a 20-MHz envelope bandwidth.

	Architecture in Figure 8a		Architecture in Figure 8b		Architecture in Figure 9		Conventional EER in Figure 1	
Oversampling ratio	10	15	10	15	10	15	10	15
PAE (%)	43.748	43.52.4	43.524	42.44	51.099	51.72	47.235	47.295
Pout (W)	0.574	0.576	0.372	0.389	0.503	0.516	0.452	0.456
IM3 (dBc)	13.16	12.53	17.47	17.63	16.11	15.99	13.52	13.20

The IM3 of the architecture using a mixer as a modulator (Figure 8a) is similar to that of the conventional EER, but its PAE is worse. This is due to the high conversion loss of the RF mixer. The architecture using an SPST switch (Figure 8b) provides the lowest IM3, with both 10- and 20-MHz envelope signal bandwidths. It provides similar PAE to the conventional EER at a 20-MHz envelope bandwidth, but at 10 MHz, its PAE is 5% higher than that of the conventional EER. The architecture using a $\Sigma\Delta$-modulated supply voltage (Figure 9) provides better PAE than both the conventional EER and the architecture in Figure 8b. With a 20-MHz envelope bandwidth, its IM3 level is slightly worse than that of the architecture in Figure 8b but better than that of the conventional EER. When the performances of these architectures are compared, the architecture in Figure 9 may be suitable for broadband applications. However, in this architecture, the class-S amplifier stage cannot be removed and the circuit complexity is high. If system simplicity is the most important parameter in the design, then the architecture in Figure 8b provides a good compromise among complexity, linearity, and efficiency.

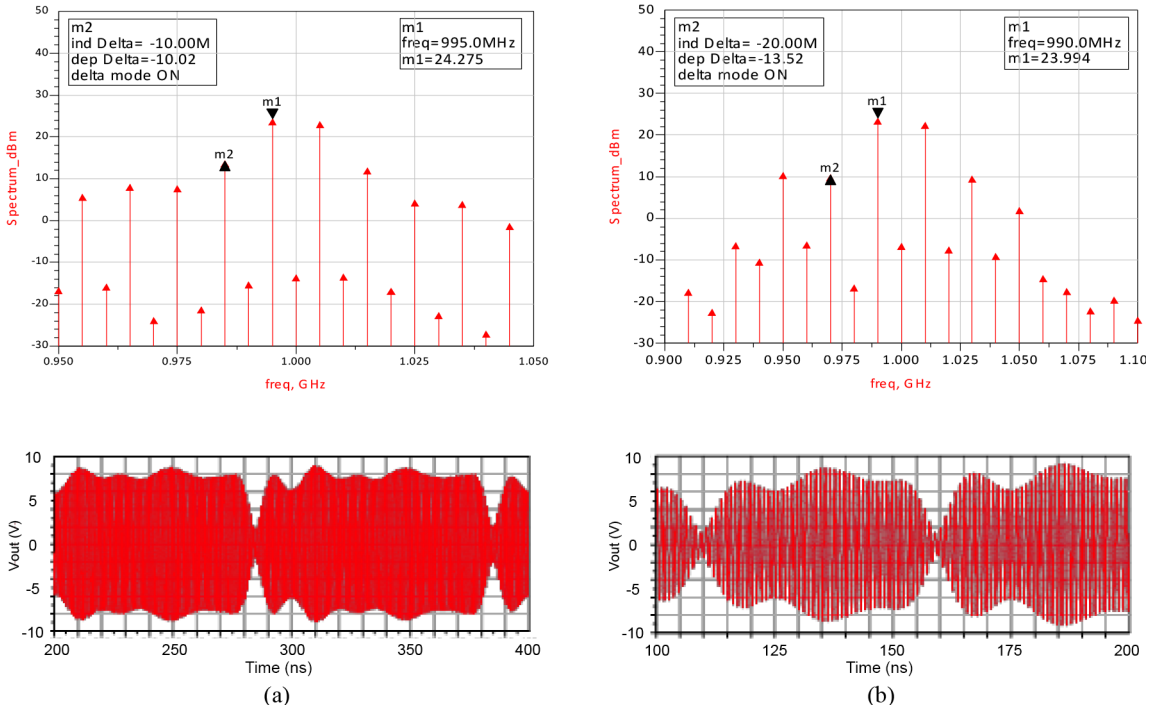


Figure 18. Output spectrum and time-domain output waveform of the conventional EER transmitter, 10 times oversampled: a) 10-MHz tone-separation and b) 20-MHz tone-separation.

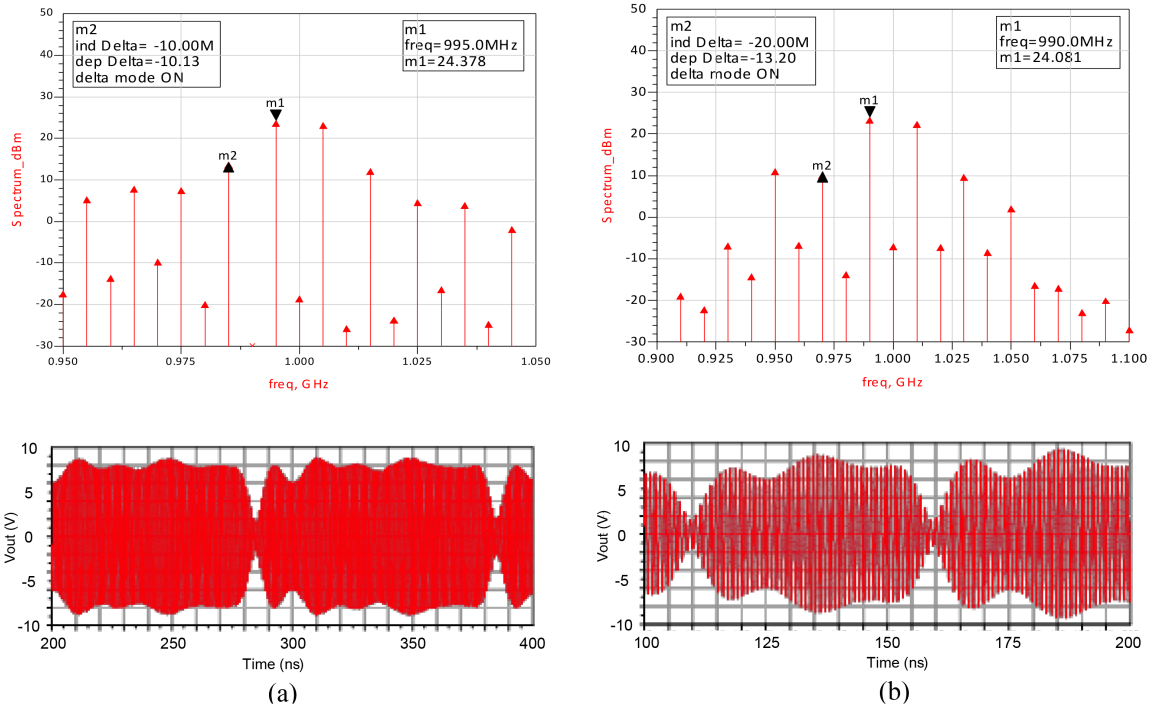


Figure 19. Output spectrum and time-domain output waveform of the conventional EER transmitter, 15 times oversampled: a) 10-MHz tone-separation and b) 20-MHz tone-separation.

4. Conclusion

The EER transmitter architecture was investigated and the factors limiting its performance were identified. It was shown that the envelope reconstruction process reduces the average PAE and introduces nonlinearity to the EER transmitter. Novel EER architectures were proposed to improve the linearity and achieve maximum PAE regardless of the statistical properties of the envelope. It was demonstrated that the proposed architectures may provide better linearity and efficiency than EER transmitters. The architecture in Figure 9 requires a class-S switching amplifier on the envelope signal path, and if system complexity is not an issue, it may be a good choice for broadband applications since it provides the highest PAE. The architecture shown in Figure 8b does not require a class-S stage and it provides the highest linearity among the transmitters, whereas its efficiency is similar to that of the conventional EER.

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