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# A reconfigurable baseband circuit applied for WiMAX low-IF receivers

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**Abstract:** This paper presents a reconfigurable baseband circuit for WiMAX low-IF receivers, including a complex filter and 2 automatic gain controllers (AGCs) for I and Q channels. Only by changing the capacitor values can the center and cutoff frequencies of the complex filter be adjusted simultaneously to realize the reconfigurability. Meanwhile, a novel one-step method to obtain fast gain settling of AGCs is proposed. The chip is fabricated in 0.13-$\mu$m CMOS technology, occupies 0.9 $\times$ 1.3 mm$^2$, and consumes 14.8 mW of power with a 1.2-V power supply. The measurement results show a reconfigurable bandwidth of 2 K to 3.5/5/10 MHz, a gain range of 10 to 58 dB, and a total harmonic distortion of 0.43% to 1.66%.

**Key words:** WiMAX, reconfigurable, baseband circuit, complex filter, automatic gain controller

## 1. Introduction

With the fast growth of wireless communications and mobile applications in the last few years, more and more radio frequency (RF) receivers are designed to achieve a high degree of integration and high performance with low power and low cost. Among several receiver architectures, superheterodyne receivers require an off-chip surface acoustic wave filter to reject image signals, which results in a low integration level and high power [1]. Zero intermediate frequency (IF) receivers can be realized as highly integrated by down-converting the RF signal to the baseband directly, thus eliminating the image signal, but they suffer from flicker noise, direct current offset, and local oscillator leakage, which limit their performance [2]. Compared with zero-IF topologies, low-IF topologies are immune to these problems because the RF signal is converted to an IF of a few MHz instead of 0 MHz. Since low-IF receivers provide a superior tradeoff between the integration level and performance, they are widely used in wireless communications [3].

As shown in Figure 1, a low-IF receiver consists of a low-noise amplifier (LNA), mixer, filter, and automatic gain controller (AGC), where the filter and AGC belong to the baseband circuit. In a low-IF receiver, the filter provides channel selection, image rejection, and noise rejection, while the AGC works to adjust the gain and maximize the dynamic range (DR) of the system. As the interface between the RF front-end and analog-to-digital converter (ADC), it is important to design a high-performance baseband circuit that improves the overall quality of the receiver and relaxes the specifications of the ADC.

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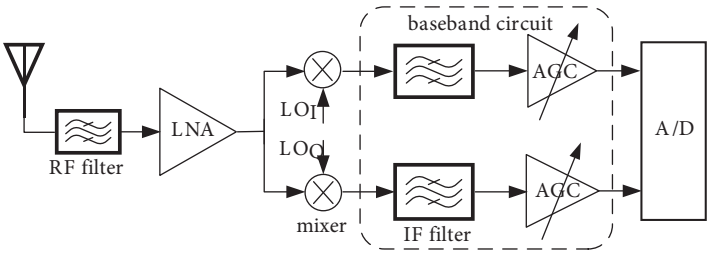


**Figure 1.** Architecture of low-IF receiver.

Worldwide Interoperability for Microwave Access (WiMAX) is an access technology of the wireless metropolitan area network based on the IEEE 802.16 family. Its advantages, such as greater coverage range, higher transmission rate, and better method to solve the last 1-km problem, make WiMAX a competitive candidate for cable access and digital subscriber lines [4]. As the IEEE 802.16 standard defines a multichannel bandwidth from 1.25 MHz to 20 MHz [5], a reconfigurable baseband circuit with programmable channel selection to satisfy different channel bandwidths is required for WiMAX applications.

This paper presents a reconfigurable baseband circuit for WiMAX low-IF receivers, in which the complex filter realizes the reconfigurability only by changing the capacitor values, and the gain control of the AGC is carried out by a new one-step method for the shortened settling time. This paper is organized as follows. Section 2 describes the architecture of the proposed baseband circuit. In Section 3, the circuit design of the key blocks is discussed. Section 4 presents the experimental results and Section 5 draws the conclusions.

## 2. Architecture of the baseband circuit

As shown in Figure 2, 3 variable gain amplifier (VGA)-filter topologies can be used in the baseband circuit of the RF receiver. According to the noise factor in Eq. (1) and the input-referred third-order intercept point (IIP3) in Eq. (2) of a cascaded system, a gain stage ahead can improve the noise performance but degrade the IIP3. Thus, the filtering-gain topology shown in Figure 2a yields high linearity with poor noise performance, while the gain-filtering topology in Figure 2b shows a low noise factor at the cost of a decreased IIP3. In the case of the gain-filtering interleaved architecture in Figure 2c, which is adopted in this paper, a superior tradeoff between noise and linearity is achieved by placing gain stages both before and after the filter [6,7].

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_N - 1}{\prod_{n=1}^{N-1} G_n} \tag{1}$$

$$\frac{1}{IIP3_{tot}} = \frac{1}{IIP3_1} + \sum_{j=2}^{n} \left\{ \frac{1}{IIP3_j} \prod_{i=1}^{j-1} A_{vi}^2 \right\} \tag{2}$$

The architecture of the proposed baseband circuit is shown in the dashed circle of Figure 3. A complex filter is used here to improve image rejection due to the stringent image rejection requirement of the low-IF receiver. Moreover, the system includes a coarse gain-setting block and a fine gain-setting block to accelerate the locking speed [8]. At last, a fixed gain amplifier (FGA) with good linearity is followed to improve the linearity of the baseband chain. As shown in Figure 3, the received RF signal is down-converted to an IF signal by the RF front-end, and then by coarse gain-settling of the programmable gain amplifier (PGA), channel selection and image rejection of the complex filter, fine gain-settling of the VGA, and amplification of the FGA in sequence, it turns into an output signal with a constant amplitude and is sent to the ADC. The detailed circuit implementation of the main blocks will be described in the next section.

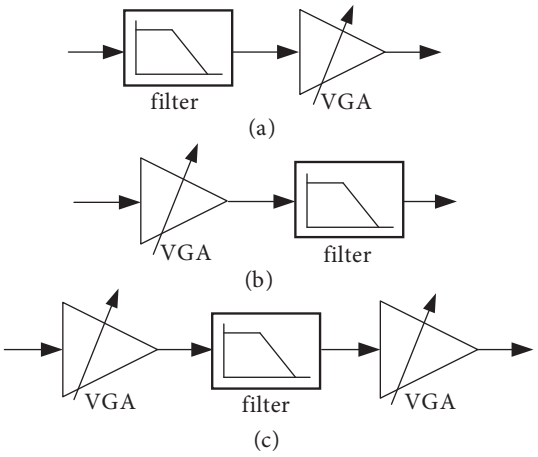


**Figure 2.** The 3 VGA-gain topologies in the baseband circuit.

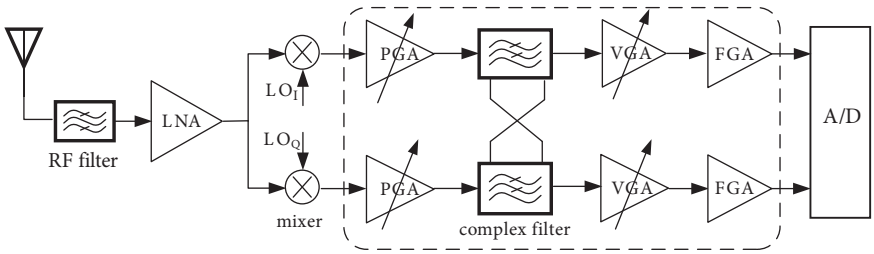


**Figure 3.** Architecture of the proposed baseband circuit.

## 3. Circuits implementation

### 3.1. Complex filter

Based on the IEEE 802.16 standard, which demands an 11-dB rejection at the adjacent channel and a 30-dB rejection at the alternate adjacent channel in the WiMAX system, a fifth-order Butterworth Gm-C complex filter is designed, as shown in Figure 4, to meet the requirements. In this design, a filter with a leapfrog structure is used because of its lowest sensitivity and best dynamic range performance. The capacitances of the filter can be expressed as:

$$Ci = \frac{\tau i \cdot Gm}{2\pi fc} \quad (i = 1, \cdots, 5), \tag{3}$$

where $fc$ is the cutoff frequency and $\tau i (i = 1, \cdots, 5)$ are constant depending on the adopted filter. The transconductors $G_m^{'}$ form a feedback loop with $Gm$, and the cross-coupling transconductors $Gmi (i = 1, \cdots, 5)$ realize frequency transformation from the real filter to the complex filter, which are given by:

$$Gmi = 2\pi fo \cdot Ci \quad (i = 1, \cdots, 5), \tag{4}$$

where $fo$ is the center frequency.

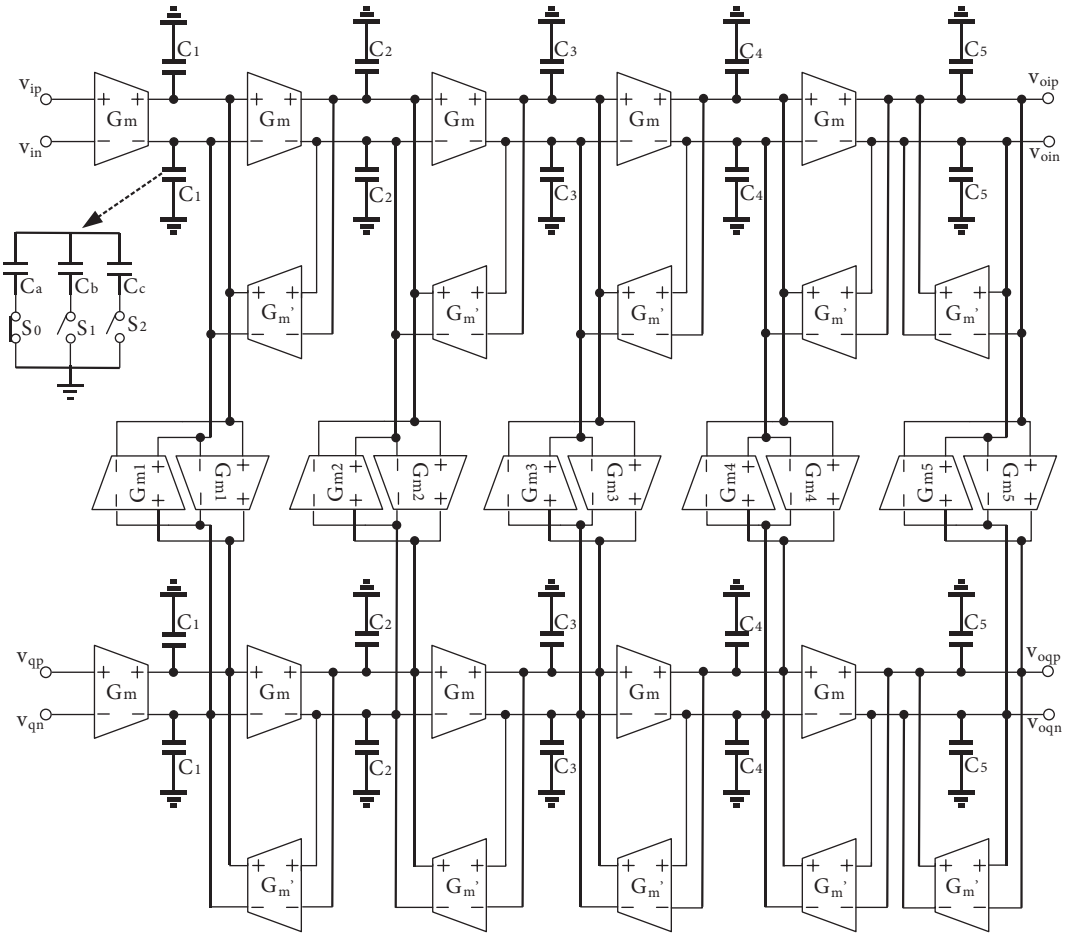


**Figure 4.** Fifth-order Butterworth Gm-C complex filter.

According to the communication protocol, the channel bandwidth is adjusted from 1.25 MHz to 20 MHz, which is 1.25/2.5/5/10/20 MHz, 1.75/3.5/7/14 MHz. A reconfigurable channel selection filter is therefore required for WiMAX applications. As shown in Eq. (3), for real filters, reconfigurability can be realized normally by tuning the transconductors or by tuning the values of the capacitors to adjust the cutoff frequency (namely, bandwidth) [9,10]. However, for complex filters, there are 2 frequency variables, center frequency and cutoff frequency, which increase the difficulty of the reconfigurable design. In this paper, a new method to realize the reconfigurability is used. Based on this method, the center frequency and cutoff frequency of the complex filter can be adjusted simultaneously only by changing the capacitor values while keeping the transconductors unchanged.

Using 3 bandwidths of 3.5 MHz, 5 MHz, and 10 MHz for examples, the reconfigurability design is presented as follows. The center frequencies of the filter are set as half of the bandwidths to relax the image rejection requirement [11], which are 1.75 MHz, 2.5 MHz, and 5 MHz, respectively. Thus, the image signal after mixing will be located at the adjacent channel of the desired signal, whose power is much smaller than the power of the desired signal. Considering the spacing between channels, a cutoff frequency of 1.5 MHz is chosen with a center frequency of 1.75 MHz. As shown in Table 1, the other 2 cutoff frequencies are set to meet

$$\frac{fo1}{fc1} = \frac{fo2}{fc2} = \frac{fo3}{fc3}, \tag{5}$$

which means that the cutoff frequencies are proportional to not only the center frequencies but also the channel bandwidths, because the center frequencies are set as half of the channel bandwidths. Hence, the filter can retain a fixed attenuation degree even with various channel bandwidths, such as an 11-dB rejection at an adjacent channel and a 30-dB rejection at an alternate adjacent channel.

**Table 1.** Center frequencies and cutoff frequencies in 2 modes.

| Mode | 1 | 2 | 3 |
|---|---|---|---|
| Center frequency (MHz) | 1.75 | 2.5 | 5 |
| Cutoff frequency (MHz) | 1.5 | 2.14 | 4.28 |
| Capacitor | $Ca+Cb+Cc$ | $Ca+Cb$ | $Ca$ |

For operation mode 1, Eqs. (3) and (4) become:

$$C1i = \frac{\tau i \cdot Gm}{2\pi fc1} \quad (i = 1, \cdots, 5), \tag{6}$$

$$Gm1i = 2\pi fo1 \cdot C1i \quad (i = \quad 1, \cdots, 5). \tag{7}$$

For operation mode 2:

$$C2i = \frac{\tau i \cdot Gm}{2\pi fc2} \quad (i = 1, \cdots, 5), \tag{8}$$

$$Gm2i = 2\pi fo2 \cdot C2i = \frac{fo2 \cdot \tau i \cdot Gm}{fc2} \quad (i = 1, \cdots, 5). \tag{9}$$

According to Eq. (5), this yields:

$$Gm2i = \frac{fo2 \cdot \tau i \cdot Gm}{fc2} = \frac{fo1 \cdot \tau i \cdot Gm}{fc1} = 2\pi fo1 \cdot C1i = Gm1i \quad (i = 1, \cdots, 5), \tag{10}$$

which means that reconfigurability can be achieved only by setting different capacitor values while keeping the transconductors unchanged. Sharing all of the transconductors for the 3 operation modes simplifies the design greatly. As shown in Figure 4, 3 different values of capacitor $Ca$, $Ca+Cb$, and $Ca+Cb+Cc$ at every node are selected with 2 control switches, $S_1$ and $S_2$, and thus the operation modes. For example, when $S_1$ turns on and $S_2$ turns off, the value of capacitor is set as $Ca+Cb$ and mode 2 is selected.

### 3.2. Coarse gain control

In the IEEE 802.16 WiMAX system, orthogonal frequency division multiplexing, which introduces stringent settling-time constraints, is used to allow high data rates. According to the IEEE 802.16 standard, the output power should be settled within 5 $\mu$s, which means that only 5 $\mu$s is used for the AGC gain convergence. The conventional AGC uses a closed-loop feedback scheme to settle the desired output signal level, which makes the time to determine the gain much larger than the time constant of the loop filter for loop stability. Thus, a closed-loop scheme is precluded in WiMAX applications, which require a fast response. On the other hand, feed-forward techniques have been proven to shorten the settling time drastically because, as open-loop topologies, they do not suffer stability constraints [12]. Therefore, feed-forward topology is chosen in this paper.

However, in feed-forward topology, the signal level is detected at the VGA input node, which is different from feedback topology. Thus, the detector must drive the full input DR of the AGC, which results in a tighter

design specification. To relax the input DR requirement of the detector and obtain faster gain settling, the system comprises a coarse gain-setting block PGA and a fine gain-setting block VGA, as shown in Figure 3. The coarse gain-setting step ensures that the input signal of the fine gain-setting block is not far from its optimal value. The PGA, as shown in Figure 5, provides a 0/10/20/30/40/50-dB programmable gain through five 10-dB FGAs, A1 to A5, and 5 pairs of control switches, S1 to S5. Gain control is realized by the switches that selectively turn on or off according to the corresponding control bits, generated by comparing Vi (i = 0 , ..., 4) with a reference voltage in sequence. As described in the IEEE 802.16 standard, the receiver should be capable of decoding input signals with a power level of from –90 dBm to –30 dBm. Considering a gain of 20 dB for a RF receiver front-end, namely the LNA and mixer, the input DR of the AGC should be –70 dBm to –10 dBm. After the amplification of the PGA, the input DR will be limited to 10 dBm (–20 dBm to –10 dBm), a range small enough to relax the design specifications of the VGA and detector.

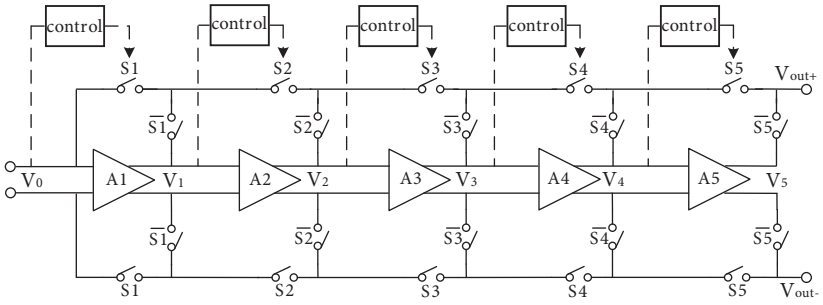


**Figure 5.** Topology of the coarse gain control.

### 3.3. Fine gain control

As mentioned before, the proposed fine gain control adopts a feed-forward technique to shorten the settling time. As shown in Figure 6a, the feed-forward AGC is composed of 2 forward paths: the signal path and the control path. The signal path is used to amplify the signal via the VGA. In order to adjust the gain of the VGA, a feed-forward control path including the detector is adopted. The detector detects the amplitude of the input signal and converts it into the control signal to control the gain setting of the VGA. This paper presents a novel method to realize gain control, which further accelerates the locking speed.

The detector in Figure 6a is shown in Figure 6b, where the differential inputs $V_{in+}$ and $V_{in-}$ from the VGA are fed into the gates of NMOS $M_1$ and $M_2$ to generate currents $I_1$ and $I_2$, respectively. Cross-coupled differential pairs $M_3$–$M_6$ full-wave rectify $I_1$ and $I_2$. The differential pairs must work as switches, so their gate voltages are driven by large signals $V_p$ and $V_n$, boosted by amplifier A. The full-wave rectified currents $I_8$ and $I_9$ are averaged to complete the amplitude detection. A cascade of 2 first-order low-pass filters performs the averaging. By current mirror and current subtraction, the current $I_c$ equals $I_9 - I_8$, which is proportional to the detected amplitude. $I_c$ is then mirrored to the VGA via $V_c$ to achieve gain control. We assume that

$$IC = k1Ain, \tag{11}$$

where $Ain$ is the amplitude of input signal and $k1$ is a constant depending on the detector.

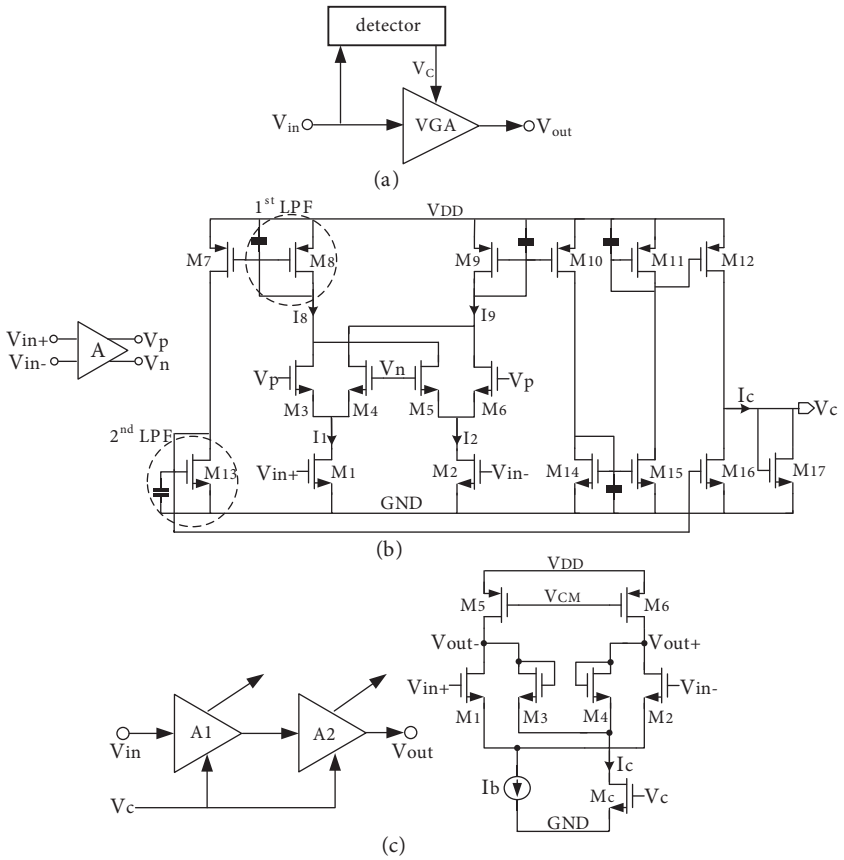


**Figure 6.** a) Feedforward AGC, b) schematic of the detector, and c) schematic of the VGA.

As shown in Figure 6c, the proposed VGA is implemented by a cascade of 2 identical amplifiers, where the tail current $I_c$ is mirrored from the detector. The gain of A1 (A2) can be expressed as:

$$Av1 = \frac{gm1,2}{gm3,4} = \sqrt{\frac{(W/L)1,2Ib}{(W/L)3,4IC}} = \sqrt{\frac{k2}{IC}}, \tag{12}$$

where $k2 = \frac{(W/L)1,2Ib}{(W/L)3,4}$.

Therefore, the gain of the VGA is given by:

$$Av = A_{v1}^2 = \frac{k2}{IC}. \tag{13}$$

The substitution of Eq. (11) into Eq. (13) yields

$$Av = \frac{k2}{k1Ain}, \tag{14}$$

which means that the gain of the VGA is inversely proportional to the input signal amplitude. Thus, for a VGA input signal with an amplitude of $Ain$, the amplitude of the VGA output can be expressed as:

$$Aout = Av \cdot Ain = \frac{k2}{k1Ain} \cdot Ain = \frac{k2}{k1}, \tag{15}$$

which means that the output of the VGA remains constant for any signal within the input DR. Furthermore, the gain convergence is done in one-step, i.e. as soon as the input signal is detected, the gain of the VGA is settled.

## 4. Experiment results

The circuit is fabricated in a standard 0.13-$\mu$m CMOS process. A microphotograph of the chip, which consists of 2 AGCs for the I and Q channels and a complex filter, is shown in Figure 7, and the whole area, including the pads, is 0.9 $\times$ 1.3 mm$^2$. Using 4-orthogonal input signals from a Tektronix AWG5014C signal generator, the output transient signals are measured by an Agilent MSO-X 3024A oscilloscope and the output spectra are measured by an Agilent E4447A spectrum analyzer.

Figure 8 gives the gain vs. input amplitude plot of the baseband circuit, which shows a gain range of 10.13 to 58.06 dB, with a gain error of less than 0.9 dB when the amplitude of the input signal varies from 120 mV to 0.5 mV. Since the gain of the filter keeps approximately constant within the passband, it can be thought that the AGC achieves a gain range of 48 dB.

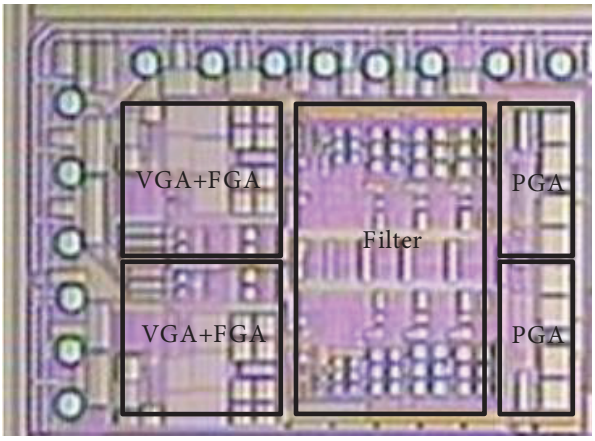


**Figure 7.** Chip photograph of the proposed baseband circuit.

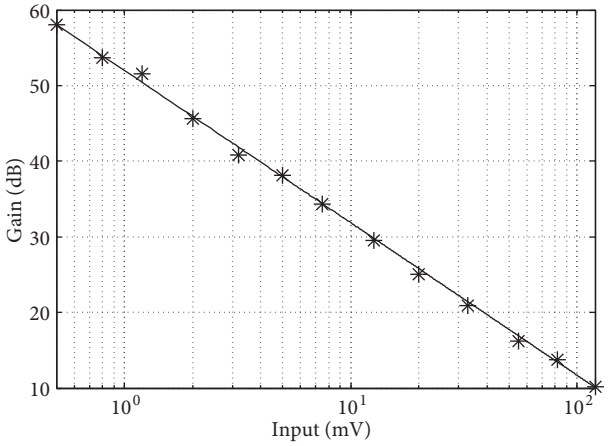


**Figure 8.** Gain vs. input amplitude plot of the baseband circuit.

It can be seen from Section 3.2 that the gain of the PGA is set as 0 dB when a signal with relatively large amplitude is input, and thus the input signal of the complex filter is the same as that of the baseband circuit. This means that the input-output gain plot of the filter can be obtained with the input signal of the baseband circuit and the filter output wave is measured from mid-measure-point. Figure 9 gives the frequency characteristics curve fitted from the input-output gain plots of the filter at different frequency points. This shows that the reconfigurable function works well and, for all of operation modes, the image rejection ratio (IRR) is about 32 dB and the attenuations for the adjacent and alternate adjacent channels are more than 25 dB and 40 dB, respectively, which meet the requirements of the IEEE 802.16 standard.

Figure 10 gives the frequency response of the baseband circuit with different input amplitudes operated in mode 3, which shows a 3-dB bandwidth of 2 K to 10 MHz. The measured total harmonic distortion (THD) vs. input amplitude plot is given in Figure 11. It shows a minimum THD of 0.43% for a 50-mVp input signal and a maximum THD of 1.66% for a 120-mVp input signal. The whole baseband circuit operates from a 1.2-V power supply and draws 12.3 mA. Finally, the principal characteristics of this work and a comparison with other baseband circuit designs are summarized in Table 2.

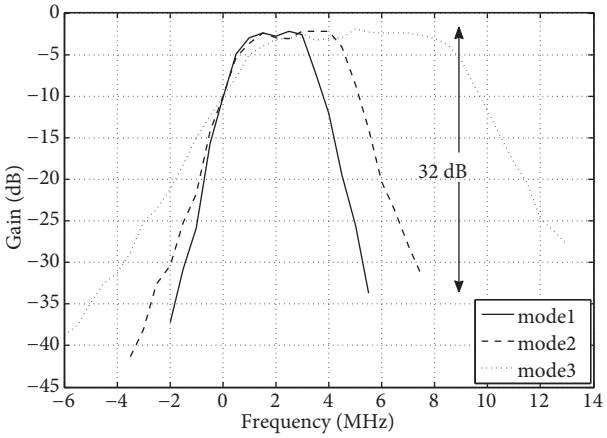


**Figure 9.** Frequency characteristics of the complex filter under different operation modes.

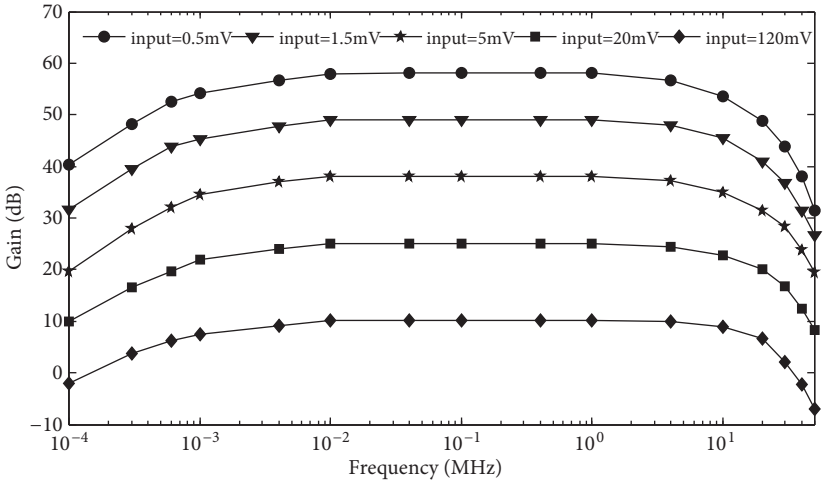


**Figure 10.** Frequency response of the baseband circuit.

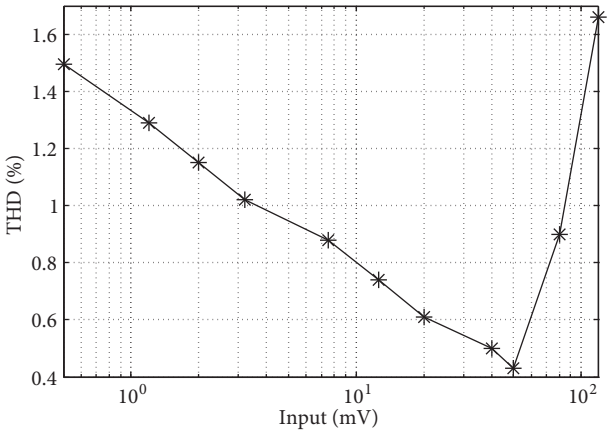


**Figure 11.** THD vs. input amplitude plot of the baseband circuit.

**Table 2.** Comparison of principal characteristics.

| | [2] | [7] | [10] | This work |
|---|---|---|---|---|
| Process | 0.35-$\mu$m SiGe BiCMOS | 40-nm CMOS | 0.18-$\mu$m CMOS | 0.13-$\mu$m CMOS |
| Die size (mm$^2$) | 1.1 | 0.38 | 1.68 | 1.17 |
| $V_{DD}$ (V) | 2.8 | 1.1 | 1.8 | 1.2 |
| Power (mW) | 45.9 | 18 | 31.3 | 14.8 |
| Bandwidth (Hz) | 5 K to 4.28 M | 100 M | 0.8 K to 18 M | 2 K to 3.5/5/10 M |
| IRR(dB) | 35 | 20 | 34 | 32 |
| Passband ripple (dB) | 0.5 | 0.8 | 1 | 0.5 |
| Gain range (dB) | 5–45 | 0–48 | 0–39 | 10–58 |
| Settling time ($\mu$s) | – | – | 4.8 | 1.2 |
| Linearity @ gain | OIP3 = 5.7 dBm @ 8 dB | THD = 1.8% @ 16 dB | IIP3 = 10 dBVp @ 0 dB | THD = 0.43% @ 16 dB |

## 5. Conclusions

In this paper, a baseband circuit applied for WiMAX low-IF receivers including a complex filter and AGC was presented. The reconfigurability was realized by changing the capacitor values of the complex filter to satisfy the different channel bandwidths defined in the IEEE 802.16. Moreover, a new fast-settling AGC was designed by setting the gain of the VGA inversely proportional to input signal amplitude. The chip was fabricated in 0.13-$\mu$m CMOS technology and consumes 14.8 mW of power with a 1.2-V power supply. The measurement results show a reconfigurable bandwidth of 2 K to 3.5/5/10 MHz, a gain range of 10 to 58 dB, and a THD of 0.43% to 1.66%.

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## References

[1] B. Razavi, "Architectures and circuits for RF CMOS receivers", IEEE Custom Integrated Circuits Conference, pp. 393–400, 1998.

[2] H. Ma, F. Yuan, S. Liu, "A low power baseband chain for CMMB application", IEEE International Conference on Communication Systems, pp. 1466–1470, 2008.

[3] J.S. Syu, C.C. Meng, Y.H. Teng, "Large improvement in image rejection of double-quadrature dual-conversion low-IF architectures", IEEE Transactions on Microwave Theory and Techniques, Vol. 58, pp. 1703–1712, 2010.

[4] S.K. Ray, K. Pawlikowski, H. Sirisena, "Handover in mobile WiMAX networks: the state of art and research issues", IEEE Communications Surveys and Tutorials, Vol. 12, pp. 376–399, 2010.

[5] IEEE Computer Society, IEEE Standard 802.16 TM-2004-Air Interface for Fixed Broadband Wireless Access Systems, New York, IEEE, 2004.

[6] S.J. Yoo, Design of analog baseband circuits for wireless communication receivers, PhD, Ohio State University, Columbus, OH, USA, 2004.

[7] M. Miyahara, H. Sakaguchi, N. Shimasaki, A. Matsuzawa, "A 84 mW 0.36 mm$^2$ analog baseband circuits for 60 GHz wireless transceiver in 40 nm CMOS", IEEE Radio Frequency Integrated Circuits Symposium, pp. 495–498, 2012.

[8] J.P. Alegre, B. Calvo, S. Celma, "A high-performance CMOS feedforward AGC circuit for a WLAN receiver", IEEE Transactions on Industrial Electronics, Vol. 57, pp. 2851–2857, 2010.

[9] A. Miller, J.S. Hong, "Wideband bandpass filter with reconfigurable bandwidth", IEEE Microwave and Wireless Components Letters, Vol. 20, pp. 28–30, 2010.

[10] J. Okjune, "Analog baseband processor for CMOS 5-GHz WLAN receiver", PhD, University of Florida, Gainesville, FL, USA, 2007.

[11] K. Kwon, J. Choi, Y. Hwang, "A 5.8 GHz integrated CMOS dedicated short range communication transceiver for the Korea/Japan electronic toll collection system", IEEE Transaction on Microwave Theory and Techniques, Vol. 58, pp. 2751–2763, 2010.

[12] F.Y. Li, H.G. Yang, Y. Wang, "Current mode feed-forward gain control for 0.8 V CMOS hearing aid", IEEE International Symposium on Circuits and Systems, pp. 793–796, 2011.