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Class-E GaAs HBT power amplifier with passive linearization scheme for mobile wireless communications

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Abstract: A linearization technique for improving the class-E power amplifier (PA)'s adjacent channel power ratio (ACPR) is proposed. The design is simulated in a 2-μm InGaP/GaAs heterojunction bipolar transistor process. The integration of a passive predistorter at the input of the PA linearizes the proposed architecture. At a 29-dBm output power, the PA's ACPR is indicated to be –51 dBc, meeting the stringent code division multiple access regulation. At this exact output power, the simulated power added efficiency is 55% with the collector voltage headroom consumption of 3.4 V. The input return loss, S11, of the PA is simulated as –12.5 dB. With an active finger print dimension of 1000 μm $\times$ 750 μm, the proposed PA is well suited for the application of mobile wireless communication.

Key words: Class-E, HBT, linearization, power amplifier

1. Introduction

In recent years, increasing demand for a higher data rate for mobile wireless communication has set an innovative milestone in the art of transmitter design. As the data rate increases, the transmitter, in particular the power amplifier (PA), needs to maintain a linear operating region, thus establishing the requirement to operate at a back-off region from maximum saturated output power [1]. This restriction imparts design challenges in maintaining high power-added efficiency (PAE) at the back-off output power level.

In an effort to improve the efficiency at the back-off output power, the preferred enhancement methods can be capsulated into 2 distinct categories, the efficiency enhancement method and linearization method [2]. These methods have gained popularity and are reported in several distinguished implementations [3–12].

Among the architecture of design concern in targeting efficiency enhancement are Doherty PA and envelope tracking PA. The Doherty PA, consisting of 2 amplifiers connected in parallel, employs the load modulation technique to enhance the efficiency at the back-off output power [3–6]. A quarter-wave transformer is used to modulate the load in improving the efficiency and third-order intermodulation distortion (IMD3) cancellation between the main and auxiliary amplifiers, paving into the linearity enhancement [7]. The implementation and integration of an on-chip quarter-wave transformer will substantially increase the die size. Alternately, a popular method in improving the efficiency of the PA is envelope tracking, where the supply voltage of the PA is modulated respective to the output power level. This enables the PA to operate at a low supply voltage at an equivalently low power level, which in turn boosts its efficiency. However, the complexity in implementation serves to be the penalty paid. Often, a hybrid technology merger of the complementary metal-oxide

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semiconductor solution to modulate the supply voltage and GaAs heterojunction bipolar transistor (HBT) PA is adapted to implement this technique [8].

In the event of a reduced quiescent current, a high-efficiency PA is delivered, where the PA is operated close to the cutoff point in the I-V curve, which translates to a highly nonlinear operation. Conventionally, feedback and feedforward [9] techniques are adapted to linearize the PA. In current practice, the analog predistortion (APD) and digital predistortion (DPD) techniques are gaining popularity in the implementation. Through these methods, the input signal to the PA is distorted prior to amplification, as such that the magnitude and phase of its nonlinear transfer function have opposite phase and magnitude responses from the amplifier. The DPD method highlights the use of a DSP processor to generate the nonlinear response [10]. Complex integration is the primary disadvantage in DPD. In contrast, APD imparts a simple construction by integrating an additional active device to the input of the power amplifier [11]. A similar cancellation is also possible with cascode topology integration [12].

In this work, the APD technique is proposed to linearize a nonlinear highly efficient class-E PA. The PA is linearized by integrating a passive predistorter at the input. The architecture results in a PAE of 55%, while complying with code division multiple access (CDMA) ACPR specifications at 29-dBm of output power. The organization of this paper is as follows. Section 2 reviews the theory of operation of the designed class-E PA along with the proposed linearization technique. In Section 3, the simulation result is presented followed by the conclusion in Section 4.

2. Theory of operation

2.1. Class-E PA design

Figure 1 describes the topology of the proposed PA, which integrates a class-E PA passive predistorter linearizer and an output matching network.

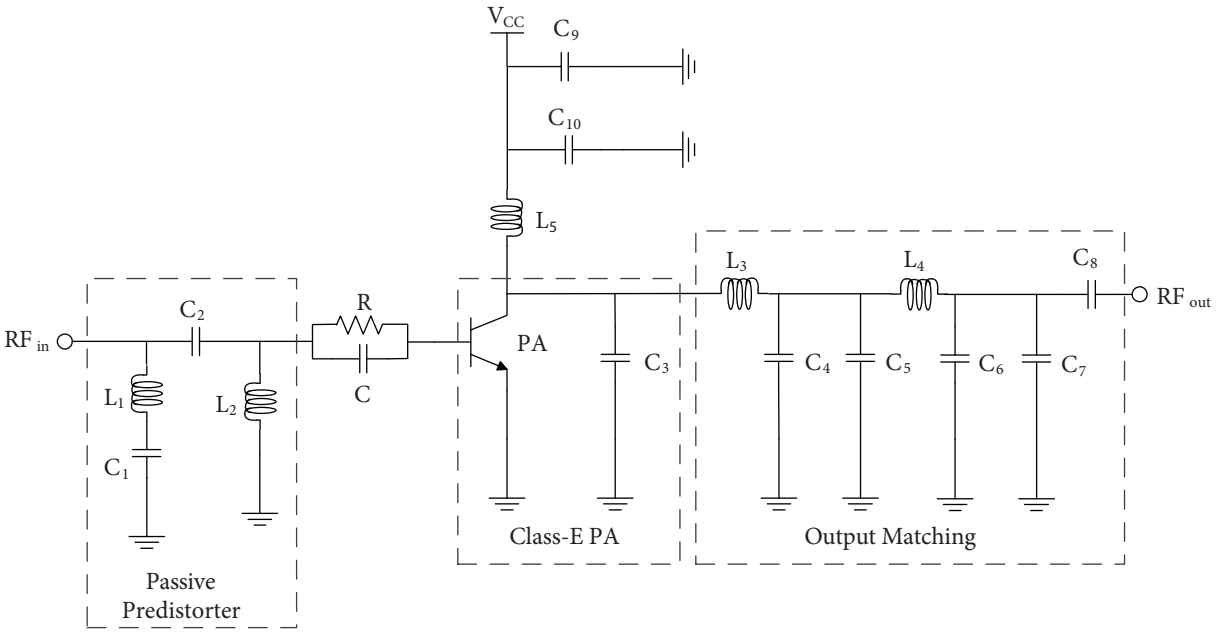

Figure 1. Proposed class-E PA with integrated passive analog predistorter.

2.1.1. Optimum load resistance

In the initial step of the design methodology, the essential maximum output power for the linear transmission is determined by selecting an appropriate amplifier dimension. This is done by computing the optimum load resistance, R_{opt}, of the class-E amplifier, given as:

$$R_{opt} = \frac{V_{dc} - V_k}{I_{\max}}, \tag{1}$$

where V_{dc} is the desired operating voltage, V_k is the I-V curve knee voltage, and I_{max} is the maximum current obtained in the event that the device is biased at a class-A biasing point. Referring to Eq. (1), the optimum load line resistance is computed as 4.7 Ω. The load resistance is presented as a family of contours for various output power levels in the Smith chart, as described in Figure 2. In this plot, R_1 is the optimum location for the PAE at a back-off output power of 29 dBm.

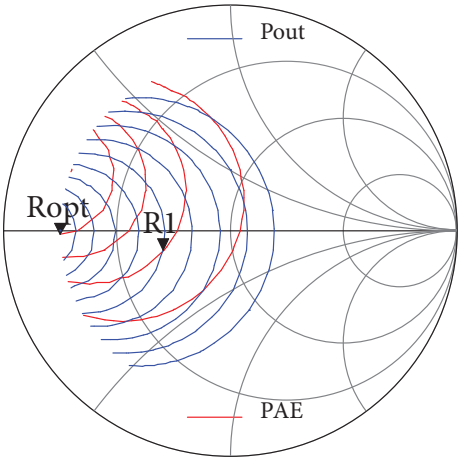

Figure 2. Output power and PAE contours.

2.1.2. Principle operation of the class-E PA

In an ideal class-E PA, the transistor operates as a switch by shaping the current and voltage responses, avoiding an overlap. Since the power dissipation is minimized, the PA observes a highly efficient operation. This desirable characteristic is achieved by biasing the PA close to the cut-off region of the I-V curve. In reference to Figure 3, the voltage and current waveforms of a class-E PA when the switch is turned ON can be represented as [13]:

$$v_{sw} = 0, \tag{2}$$

$$i_{sw}(\omega t) = i_{out}\left[\sin(\omega t + \alpha) - \sin\alpha\right]. \tag{3}$$

Alternately, when the switch is OFF, the voltage and current are given by:

$$v_{sw} = \frac{1}{\omega C_1}\int_{\pi}^{\omega t} i_c(\omega t)\, d\omega t, \tag{4}$$

$$i_{sw} = 0, \tag{5}$$

where α represents the incurred phase shift.

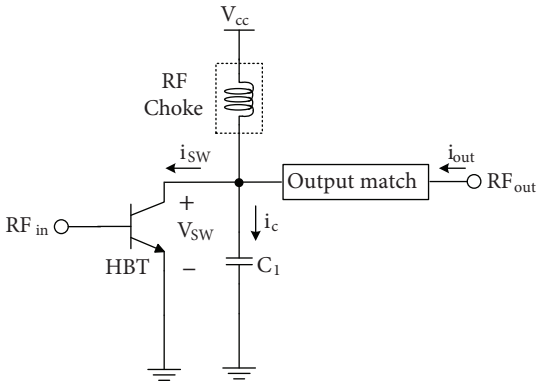

Figure 3. Current and voltage representations in the class-E PA.

The result of Eqs. (2) to (5) are illustrated in Figure 4, which evidently describe a class-E operation.

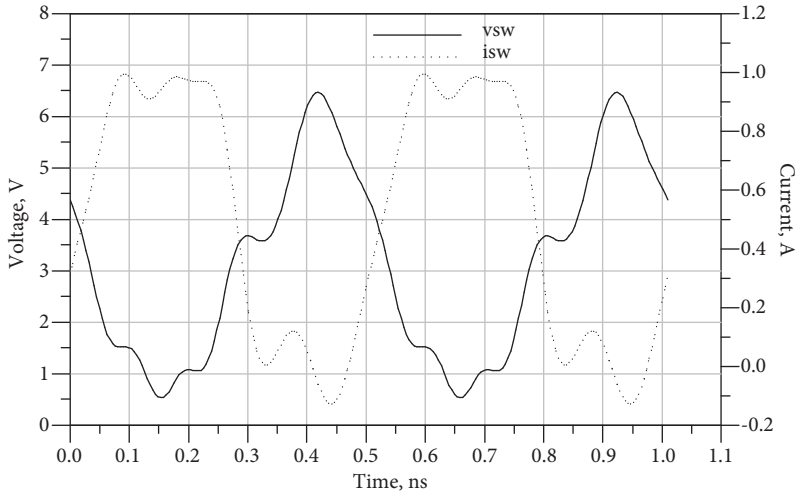

Figure 4. Simulated class-E waveforms.

In Figure 4, the profile shapes of the voltage and current waveforms are distorted due to the significant impact of the harmonic components [2].

2.2. Passive predistortion linearization technique

A class-E PA has high nonlinear characteristics. The nonlinearity is defined as such that the presence of higher-order components, respective to the linear relationship between the output and input voltage of the PA, is given by:

$$v_{out} = K_1 v_{in} + K_2 v_{in}^2 + K_3 v_{in}^3 .... + K_n v_{in}^n, \tag{6}$$

where v_{in}^n is the nonlinear product and K_n is a constant that represent the amplitude and phase of the amplifier. In order to linearize the PA, the nonlinear products in Eq. (6) are driven to have an opposite phase response between the input and output of the PA. The third-order component, $K_3 v_{in}^3$, represents the third intermodulation product IMD3, which has a significant impact on the ACPR performance of the PA. The

relationship between the IMD3 and ACPR is expressed as [14]:

$$ACPR_{dBc} = IMR_{2dBc} + 10\log\left[\frac{n^3}{2\times\left(8\sum_{r=1}^{n-1}N_1(n,r)+2\sum_{r=1}^{n-1}M_1(n,r)\right)}\right], \tag{7}$$

where

$$\begin{array}{l}\sum_{r=1}^{n-1}N_1(n,r)=\frac{2n^3-3n^2}{24}+\frac{\varepsilon}{8}\\ \sum_{r=1}^{n-1}M_1(n,r)=\frac{n^2-\varepsilon}{4}\\ \varepsilon=\mathrm{mod}\left(\frac{n}{2}\right)\end{array}.$$

Here, n represents the number of tones and IMR is the multitone IMD-to-carrier ratio.

In order to eradicate the IMD3 effect at the back-off output power, a passive predistorter is integrated at the input of the PA and conceptually described in Figure 5.

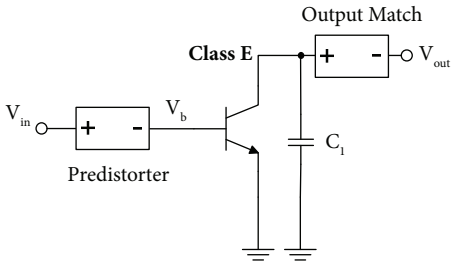

Figure 5. Predistortion concept analysis on a class-E PA.

Referring to Figure 5, the power series is expressed as:

$$f(x)=\sum_{n=0}^{\infty}a_nx^n, \tag{8}$$

$$v_{out}=a_o+a_1v_b+a_2v_b^2+a_3v_b^3, \tag{9}$$

where

$$v_b=b_o+b_1v_{in}+b_2v_{in}^2+b_3v_{in}^3. \tag{10}$$

Taking into consideration the fundamental and third-order component, and substituting Eq. (10) into Eq. (9):

$$\begin{array}{rcl}v_{out} & = & a_1\left(b_1v_{in}+b3v_{in}^3\right)+a_3\left(b_1v_{in}+b_3v_{in}^3\right)^3\\ & = & a_1b_1v_{in}+\left(a_1b_3+a_3b_1^3\right)v_{in}^3+3a_3b_1^2b_3v_{in}^5+3a_3b_1b_3^2v_{in}^7+a_3b_3^3v_{in}^9\end{array} \tag{11}$$

To nullify the third-order component:

$$a_1b_3+a3b_1^3=0, \tag{12}$$

$$b_3=-\frac{a_3b_1^3}{a_1}. \tag{13}$$

By setting the fundamental amplitudes a_1 and b_1 to 1:

$$b_3 = -a_3. \tag{14}$$

In the passive predistorter method, if Eq. (14) is satisfied, the IMD3 component of the nonlinear class E PA is nullified.

3. Simulation results and discussion

Figure 6 illustrates the physical layout view of the class-E PA and the passive predistorter in an active chip area consumption of 1000 μm $\times$ 750 μm.

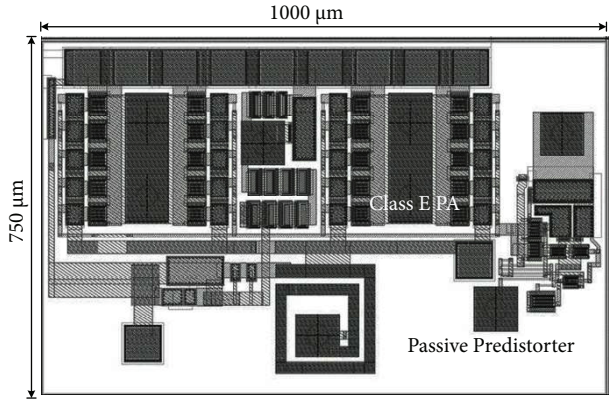

Figure 6. Layout view of the class-E amplifier.

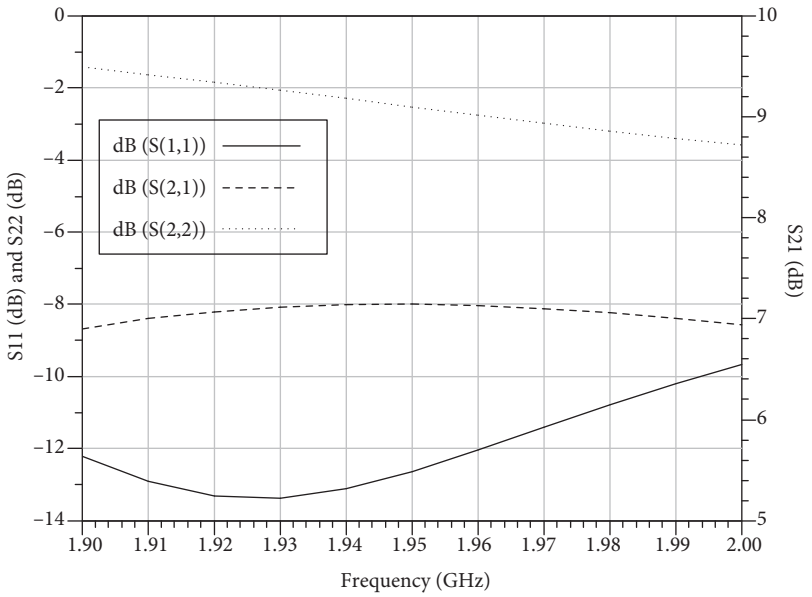

Figure 7. Small signal performance.

The input return loss performance is not compromised in the tradeoff to linearize the PA with an integrated passive predistorter. This is depicted in Figure 7, where the input return loss, S11, is indicated as –12.5 dB at 1.95 GHz, with a corresponding power gain of 7 dB.

The ACPR performance of the PA is simulated, applying the CDMA IS-95 modulated input signal. Figure 8 illustrates the ACPR performance. It can be observed that the ACPR is less than –45 dBc across the output power at 1.95 GHz. The ACPR curve starts to roll-off at 24 dBm of output power. This translates to a lower IMD3 component due to the opposite IMD3 phase response generated by the passive predistorter. At 29 dBm, the simulated ACPR is observed to be –51 dBc. At this power level, the IMD3 phase cancellation is optimum.

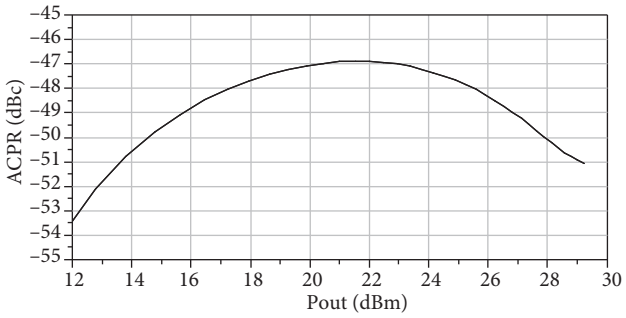

Figure 8. ACPR performance across the output power.

Figure 9 illustrates the spectrum of the PA at 1.95 GHz, prior to and after linearization. It can be observed that prior to linearization the sidebands power are substantially high, almost equivalent to the main spectrum, due to the presence of a high IMD3 component. This is an indication of a nonlinear operation of the class-E PA. By employing the passive linearization scheme, which reduces the IMD3 response of the PA, the sideband powers are relatively low respective to the main channel power. In other words, the predistorter reduces the power from dominating its adjacent channel.

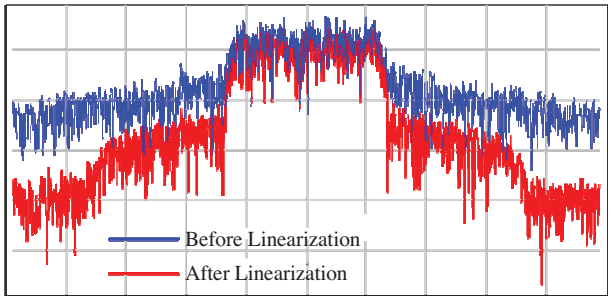

Figure 9. Spectrum of the PA at 1.95 GHz.

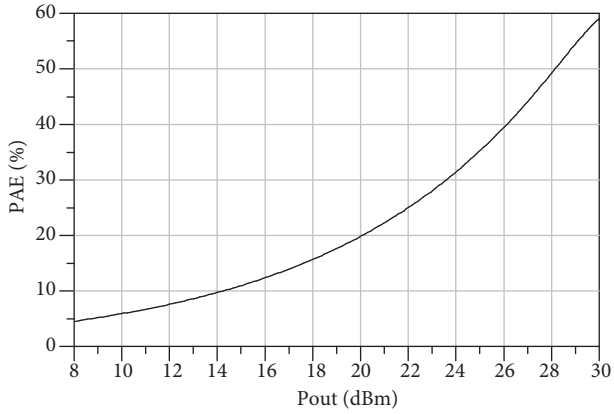

Figure 10. PAE across the output power.

Figure 10 illustrates the PAE performance across the output power, which is 55% at a linear output power of 29 dBm. At the maximum output power of 30 dBm, the PAE is observed to be 60%, ensuring a class-E performance under modulated conditions. The simulated performance summary of the PA is tabulated in Table 1.

Table 2 summarizes the performance comparison of the proposed PA, respective to other recent reported works. It could be deduced that the proposed architecture observes an optimum PAE while satisfying the APCR regulation.

Table 1. Simulated performance summary at 1.95 GHz.

Quantity	Results
Technology	2-μm InGaP/GaAs HBT
Supply	3.4 V
Frequency	1.92 GHz–1.98 GHz
Max linear output power	29 dBm
PAE	55%@29 dBm
S11	–12.5 dB
Gain	7 dB

Table 2. Performance comparison of recent reported works in mobile PA.

Reference	Supply voltage (V) voltage (V)	Max linear output power (dBm) power (dBm)	PAE (%)
[15]	3.4	30.1	46.3
[16]	4.5	27.5	36.3
[17]	3.4	27.2	34.5
This work	3.4	29.0	55.0

4. Conclusion

A class-E PA with an integrated passive predistorter linearizer is designed for mobile wireless applications. The PA is designed to operate across the range of 1.92–1.98 GHz, intended for CDMA applications. The nonlinear class-E amplifier is linearized by the passive predistorter, ensuring a linear operation at up to 29 dBm of output power. At this output power, the delivered PAE is 55%. The proposed linearization scheme delivers a good S11, which is essential to reduce the mismatch loss between the PA and baseband chip, once integrated in the transmitter. This result verifies a highly efficient and linear CDMA PA for mobile wireless communication.

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