Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2015) 23: 505 – 521

doi:10.3906/elk-1304-45

Type III compensated voltage mode line feedforward synchronously rectified boost converter for driving Class D audio H-bridge to deliver 7 W peak power into an 8 Ω speaker

Yavuz KILIÇ*
Dialog Semiconductors UK Ltd., Edinburgh, UK

Received: 05.04.2013 • **Accepted:** 10.04.2013 • **Published Online:** 23.02.2015 • **Printed:** 20.03.2015

Abstract: In this paper, a circuit topology for a synchronously rectified boost converter aimed to act as a power supply for a Class D H-bridge that would deliver up to 7 W peak power into an 8 Ω speaker is presented. The design is implemented in a submicron BCD process technology. Some of the challenges in this design are as follows. The first challenge was to optimise the design such that it would not cause on-chip power dissipation levels that would go beyond acceptable levels for Wafer Level Chip Scale Package (WLCSP), which is a commonly used package for space constrained applications in portable spaces. To address this issue, a Class G mode of operation to deliver multiple boost voltage levels has been proposed. Second, due to the chosen submicron BCD process lacking some devices such as zener diodes to clamp maximum voltages that active device gate-source and/or drain-source terminals in case of transient or normal operating conditions of the circuit, new ways of circuit implementation techniques have been come up with to prevent active devices from being damaged. One more important issue for handheld applications is that it is imperative to choose a small form factor (height and footprint) external inductor, which can also stand up to 4 A for this particular design. The new trend in small footprint power inductors is to use an iron powder core to keep the inductance constant. This creates a new problem with these types of inductors, whereby the series resistance of the inductor would increase with the frequency, which will increase the inductor AC core losses at switching frequencies of the switching converter. Trade-offs between total harmonic distortion plus noise and boosted voltage levels are also studied.

Key words: Boost converter, DC-DC converter, voltage mode, line feedforward, pulse width modulation, synchronous rectification, Class D, Class G, audio, BCD, inductor

1. Introduction

There is a growing demand in the battery operated portable electronics industry for a more efficient yet more powerful power management integrated circuit with audio processing capabilities. The demand for the increase of power is due to the ever-increasing demand for so-called 'more loudness' in portable electronic devices such as mobile phones and tablets. Due to being very efficient, Class D is the choice of amplifier topology for audio applications. Battery voltage for most portable electronic devices such as mobile phones is between 3 V and 4.2 V, and typically the battery voltage is around 3.6 V. Typically, impedance of speakers for mobile applications is 8 Ω.

To cope with the 'more loudness' demand, there is a commercial trend to integrate a boost converter alongside a Class D audio driver on the same chip to maintain the desired output power levels over the battery

*Correspondence: dr_kilic@yahoo.co.uk

voltage range. There are a number of commercially available products such as the LM48510 and TPA2015D1 from Texas Instruments (TI), MAX98502 from Maxim Integrated, and FAB3103 from Fairchild Semiconductors that address this demand, as well as academically published ones such as [1]. The boost converter may be either diode rectified or synchronously rectified. With synchronous rectification, the external recirculation diode is eliminated from the design at the expense of the silicon area used for an on-chip second switch.

With the standard 5 V compliant CMOS processes, the boosted voltage level is reported to vary from 5.4 V to 5.65 V in the abovementioned commercially available products, where the quoted maximum average power levels vary from 2 W at 6% total harmonic distortion plus noise (THD+N) to 2.3 W at 10% THD+N for a 1 kHz sine wave as the audio output into an 8 Ω speaker from a 3.6 V battery voltage level. Even though the attempt to make the delivered power levels look as big as possible is a marketing gimmick, the quality of the delivered power levels into the speaker usually dictates that the THD+N be lower than 1% for the audio signal in the speaker to be distortion-free and without being clipped. With 1% THD+N, the maximum reported power level with 5.65 V boosted voltage level reported in the FAB3103 product is measured at 1.85 W average power into an 8 Ω speaker from 3.6 V battery voltage. To deliver more power than these quoted levels into an 8 Ω speaker at 1% THD+N dictates higher boosted voltage levels.

In this paper, a synchronously rectified boost converter that aims to deliver 7 W peak (or 3.5 W average) power at 1% THD+N into an 8 Ω speaker via Class D amplifier is presented.

2. The proposed type III compensated voltage mode line feedforward synchronously rectified boost converter

DC-DC converters can either operate in continuous current conduction (CCM) or discontinuous current conduction (DCM) mode of operation depending on the input line and output load conditions. DC-DC converters usually employ either current mode (CM) or voltage mode (VM) for the control. The differences in these 2 types of control schemes, VM and CM for DC-DC converters, are discussed in [2], and the debate over which one of these control schemes is better depends on the specific application and the type of DC-DC converter being designed. In general, VM offers simpler design implementation for DC-DC converters compared with CM, where more complicated circuit implementation is required. CM offers simplification of the compensation network around the error amplifier, thus making the LC stage look like a single pole, meaning that one can get away with using type II compensation [2,3]. The theory of DC-DC converters is well studied in the literature and is beyond the scope of this paper. The interested reader is referred to [2—4] to gain insight into the DC-DC converters.

The difference between type II and type III compensation is the addition of an extra resistor and a capacitor in the compensation network to create an additional zero. In the case of boost converters, the crossover frequency (bandwidth) of the closed loop is mainly due to the inherent right hand plane (RHP) zero, which cannot be eliminated by using CM.

Line feedforward is a technique where the disturbances in the input line voltage are sensed and fed directly into the PWM control to make sure the converter does not wait for the output feedback through the error amplifier to correct for these changes [2]. If the input voltage increases, then the slope of the sawtooth ramp is increased to increase the duty cycle, and if the input voltage is decreased, then the slope of the sawtooth ramp is decreased to decrease the duty cycle. Line feedforward is only applicable to the VM DC-DC converters [2].

For the reasons discussed above, type III compensation with VM and line feedforward was used for the proposed boost converter design.

2.1. Boost converter

The block diagram of the proposed boost converter is given in Figure 1. As can be seen in the block diagram, there are a few circuit blocks that are used to construct the boost converter, together with the external inductor, L, and the external capacitor, Co. It can also be seen in this block diagram that the load is considered to be a Class D audio H-bridge driver. The Class D H-bridge then drives an 8 Ω speaker. The main building blocks of the boost converter are the error amplifier and on-chip implemented type III compensation network, line feedforward ramp oscillator, PWM comparator, minimum and maximum duty limiter, boost control, and power stage. Circuit implementations in the chosen submicron BCD process for some of these blocks are given in Figures 2 through 8. The error amplifier, in conjunction with the type III compensation network, senses the output boost voltage and compares it with a reference voltage, vref, and then creates an error voltage, verr, which is then compared with the sawtooth ramp. The line feedforward ramp oscillator generates a sawtooth ramp signal whose peak amplitude changes with the input voltage, vbat, while the frequency of the oscillation remains fixed. That means the changes in the input voltage will directly change the duty cycle of the signal out of the PWM comparator, without waiting for the whole boost feedback loop from the output to react to those changes. The power state comprises the power switches: the main control switch, NMOS, and the synchronously rectifying switch, PMOS, and the predrive for driving the power switches. The predrive block to drive the power switches incorporates a proprietary multilevel floating ground scheme to drive the PMOS power switch.

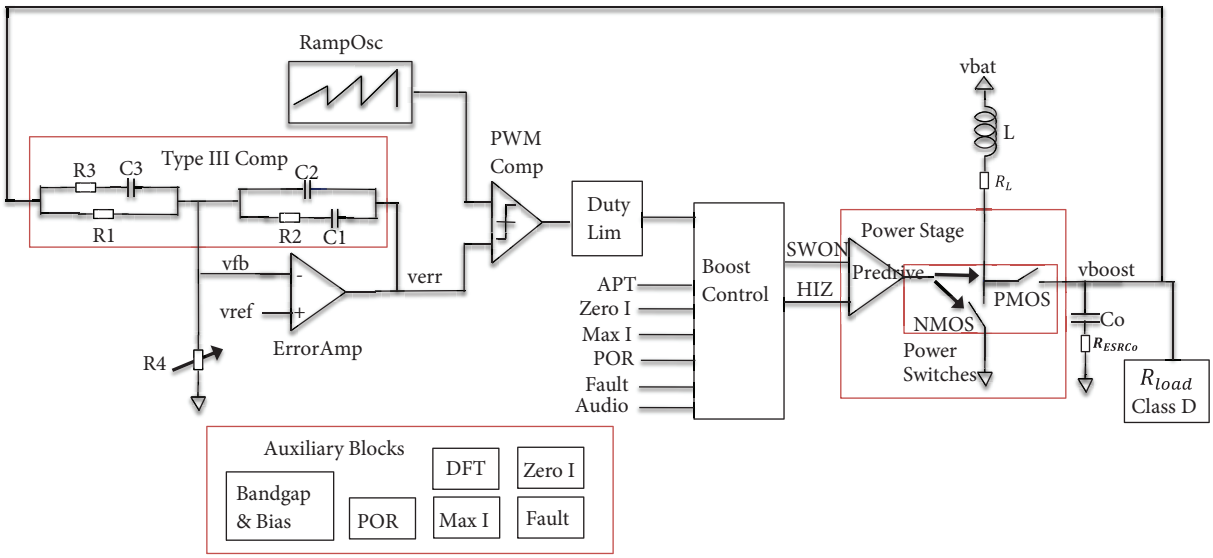

Figure 1. Block diagram of the proposed type III compensated VM line feedforward synchronously rectified boost converter.

The boost control block generates 2 signals, SWON and HIZ. SWON is basically an on/off signal for the power switches (if one switch is on, the other is off), and HIZ is a signal to turn both switches off in the event of the detection of overvoltage at the output of the boost converter. The APT signal to the boost control block is the so-called auto pass through mode, whereby the PMOS switch is permanently turned on while the NMOS switch is permanently turned off to ensure that the input supply, vbat, is connected to the output. The POR signal to the boost control block is the "power on reset" signal, Zero I is the inductor zero current detect signal,

Max I is the maximum inductor current signal, Fault indicates the fault condition signals, and Audio is the input audio demand indicator signal.

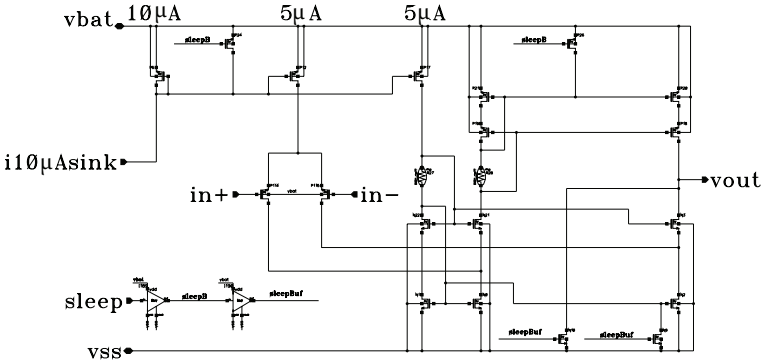

Figure 2. Error amplifier.

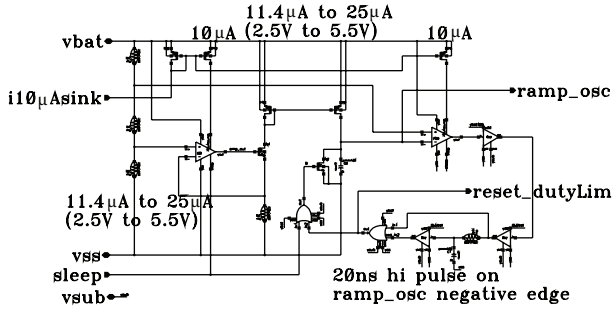

Figure 3. Line feedforward ramp oscillator.

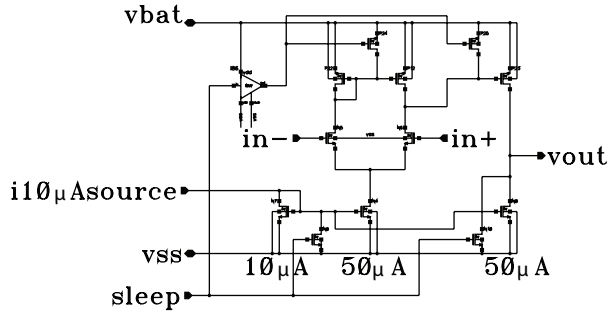

Figure 4. PWM comparator.

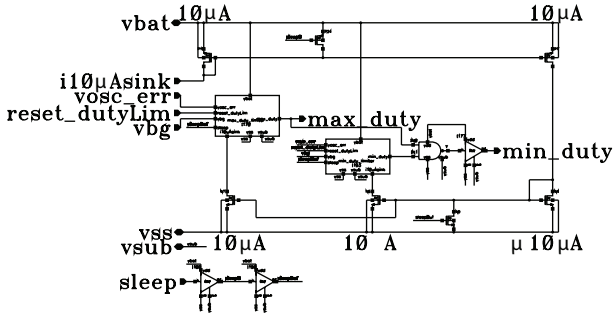

Figure 5. Min–max duty limit circuit.

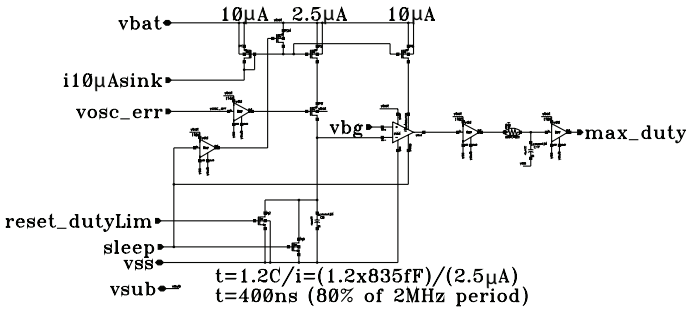

Figure 6. Max duty limiter.

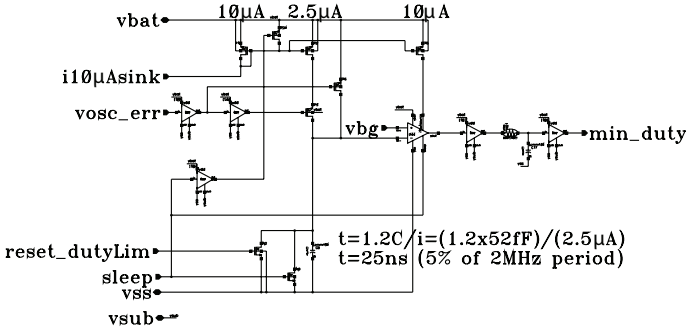

Figure 7. Min duty limiter.

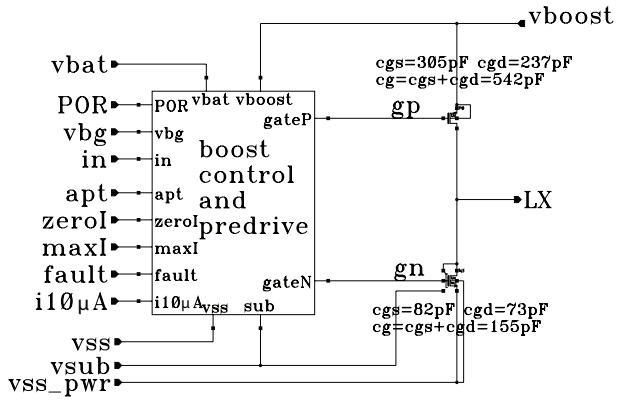

Figure 8. Power stage including the control.

The duty cycle for a boost converter can be given by:

$$D = 1 - \frac{v_{bat} \times efficiency}{v_{boost}}. \tag{1}$$

The efficiency term in Eq. (1) is an empirical constant that is factored in to account for the efficiency of the whole boost converter together with the Class D H-bridge driver due to on-chip power losses and off-chip power losses. The total efficiency to deliver 2 W average power into the 8 Ω speaker from the 3.6 V battery supply is quoted in the TPA2015D1 product datasheet mentioned above to be around 77%, compared with the efficiency figure of around 82% when delivering 1 W average power into an 8 Ω speaker from a 3.6 V battery supply. This means that the total efficiency drops around 5% when the power is increased by 1 W. The efficiency will be

much worse when delivering 3.5 W average power into an 8 Ω speaker and will be approximately 70%. There exists a relationship between the maximum conversion ratio from the boosted voltage to the input voltage, $M = \frac{vboost}{vbat}$, and the maximum allowed duty cycle, $D_{\max}$ [4]. While the detailed explanation of this is outside the scope of this paper and can be found in [4], this is mainly due to the inductor DC and AC resistances, which force the conversion to reach a peak and then tend to zero as the duty cycle approaches 1. Therefore, in order for the boost converter to not operate in the unstable region where the M curve is negative, the duty limiter block makes sure that the duty limit is set to a maximum level governed by the design under consideration.

In addition to the major building blocks mentioned above, there are also a few auxiliary circuit blocks that create the reference voltage, biases, POR, etc., which are depicted in Figure 1.

The closed loop boost converter can also be drawn as given in Figure 9 to show its plant and feedback blocks [2]. The transfer function of the plant, $G(s)$, which is also called the "control-to-output transfer function", has been well studied in the literature [2—4] and can be given by:

$$G(s) = G_{DC} \times \frac{\left(1+\frac{s}{\omega_{zESRCo}}\right) \times \left(1-\frac{s}{\omega_{zRHP}}\right)}{1+\frac{s}{\omega_{pLC} \times Q}+\frac{s^2}{\omega_{pLC}^2}} \tag{2}$$

where the DC gain, G_{DC}, is given by:

$$G_{DC} = \frac{1}{vramp} \times \frac{vbat}{(1-D)^2} \tag{3}$$

where vramp is the amplitude of the sawtooth ramp and vbat is the input voltage. From Eq. (2), it can be seen that the boost converter has a double-pole frequency due to the L-C network, which can be given by:

$$f_{pLC} = \frac{1}{2\pi\sqrt{(L \times C)}} \times \sqrt{\frac{R_L + (1-D)^2 \times R_{load}}{R_{load}}} \tag{4}$$

and the quality factor, Q, is given by:

$$Q = \frac{\omega_{pLC}}{\frac{R_L}{L}+\frac{1}{C_o \times (R_{load}+R_{ESRCo})}} \quad . \tag{5}$$

The output capacitor ESR zero can be given by:

$$f_{zESRCo} = \frac{1}{2\pi \times R_{ESRCo} \times Co} \quad . \tag{6}$$

The RHP zero can be given by:

$$f_{zRHP} = \frac{(1-D)^2 \times (R_{load}-R_L)}{2\pi \times L}. \tag{7}$$

The effect of the RHP zero on the boost converter system is such that if the converter is in the unstable mode of operation due to the RHP zero, the NMOS switch is on for a longer time to charge the inductor with more energy to try to boost to the desired level. If the NMOS switch is on for longer periods of time, there will not be enough time left to connect the inductor to the output capacitor via the PMOS switch. Since the inductor is disconnected from the load for a long period of time, this will cause the output voltage to drop while the system

is trying to increase the output voltage. As a result of this, the control loop cannot act in time to stabilize the boosted voltage; hence, the whole system will oscillate. Another way to think of the RHP zero effect is to look at it in the frequency domain; while the RHP zero increases the gain, it also causes the phase to drop, degrading the stability of the whole system. Hence, to prevent the RHP zero from causing system instability, the bandwidth of the whole closed loop boost converter should be limited to be much lower than the RHP zero frequency; a good rule of thumb would be to limit the closed loop system bandwidth to be at least 4–6 times lower than the RHP zero frequency.

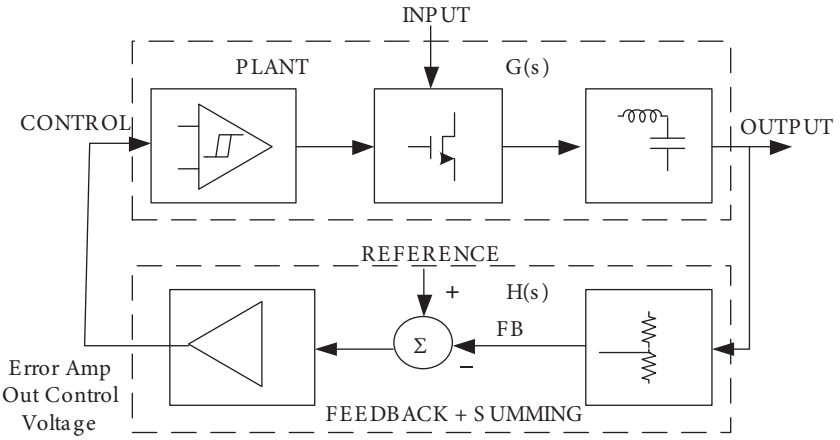

Figure 9. Closed loop boost converter redrawn to show plant and feedback blocks [2].

The Bode plot of the plant transfer function given in Eq. (2) is depicted in Figure 10. This is a simplified plot where an assumption is made such that f_{pLC}, f_{zESRCo}, f_{zRHP} are all well apart from each other by 2 orders of magnitude in the frequency axis, so that one can clearly show the effects of all these poles and zeros on the gain and phase independently. It is also assumed that ESR zero kicks in before the RHP zero does. There will also be other poles at higher frequencies due to unwanted parasitic R and C in the system, which are not shown in Eq. (2). Depending on the DC gain, G_{DC}; the location of the double pole, ESR zero, and RHP zero; and higher frequency parasitic poles, the gain will cross 0 dB at different frequencies. In the next section, the need for compensating for the plant function is discussed.

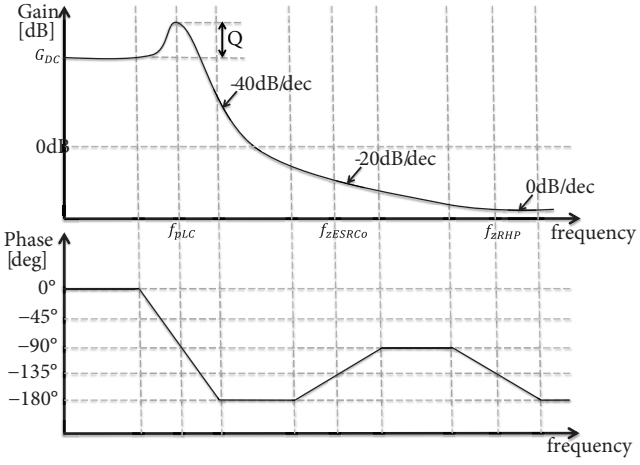

Figure 10. Bode plot of the boost converter plant stage.

2.2. Type III compensation for the boost converter

Before one can discuss type III compensation for the boost converter, one should look at the specific requirements for the boost converter one tries to implement. As mentioned in Section 1, the intent is to deliver 3.5 W average power, $P_{speakerAVG}$, into an 8 Ω speaker from the Class D H-bridge driver from a 3.6 V battery supply. The boost converter will act as a power supply to the Class D H-bridge driver. The output power into the 8 Ω speaker can be given by the following equation:

$$P_{speakerAVG}=\frac{V^2_{speakerRMS}}{R_{speaker}}. \tag{8}$$

As the speaker is 8 Ω and the power is 3.5 W average, the RMS voltage across the speaker can easily be calculated:

$$V_{speakerRMS}=\sqrt{(P_{speakerAVG}\times R_{speaker})}=5.29\,V \tag{9}$$

This means that the peak value of the speaker voltage will be 7.48 V. There will be some losses due to the Class D H-bridge driver. It is desired to achieve less than 1% THD+N in order for the audio signal in the speaker to not be clipped or distorted. Because of this, one would need to boost the voltage to be larger than 7.48 V. Class D H-bridge drivers operate very efficiently and typically achieve efficiencies over 90%. If this is taken into account, one will need the boosted voltage to the Class D H-bridge to be some 10% or so more than the required 7.48 V across the speaker. This means that the boosted voltage level should be 8.23 V. The expected total efficiency of the boost converter and the Class D H-bridge system was expected to be around 70%, as mentioned in Section 2.1. By plugging this efficiency figure, the needed boosted voltage level of 8.23 V, and the input battery voltage of 3.6 V into Eq. (1), one can easily find the peak duty cycle, D_{peak}, to be around 69.38%, which suggests that the boost converter is working in CCM. Eq. (8) for power delivered into the speaker could also be written as:

$$P_{speakerAVG}=I^2_{speakerRMS}\times R_{speaker} \tag{10}$$

From this equation, one could calculate the peak speaker current to be:

$$I_{speakerPEAK}=\sqrt{\left(P_{speakerAVG}/R_{speaker}\right)}\times\sqrt{2}=935.4\,mA \tag{11}$$

Average inductor current for a boost converter operating in the CCM can be given by:

$$I_{L(AVG)}=\frac{I_{load}\times v_{boost}}{v_{bat}\times efficiency} \tag{12}$$

If one plugs the value of 935.4 mA for the load current calculated in Eq. (11) together with the boosted voltage of 8.23 V from 3.6 V input battery voltage with the total system efficiency of 70% into Eq. (12), the average inductor current can then be calculated to be around 3 A. For a boost converter operating in CCM, the inductor ripple current should be around 33% to 50% of the average inductor current, while the optimum value of the inductor ripple current is 40% of the average inductor current [2]. This means that when boosting to 8.23 V from a 3.6 V input battery with total system efficiency of 70%, the maximum inductor ripple current should be around 1 A. The peak inductor current would be the summation of the average inductor current and half of the

ripple current, and thus the peak inductor current will be 3.5 A for our case. With the inductance tolerances, temperature, etc., the chosen inductor for this type of application should be able to handle more than this peak current of 3.5 A by at least 25%, meaning that one needs an inductor that can handle over 4 A.

For battery operated portable electronic devices, the feature size of components tends to shrink at the pace of technological advancement in industry. In line with this, the form factor used for the inductors and capacitors for battery operated portable electronic devices is also forced to get smaller and smaller, and the preferred trend is for the inductor height to be less than 1 mm. At the time of writing this paper, there was no standard inductor released by manufacturers that would handle above 4 A with a form factor of 1 mm or less height. The new trend for inductor manufacturers is to use an iron powder core as opposed to a ferrite core in order to keep the inductance flat over operating frequency and temperature ranges. The problem with the iron powder core used for inductors is that it makes the undesired series resistance of the inductor go up as the switching frequencies increase for the DC-DC converters. Not only will this increase in the inductor series resistance increase the off-chip dissipated power levels, but it will also lower the RHP zero frequency and decrease Q of the system according to Eqs. (5) and (7). An example of an inductor that would handle more than 4 A but not satisfy the requirement of 1 mm or less height would be the Coilcraft XFL4020 1 μH inductor. The quoted DC resistance of the Coilcraft XFL4020 1 μH inductor is 10.8 mΩ, and due to the iron powder core heating at higher switching frequencies, this series inductance value could be increased by an order of magnitude. For this paper, the value of series resistance of the Coilcraft XFL4020 1 μH inductor is considered to be 100 mΩ.

A reasonable choice for the output capacitor could be the Murata 0805 X5R 10 μF capacitor for this type of application, which has an ESR of 260 mΩ at 2 MHz switching frequency. A good compromise in the design implementation of the proposed boost converter could be achieved at 2 MHz switching frequency, while keeping the inductor size as low as 1 μH and the output capacitor size of 10 μF to give acceptable output voltage ripple, and yet optimizing for the on-chip dissipated power levels due to switching frequency. Based on the information given above and the fact that the amplitude of the ramp of the line feedforward sawtooth oscillator used is nearly the same as the input battery supply voltage, one can calculate the values of the duty cycle, DC gain, Q, double pole frequency, ESR zero frequency, and RHP zero frequency by using Eqs. (1), (3), and (4)–(7). The calculated values for the double pole, ESR zero, and RHP zero frequencies are given in Table 1. As can be seen from the results given in Table 1, the double pole, ESR zero, and RHP zero are located less than an order of magnitude apart from one another in the frequency domain. The gain at double pole frequency goes up to around 33.57 dB with Q of 4.5, which is 13 dB. The gain will go down to around 21 dB or so nearing the ESR zero due to –40 dB/decade slope coming from the L-C. The gain will then probably will go down a few more dB due to the gain slope changing to –20 dB/decade due to the ESR zero, and then the gain will stay flat once reaching the RHP zero. The phase, however, will have shifted down by 180° at around 10 times the RHP zero. Due to the parasitic poles at high frequencies, by the time the gain crosses 0 dB, the phase shift will get below 180°, meaning that the system is unstable. The values given in Table 1 are for only one line and load condition. As the line, load, and inductor series resistance and capacitor ESR change, the locations of double pole, ESR zero, RHP zero, and higher frequency poles and the value of the Q will change, making the system unstable at different frequencies.

There are disturbances in the plant stage of the boost converter, which are the line and the load variations. To suppress these effects and also keep the boosted voltage at a stable level, one needs a feedback stage around the boost converter, from the output of the boost converter into the plant stage. Usually, the first step of implementing a feedback stage is to realize an integrator function together with the error amplifier, creating a

pole at zero [2]. Even if one only had this integrator function within the feedback stage, this would mean that the gain of the closed loop system will be starting from –20 dB/decade from DC due to this integrator function and then go to –60 dB/decade after the double pole due to the L-C stage.

Table 1. Calculated double pole, ESR zero, and RHP zero frequencies using a Coilcraft XFL4020 1 μH inductor, Murata 0805 X5R 10 μF capacitor, 2 MHz switching frequency.

vbat [V]	vboost [V]	$P_{speakerAVG}$ [W]	Duty cycle [%]	DC Gain [dB]	Q [dB]	f_{pLC} [kHz]	f_{zESRCo} [kHz]	f_{zRHP} [kHz]
3.6	8.23	3.5	69.4	20.57	13	16.39	61.2	119

For the reasons explained above, one needs the feedback section in the boost converter, which consists of the error amplifier and the compensation network around it. As one needs to compensate for a double pole and 2 zeros, one needs a type III compensation network, which is also called double lead-lag/lag and has a pole at zero from the integrator, 2 poles, and 2 zeroes. The error amplifier with the type III compensation network is given in Figure 1.

The derivation of the transfer function of the feedback stage type III compensation network, $H(s)$, is beyond the scope of this paper, as it is well studied in the literature [2—4], and can be given by:

$$H\left(s\right)=\frac{\omega_{p0}}{s}\times\frac{\left(1+\frac{s}{\omega_{z1}}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \tag{13}$$

where ω_{p0} is the crossover frequency of the pole at zero due to the integrator, and a further 2 zeroes ω_{z1}, ω_{z2} to cancel the double pole of the plant function due to the L-C, and 2 poles ω_{p1}, ω_{p2} to cancel the ESR and RHP zeroes, making sure that the closed loop gain crosses 0 dB at a specified frequency while maintaining enough phase margin for the whole system to be stable. If one relates the poles and zeroes of Eq. (13) with the type III network given in Figure 1, one can write the following equations [2]:

$$f_{p0}=\frac{1}{2\pi R_1(C_1+C_2)}, f_{p1}=\frac{1}{2\pi R_2C_e}, f_{p2}=\frac{1}{2\pi R_3C_3}, f_{z1}=\frac{1}{2\pi R_2C_1} f_{z2}=\frac{1}{2\pi(R_1+R_3)C_3} \tag{14}$$

where

$$C_e=\frac{C_1C_2}{C_1+C_2}. \tag{15}$$

With the addition of the feedback function into the boost system, the simplified closed loop boost converter could be given as shown in Figure 11 [2]. From this block diagram, one can write the following equations for the closed and open loop gain:

$$\frac{OUT}{IN}=\frac{G}{1+GH}=\frac{G}{1+T}\ \left(closed\,loop\,gain\right), \tag{16}$$

$$T=GxH\left(open\,loop\,gain\right). \tag{17}$$

From the control theory it is known that if $T=-1$ for the closed loop transfer function the system will be unstable. The stability of the loop is ensured when the open loop gain, T, crosses the 0 dB axis with a –20 dB/decade slope. To maximize the bandwidth to achieve quick response to step changes of load or line, the

crossover frequency of the open loop gain, f_{OLx}, should be chosen to be as high as possible. From the sampling theory, it is known that the crossover frequency must be less than the switching frequency, which is the case for the boost converter presented in this paper. One also must make sure that the crossover frequency is well below any troublesome poles or zeroes (RHP zero in our case, and 'subharmonic instability pole' in the case of current mode control in CCM). The open loop crossover frequency for the boost converter presented in this paper is chosen to be one-sixth of the worst value of RHP zero frequency. As the worst case RHP zero was calculated in Table 1 to be 119 kHz, the open loop crossover frequency is chosen to be around 20 kHz for the boost converter presented in this paper.

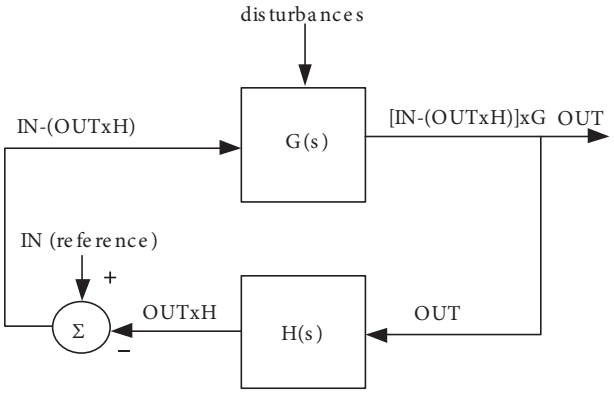

Figure 11. Simplified closed loop boost converter.

As mentioned above, the loop gain, $T(s)$, is a cascade of the plant transfer function, $G(s)$, and the feedback transfer function, $H(s)$. Knowing this, one can write the following relationship between f_{p0} and f_{OLx}:

$$f_{OLx}=G_{DC}\times f_{p0}. \tag{18}$$

The compensating zeroes are usually placed at half of the LC pole frequency (which gives a $2\times$ gain boost of 6 dB):

$$f_{z1}=f_{z2}=\frac{1}{2}f_{pLC}, \tag{19}$$

and the compensating poles are placed at the ESR zero frequency, as it is lower than RHP zero for the boost converter presented in this paper:

$$f_{p1}=f_{p2}=f_{zESRCo}. \tag{20}$$

Generally, C_1 is much bigger than C_2 in the type III compensation network given in Figure 1. Using this assumption and plugging Eqs. (18)–(20) into Eq. (14), one can write the following relationships between the poles, zeroes, and passive component values of the compensation network:

$$C_1=\frac{1}{2\pi f_{UG}R_1A_c}, \tag{21}$$

$$R_2=\frac{1}{2\pi f_{z1}C_1}, \tag{22}$$

$$C_2=\frac{1}{2\pi f_{zESRCo}R_2}, \tag{23}$$

$$C_3=\frac{\frac{2}{f_{pLC}}-\frac{1}{f_{zESRCo}}}{2\pi R_1}, \tag{24}$$

$$R_3=\frac{1}{2\pi f_{zESRCo}C_3}, \tag{25}$$

$$R_1=\frac{1}{\pi f_{pLC}C_3}-R_3. \tag{26}$$

If an initial value of 2.3 MΩ is chosen for the resistor, R_1, and the values calculated in Table 1 are plugged into Eqs. (21)–(26), one could calculate the values of the passive components easily, which are given in Table 2. As can be seen in Table 2, the values of the passive components are at levels where they can be implemented on chip without too much area penalty. The total area required to implement these passive resistors and capacitors in the chosen submicron BCD process technology would be a reasonably small die area overhead.

Table 2. Passive component values of the type III compensation network.

R_1 [MΩ]	C_1 [pF]	C_2 [pF]	R_2 [MΩ]	R_3 [MΩ]	C_3 [pF]
2.3	40.39	5.04	0.516	0.328	7.93

2.3. Boost converter efficiency and power dissipation

A simplified block diagram of a switching power converter is shown in Figure 12. The efficiency of a switching power converter is given by:

$$\eta_{eff}=\frac{P_o}{P_{in}}. \tag{27}$$

The losses in a power converter are static and dynamic losses. Static losses are switch-on resistance (RDSON), ESR, inductor series resistance, R_L, and quiescent current losses. Dynamic losses are gate drive, dynamic switching, reverse recovery, and core losses. In this paper, reverse recovery and core losses will not be discussed.

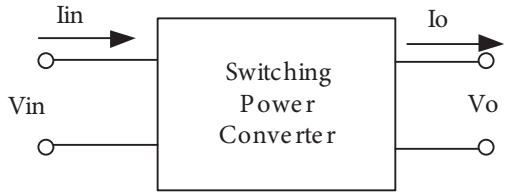

Figure 12. Simplified block diagram of a switching power converter.

For a synchronously rectified boost converter, the losses mentioned above are well studied in the literature and can be given by the below equations [2]:

$$Switch\,on-resistance\,loss: R_{dson}\left(\frac{I_o^2}{(1-D)^2}+\frac{\Delta I^2}{12}\right) \tag{28}$$

$$ESR\,loss: R_{ESRCo}\left(\frac{D^2I_o^2}{(1-D)^2}+\frac{\Delta I^2}{12}\right)(1-D)+I_o^2R_{ESRCo}D, \tag{29}$$

$$DCR\,loss: R_L\left(\frac{I_o^2}{(1-D)^2}+\frac{\Delta I^2}{12}\right), \tag{30}$$

$$Quiescent\,current\,loss : v_{bat} I_Q, \tag{31}$$

$$Gate\,drive\,loss : 2C_g v_o^2 f_s, \tag{32}$$

$$Dynamic\,switching\,loss : \frac{\mathbf{2v_o t_s f_s}}{\mathbf{3}} \left(\frac{\mathbf{I_o}}{\mathbf{1-D}} + \frac{\mathbf{\Delta I}}{\mathbf{2}} \right), \tag{33}$$

where t_s is the crossover time or transition time that is required from the switch being turned on to voltage across the switch going to its minimum (this could be simplified as the turn on/off time of the switch itself), and f_s is the switching frequency. There will be an additional loss due to the increase in the series resistance of the inductor switching at 2 MHz for the boost converter presented in this paper. This loss is not discussed in this paper. The ESR and DCR related losses are off-chip.

As a numerical example for the synchronously rectified boost converter presented in this paper, when delivering 3.5 W average power into an 8 Ω speaker from 3.6 V input battery voltage when a 1 kHz sine wave is presented as the audio signal, the on-chip and off-chip losses can be calculated using Eqs. (28)–(33). For this numerical example, t_s is assumed to be 20 ns, and on resistance of the on-chip power switches is designed to be 150 mΩ, which gives around 542 pF total gate capacitance for the PMOS power switch and 155 pF for the NMOS power switch when both switches are implemented in the chosen submicron BCD process technology. As the input audio signal is assumed to be a 1 kHz sine wave playing through the 8 Ω speaker, the calculation done before for the duty cycle needs to reflect this. To simplify matters, the duty cycle calculated before and given in Table 1 is reduced by around 6%, which is an empirical factoring based on calculation and simulation comparison; since it is beyond the scope of this paper, it is not presented here. The new duty cycle will be around 65%. As the quiescent current related losses are going to be negligible compared with other losses when the boost converter is heavily loaded, they are not taken into account in this paper. Based on the information given above, the losses are calculated and presented in Table 3. As can be seen, the efficiency of the boost converter at heavy load is calculated to be 76.79%. It can also be seen that the total on-chip dissipation due to the boost converter alone is 0.828 W. If the Class D H-bridge driver is operating at 90% efficiency, this would contribute approximately 0.35 W on-chip power dissipation due to the Class D H-bridge switches, making the total system's on-chip loss 1.178 W. If this loss is also added to the total boost losses, then the efficiency of the whole system is calculated to be around 70%.

Table 3. Boost converter losses.

Pin [W]	RDSON [W]	Gate drive [W]	Dynamics [W]	ESR [W]	DCR [W]	Total on-chip [W]	Total off-chip [W]	η_{eff} [%]
4.904	0.312	0.095	0.421	0.187	0.123	0.828	0.31	76.79

The thermal resistance, θ_{JA}, of the 16-ball WLCSP package is given to be around $153\,^{\circ}C/W$ in the datasheet of the TI TPA2015D1 product. With this in mind, if one tries to see what ambient temperature the boost converter together with the Class D audio driver can be operated at, considering that the silicon junction temperature is not to exceed $150\,^{\circ}C$, the following equation can be used:

$$T_{ambientMAX} = 150 - \theta_{JA} \times P_{loss_{onchip}}. \tag{34}$$

By plugging the value of θ_{JA} quoted above into Eq. (34), the maximum ambient temperature can be calculated to be $-30.23\,^{\circ}C$, which is not very practical. In order to operate up to ambient temperatures of $85\,^{\circ}C$, the θ_{JA}

of the package and the printed circuit board (PCB) should be less than $55\,^{\circ}C/W$. It is therefore important to come up with new ways to reduce on-chip power dissipation to allow usage of the cheap WLCSP package and PCB. In this paper, a new method is presented to reduce the on-chip power dissipation by using the Class G mode of operation on the boosted voltage. In this way, there are a number of different levels of boosted voltage depending on the load demand from the Class D H-bridge. As can be also seen from Eqs. (28)–(33), the on- and off-chip power dissipation is not only related to the boosted voltage level but is also related to current from the input battery voltage into the inductor, which is the current through the on-chip power switches, and the external capacitor. This means that if the current is not limited, this will cause extra on- and off-chip dissipation unnecessarily. To that end, the Class G operation is also implemented to the inductor current as well, meaning that for each boosted voltage level, there will be a related maximum current limit level as well. The next section discusses this, and also gives simulation results of the new method.

2.4. Class G mode of operation for the boost converter and simulation results

As discussed in the previous section, it is very important to reduce the on-chip dissipated power to allow use of cheap package and PCB technologies. In order to do that, this study proposes to use the Class G mode of operation on the boost converter. This means that there will be several boosted voltage levels depending on the load demand. As the load itself is directly dependent on the audio signal, this will have implications for the number of levels one can use in the Class G mode of operation for the boost converter.

Audio signals have a frequency range from a few hundred Hz up to 22 kHz; this means that 44 kHz is the highest frequency that the Class D will demand from the boost converter. This frequency will double for the peak levels of the load demand, i.e. from no load to the peak, and from peak to no load demand (assuming a sine wave), meaning 88 kHz frequency is the highest frequency of the load demanded from the boost converter. This is over 4 times more than the open loop crossover frequency that has been chosen for the entire boost converter. The theoretical max audio frequency that can be used as the load for the boost converter will be 5 kHz. Luckily, for this type of application, the THD+N is specified at 1 kHz sine wave audio signal. At 1 kHz audio signal, the peak of the load demand will be 4 kHz, meaning 250 μs is the total time the boost converter has to reach its final value. As the open loop bandwidth is chosen to be 20 kHz, this means the boost converter will have 50 μs to reach its final value. From this, one can say that the maximum level of Class G operation for the boost converter can be calculated to be 5 levels (250 μs / 50 μs). Therefore, 5 levels of Class G operation have been chosen to be used with the boost converter presented in this paper.

A number of simulations were run with the boost converter design having 1 level and 5 levels, which were then loaded with the Class D H-bridge driving 3.5 W average power into an 8 Ω speaker with 1 kHz sine wave input. The simulation results are given in Table 4, Figure 13, and Figure 14. It can be seen from the results presented in Table 4 that by using 5 levels in Class G mode with the boost converter, 62 mW of on-chip dissipated power is saved compared to the single level boost converter. While this level of power saving is not very big when the boost converter runs with heavy loads, operating the boost converter with 5 levels means that the whole system will be much more efficient at lighter loads. This means that if the load demand is not very high, the boosted voltage level will also be regulated at a lower level as well as the inductor current. This causes the whole system to run cooler and causes less on-chip and off-chip power dissipation, which can be seen from Eqs. (28)(33). At very light loads, the boost converter operates in a discontinuous mode of operation to improve efficiency. The comparison of the boost converter design presented in this study with previous work is given in Table 5.

The chosen submicron BCD process technology lacks active clamping components such as zener diodes. This is not well suited to applications such as boost converters, where the power switches have inductive load. With the unwanted parasitic inductances due to the package and PCB, this means that when on-chip power switches are switched with less than 10 ns, the voltages seen at the device drain and source terminals will get very large spikes and make the gate-to-source voltages of the on-chip power device go way beyond their maximum allowed levels by the process technology. One way to reduce these large voltage spikes is to implement the slew-control on the turn on/off time of the switches. Slew rate control for the switches has been implemented within the predrive section of the boost converter presented in this paper.

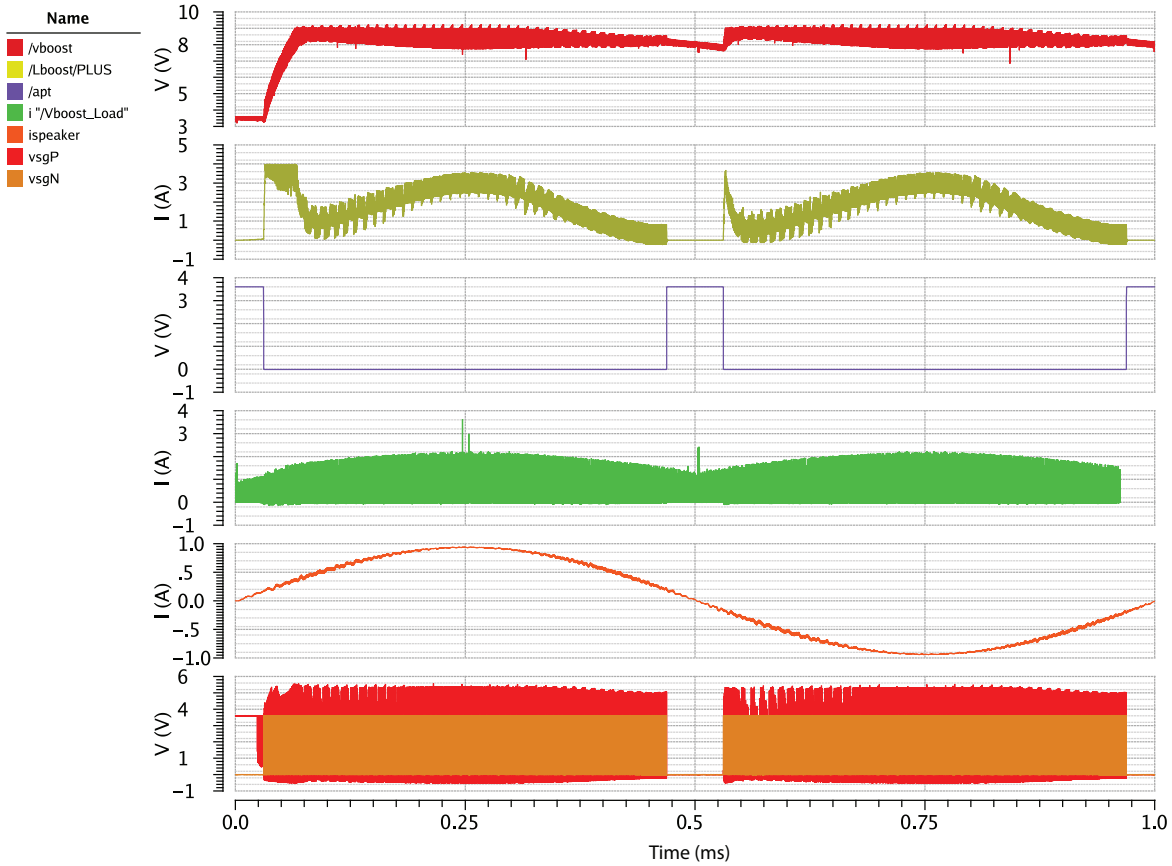

Figure 13. Simulation results for the single level boost converter.

Table 4. Simulated results for single level and multilevel boost converter.

vbat = 3V6, 1 kHz audio input, 3.5 W delivered into 8 Ω speaker								
Levels	Pvbat [W]	Pboost [W]	Pspeaker [W]	Boost on-chip_loss [W]	Class D on-chip_loss [W]	boost efficiency [%]	Class D efficiency [%]	Simulated THD [%]
1	5.007	3.786	3.5	0.847	0.286	75.61	92.45	0.39
5	4.954	3.769	3.5	0.785	0.269	76.08	92.86	1

Another problem with the boost converter driving inductive speakers through the Class D H-bridge driver is an undesired increase in the boost voltage. As the speakers are nonlinear loads with varying impedance over

the audio frequency range, a portion of speaker load current could flow back into the boost converter output capacitor via the Class D H-bridge. This could increase the boosted voltage level to go beyond the maximum allowed levels dictated by the process technology for the on-chip devices and maximum allowed levels for the external components dictated by the external component manufacturers. One way to solve this problem is to use an external zener clamp of suitable clamp level on the boost converter output voltage. Another way to solve this problem is to first put the boost converter into high impedance mode, whereby it is disconnected from the boost output capacitor. A voltage comparator from the boost voltage could keep monitoring the boost voltage, and if it goes beyond a set threshold then an internal circuitry could sink current from the boost converter output capacitor via on-chip circuitry to make sure the boost level stays within defined and well-behaved levels. The high impedance method and the current sinking method are also implemented in the boost converter presented in this paper.

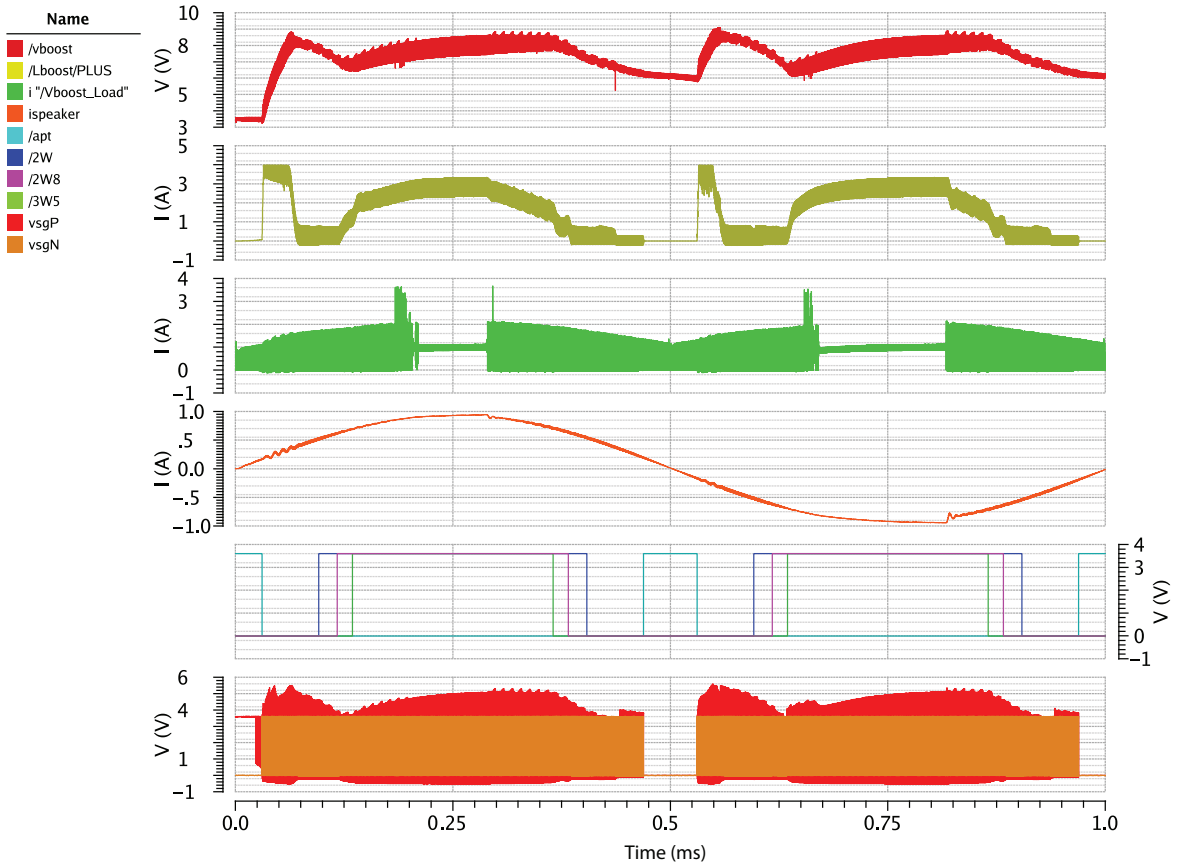

Figure 14. Simulation results for the 5-level boost converter.

3. Conclusion

In this paper, a boost converter that could drive a Class D H-bridge audio driver that could deliver up to 7 W peak power into an 8 Ω speaker is presented. The boost converter is operated in the Class G mode of operation by carefully selecting a number of levels of boosted voltage and inductor current depending on the load demand. The boost converter operates in the discontinuous mode of operation at light loads to improve efficiency. The high impedance mode of operation, together with the current sinking capability, were also implemented to make

Table 5. Comparison of the boost converter presented in this study with previous work.

	LM48510	TPA2015D1	MAX98502	FAB3103	This work	Units
Input supply range	2.7–5	2.5–5.2	2.5–5.5	2.5–5.2	2.5–5.5	V
Package	LLP	WLCSP	WLCSP	WLCSP	WLCSP	
Max boosted voltage level	5	5.4	5.65	5.75	8.2	V
Inductor	4.7	2.2	2.2	2.2	1	μH
Output power (THD+N = 1%, fin = 1 kHz)	1.7	1.7	1.7	1.85	3.5	W
Boost converter efficiency (Iout = 100 mA)	76	88	85	85	90	%
Boosted levels	1	1	1	1	Up to 5	

sure that the boosted voltage level never goes beyond maximum allowed levels. The proposed circuitry was implemented in a submicron BCD process technology. Simulation results show that the new proposed method improves upon the single level boost converter.

References

[1] Serneels B, Geukens E, Muer BD, Piessens T. A 1.5W 10V-ouput Class-D amplifier using a boosted supply from a single 3.3V input in standard 1.8V/3.3V 0.18μm CMOS. In: IEEE 2012 International Solid-State Circuits Conference; 17–21 February 2012; San Francisco, CA, USA. New York, NY, USA: IEEE, 2012, pp. 94–96.

[2] Maniktala S. Switching Power Supplies A to Z. Burlington, MA, USA: Elsevier, 2006.

[3] Ridley RB. Power Supply Design, Volume 1: Control. Monpazier, France: Ridley Engineering, 2011.

[4] Erickson RW, Maksimovic D. Fundamentals of Power Electronics. 2nd ed. Norwell, MA, USA: Kluwer Academic Publishers, 2004.