Multilevel hybrid cascade-stack inverter with substantial reduction in switches number and power losses

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Abstract: This paper proposes a multilevel hybrid cascade-stack (HCS) converter. Recently, different new topologies for cascade-type converters have been suggested with the goal of reducing switch number, loss, switch PIV, etc. Meanwhile, output voltage steps increase, and the number of switches is predominately reduced in the suggested inverter in comparison to conventional cascade converters. Additionally, a reduction in the number of on-state switches in the introduced topology causes power loss and voltage drop to decrease. Firstly, the fundamental parts of inverter configuration are described. Afterwards, symmetric and asymmetric converter types are discussed. Simulation and experimental results for 11- and 23-level symmetric types and a 31-level asymmetric form of converter are described.

Key words: Reduced number of circuit devices, inverter power losses, cascade-stack multilevel inverter, symmetric and asymmetric topology

1. Introduction

The development of power grids has created a need for converters such as multilevel inverters. The main purpose of multilevel inverters is to produce output voltage similar to sinusoidal waveform by synthesizing DC input voltages. Fully multilevel inverters are categorized into three main configurations: neutral point clamped (NPC) or diode clamped [1,2], capacitor clamped or flying capacitors (FC) [3], and cascade-type converters [4]. In diode clamp converters, the voltage steps in the output waveform are produced by selecting appropriate paths that include a number of capacitors. It is impossible to attain voltage balance in multilevel diode clamped inverters with a large number of levels for certain operating conditions [5] that involve large modulation indexes and active load currents. Flying-capacitor converters (FCC), which can be used in medium voltages, have many advantages such as self-balancing of capacitors, equal voltage stress on semiconductor power switches, and no need for a transformer. The FCC has some positive features over the diode-clamped structure, such as elimination of clamping diodes and balancing the flying capacitor's voltage using a redundant switching state (RSS) [6].

Between different types of inverter structures, the cascaded multilevel inverter is used in high voltage and power applications. Because of the modular structure of cascaded inverters, they have higher reliability. This inverter can achieve medium output voltage levels by utilizing the low-voltage components [7]. The cascade multilevel inverter, called the cascade H-Bridge (CHB), is composed of a series connection of several H-bridges. Due to the previously mentioned advantages for cascade inverters, many new cascade multilevel

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converter topologies have recently been presented by researchers. The multilevel CHB inverter is one of the cascade topologies whose number of switches is half of that of the CHB. The main advantages of the CHB over other topologies are a simple control system and the modular structure, which make it preferable for high-voltage applications. However, the main disadvantage of these topologies is the need for a large number of isolated DC voltage sources for producing more levels in output voltage. Recently introduced structures for multilevel cascade inverters try to reduce the number of DC voltage sources. Certain defects are associated with multilevel converters. For example, these require a higher number of power semiconductor switches, which makes them expensive and difficult to control, reducing the overall efficiency and reliability [8]. In [9], a cascade converter using a single DC voltage source and capacitors is proposed, which can eliminate the need for several DC sources for higher level converters; however, it has a problem in capacitor voltage balancing [10]. A new multilevel inverter is introduced in [11] that improves the number of switches compared to a CHB converter, but its peak inverse voltage (PIV) is high. In [12], a novel configuration composed of modules is suggested. Each module includes two DC sources and four IGBTs. Asymmetrical multilevel inverters have been recently introduced in [13–15]. Therefore, by utilizing different switching states, more voltage steps on the output voltage waveform can be generated by adding and subtracting DC link voltages in comparison to conventional multilevel inverters with the same number of components [13]. Using these topologies not only improves the quality of output voltage, but also decreases the size of the filter. An innovative symmetric and asymmetric multilevel cascade converter with modular characteristics is addressed in this paper. The number of switches and on-state IGBTs is reduced in this cascade-stack inverter. The recommended configuration is discussed in both symmetric and asymmetric forms. Thereafter, comparisons are made between the suggested multilevel inverter and a traditional one in order to show the advantages of this structure. The power loss of the proposed topology is calculated. Finally, the suggested topology is studied as a simulation and experimental prototype.

2. Cascade multilevel converter

As can be deduced from the term "cascade," all kinds of cascade multilevel inverter configurations are constituted by a series of full-bridge, half-bridge, or other units in which DC sources are used. A typical multilevel cascade inverter is formed from the H-bridge units, which are connected consecutively and named CHB. Each unit or inverter consists of a DC source that produces positive, negative, and zero voltage in its output terminal. The resultant output voltage steps of the CHB are obtained by synthesizing H-bridge terminal voltages using different switching states. Each H-bridge uses four semiconductor power switches, where a pair of them operates in a complementary fashion. Figure 1 shows a traditional multilevel cascade H-Bridge inverter with n DC power supplies.

3. Proposed topology

The basic unit of suggested topology is shown in Figure 2. Figure 3 illustrates the generalized form of the proposed novel multilevel cascade inverter structure. As seen in this figure, it is composed of several units where each one includes two DC sources with equal amplitude and four power switches. It is obvious that in order to avoid the undesired conduction of a middle switch, in each unit a bidirectional switch named $\bar{S}_{1n}$ and $\bar{S}_{2n}$ for nth unit is used. All cells are connected by two IGBT switches ($\bar{H}_i$ and H_i) operating in complementary mode. The last unit involves two IGBTs with one DC voltage source ($V(n)$), and a magnitude in symmetric mode considered as $(4n-1)V_1$. In each unit, just one of three switches must be turned on at any moment; otherwise a short circuit can occur across one of two DC sources. This proposed topology is adopted both for symmetric and asymmetric types.
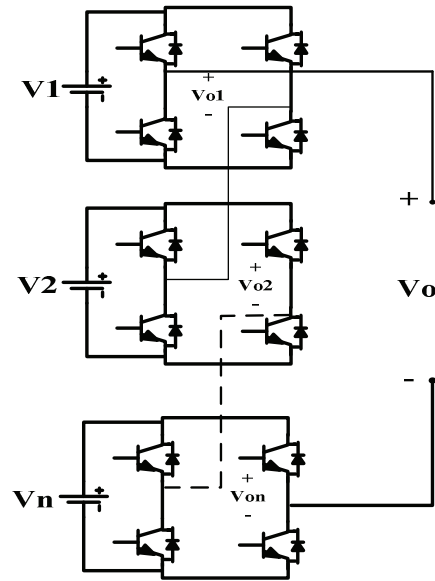
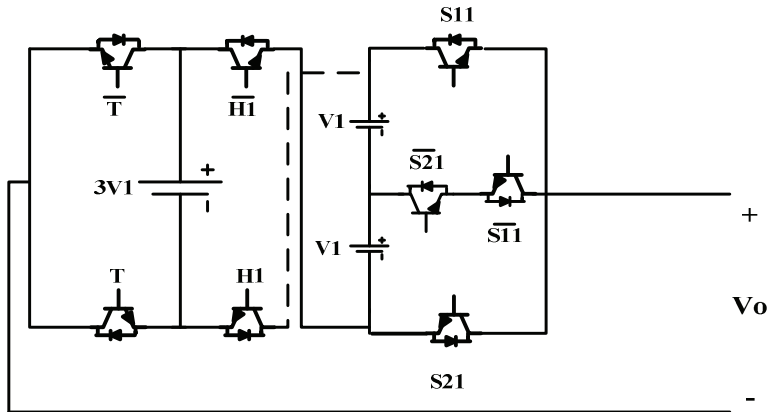**Figure 1.** A conventional multilevel cascade H-bridge inverter.

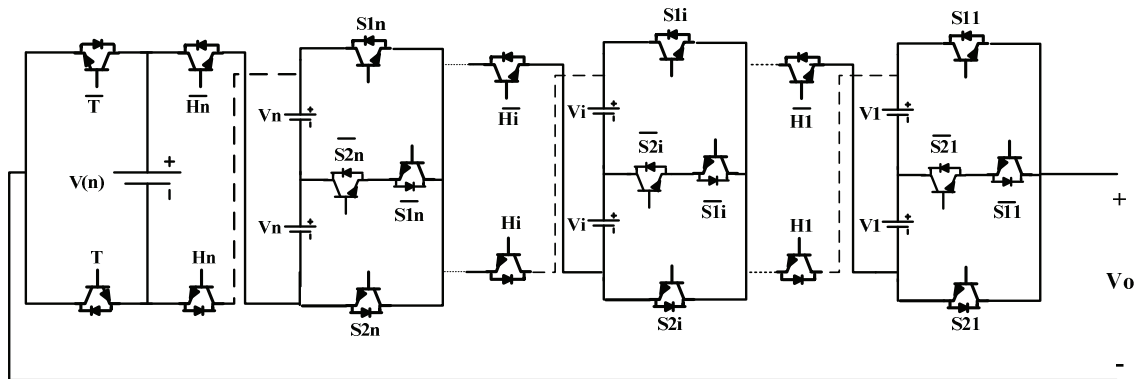**Figure 2.** Proposed topology with one basic unit.

Figure 3. Proposed topology with n basic units.

If we consider the basic unit of this multilevel inverter, it can generate maximum output voltage equal to $2 V_n$ at nth unit.

Thus in symmetric form by assuming the following:

$$V_i = V_1; i = 1, 2, .., n \tag{1}$$

It is noteworthy that n is the number of basic units and should be even.

Each basic unit can produce a maximum voltage equal to $\pm 2\,V_1$ in its output terminal. Knowing each basic unit includes two DC voltage sources and the last unit with $V(n)$, which is defined as follows:

$$V(n) = (4n - 1)V_1 \tag{2}$$

This amount is chosen to generate all levels in the output voltage in the symmetric configuration.

The maximum output voltage (Vo, max) can be described by the following:

$$V_{o,\max} = 2nV_1 + V(n) = (6n - 1)V_1 \tag{3}$$

The number of output voltage levels of the multilevel hybrid cascade stack inverter are equal to $(12n - 1)$.

The basic unit presented in Figure 2 in the symmetric configuration produces an 11-level output voltage waveform. Its switching states are illustrated in Table 1. Based on this table, the operational principle of the HC-S multilevel inverter will be much more comprehensible. The switch S is "on" when its state is 1 and "off" when its state is 0. It should be noted that in each basic unit, two IGBTs cannot be "on" simultaneously. The middle bidirectional switch operates in a complementary manner with two IGBTs on the top and bottom of the basic unit. Therefore, it is "on" when the top and bottom IGBTs are "off".

Table 1. Switching states of the 11-level symmetric proposed topology.

State no.	Switching state				V_o	I_o
	S_{11}	S_{21}	H_1	T		
1	1	0	0	1	$+5V_1$	$+$
2	0	0	0	1	$+4V_1$	$+$
3	0	1	0	1	$+3V_1$	$+$
4	1	0	0	0	$+2V_1$	$+$
5	0	0	0	0	$+V_1$	$+$
6	0	1	0	0	0	
7	0	0	1	1	$-V_1$	$-$
8	0	1	1	1	$-2V_1$	$-$
9	1	0	1	1	$-3V_1$	$-$
10	0	0	1	0	$-4V_1$	$-$
11	0	1	1	0	$-5V_1$	$-$

A 23-level symmetric topology with two modules is shown in Figure 4. The switching states of this configuration are shown in Table 2. There are many redundant switching states for some levels in the suggested topology. For example, there are two ways to generate the $+3V_1$ level shown in Table 3.

In the asymmetric form, assuming the smallest DC voltage source is V_1, we have:

$$V_i = p^{(i-1)}V_1 \, where, i = 1, 2, .., n \, and \, p = 2, 3, 4, 5 \ldots .. p \leq 2n + 1 \tag{4}$$
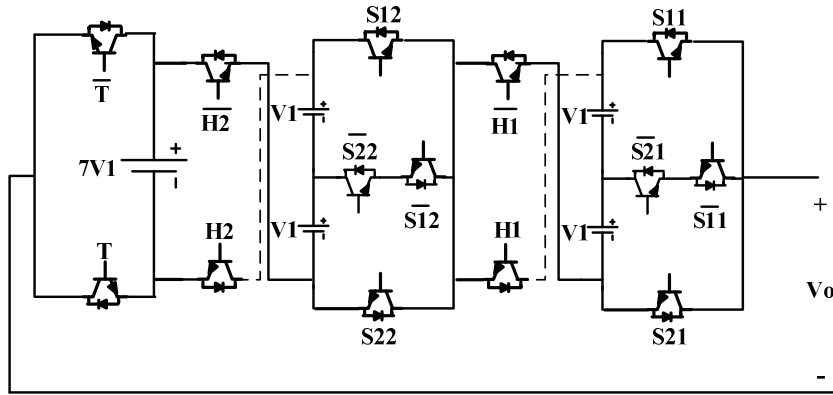
Figure 4. 23-level proposed inverter in symmetric mode.

Table 2. Switching states of the 23-level symmetric proposed topology.

State no.	Switching state							V_o	I_o
	S_{11}	S_{21}	S_{12}	S_{22}	H_1	H_2	T		
1	1	0	1	0	0	0	1	$+11V_1$	$+$
2	1	0	0	0	0	0	1	$+10V_1$	$+$
3	1	0	0	1	0	0	1	$+9V_1$	$+$
4	0	0	0	1	0	0	1	$+8V_1$	$+$
5	0	1	0	1	0	0	1	$+7V_1$	$+$
6	0	0	0	1	1	0	1	$+6V_1$	$+$
7	0	1	0	1	1	0	1	$+5V_1$	$+$
8	1	0	1	0	0	0	0	$+4V_1$	$+$
9	0	0	1	0	0	0	0	$+3V_1$	$+$
10	0	1	1	0	0	0	0	$+2V_1$	$+$
11	0	0	0	1	0	0	0	$+V_1$	$+$
12	0	1	0	1	0	0	0	0	
13	0	0	0	1	1	0	0	$-V_1$	$-$
14	0	1	0	1	1	0	0	$-2V_1$	$-$
15	0	0	0	1	1	1	1	$-3V_1$	$-$
16	0	1	0	1	1	1	1	$-4V_1$	$-$
17	1	0	1	0	0	1	0	$-5V_1$	$-$
18	0	0	1	0	0	1	0	$-6V_1$	$-$
19	0	1	1	0	0	1	0	$-7V_1$	$-$
20	0	0	1	0	1	1	0	$-8V_1$	$-$
21	0	1	1	0	1	1	0	$-9V_1$	$-$
22	0	1	0	0	1	1	0	$-10V_1$	$-$
23	0	1	0	1	1	1	0	$-11V_1$	$-$

Table 3. Redundant switching states for the $+3V_1$ level.

S_{11}	S_{21}	S_{12}	S_{22}	H_1	H_2	T
1	0	0	0	0	0	0
0	0	1	0	0	0	0

To produce all the steps of the output voltage waveform in asymmetric mode, V(n) should be defined as follows:

$$V(n) = \left(4 \sum_{i=1}^{n} P^{(i-1)} + 1 \right) V_1 - 2V_n n \geq 2 \tag{5}$$

$$V_{o,max} = \left(6 \sum_{i=1}^{n} P^{(i-1)} + 1\right) V_1 - 2V_n \tag{6}$$

For instance, here in the binary and ternary modes, the number of output voltage levels of the multilevel hybrid cascade stack inverter is determined as follows:

In the binary method:

$$N_{outputlevels} = \left(12 \times 2^n - 4 \times 2^{(n-1)} - 9\right) \tag{7}$$

In the ternary method:

$$N_{\text{outputlevels}} = 6 \times (3^n) - 4 \times 3^{(n-1)} - 3 \tag{8}$$

The proposed 31-level asymmetric topology with two modules is depicted in Figure 5. The switching states of this configuration are shown in Table 4.

Table 4. Switching states of the 31-level asymmetric proposed topology.

State no.	Switching state							V_o	I_o
	S_{11}	S_{21}	S_{12}	S_{22}	H_1	H_2	T		
1	1	0	1	0	0	0	1	$+15V_1$	$+$
2	0	0	1	0	0	0	1	$+14V_1$	$+$
3	0	1	1	0	0	0	1	$+13V_1$	$+$
4	0	0	0	0	0	0	1	$+12V_1$	$+$
5	0	1	0	0	0	0	1	$+11V_1$	$+$
13	0	0	0	0	0	0	0	$+3V_1$	$+$
14	1	0	1	0	0	1	1	$+2V_1$	$+$
15	0	0	1	0	0	1	1	$+V_1$	$+$
16	0	1	0	1	0	0	0	0	
17	0	0	0	1	0	0	0	$-V_1$	$-$
18	0	1	0	1	1	0	0	$-2V_1$	$-$
19	0	0	0	0	1	1	1	$-3V_1$	$-$
27	1	0	0	0	1	1	0	$-11V_1$	$-$
28	0	0	0	0	1	1	0	$-12V_1$	$-$
29	1	0	0	1	1	1	0	$-13V_1$	$-$
30	0	0	0	1	1	1	0	$-14V_1$	$-$
31	0	1	0	1	1	1	0	$-15V_1$	$-$

4. Comparison study

Here, n units for the proposed cascade inverter are assumed and the number of DC voltage sources was obtained according to this for both its symmetric and asymmetric states, and then it is compared to a conventional multilevel cascade inverter with similar DC voltage sources. The major advantage of the suggested topology in this paper is that there is a considerable reduction in the switch number and on-state switches. As we know, on-state switches represent voltage drop. Tables 5 and 6 show the characteristics of the proposed hybrid multilevel cascade inverter and conventional multilevel cascade inverter, respectively. It should be noted that all given parameters in these tables are in a per unit system, and V_1 is considered as the base amount. The first and second methods in this table refer to symmetric and asymmetric modes of the new configuration inverter.

Here, n is assumed to be the number of units. From this table, it is obvious that the number of IGBTs and the number of on-state switches or voltage drop in the proposed structure is considerably less than that of an ordinary cascade multilevel inverter.
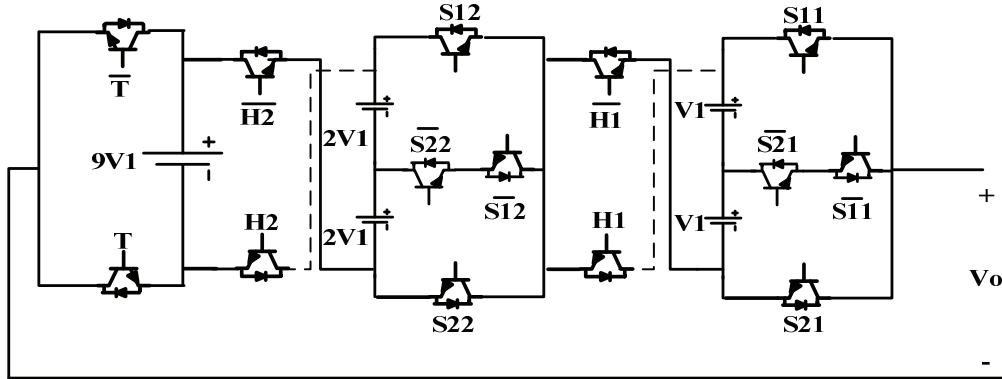

Figure 5. 31-level proposed inverter in symmetric mode.

Table 5. Comparison of the proposed hybrid cascade-stack multilevel inverter in symmetric and asymmetric modes.

Proposed	First method	Second method
	symmetric	asymmetric
No. of DC sources	2n + 1	2n + 1
No. of switches	6n + 2	6n + 2
No. of output levels	12n − 1	$12 * \left(\frac{1-p^{n-1}}{1-p} \right) - 4V_n + 3$
Maximum voltage	$(6n - 1)$	$6 * \left(\frac{1-p^{n-1}}{1-p} \right) - 2V_n + 1$
PIV	$(26n - 4)$	$10 \sum_{i=1}^{n} V_i + 4V(n)$
No. of on-state switches	3n + 1	3n + 1

Table 6. Comparison of conventional multilevel cascade inverters in symmetric and asymmetric modes.

Traditional cascade	First method	Second method
	symmetric	asymmetric
No. of DC sources	2n + 1	2n + 1
No. of switches	8n + 4	8n + 4
No. of output levels	12n + 3	$12 * \left(\frac{1-p^{n-1}}{1-p} \right) - 4V_n + 3$
Maximum voltage	$(6n + 1)$	$6 * \left(\frac{1-p^{n-1}}{1-p} \right) - 2V_n + 1$
PIV	$(20n + 4)$	$8 \sum_{i=1}^{n} V_i + 4V(n)$
No. of on-state switches	4n + 2	4n + 2

The DC voltage sources in both symmetric and asymmetric modes of the hybrid cascade stack inverter and the conventional cascade are equal numerically, and equal to $2n + 1$, where n is the number of units. It is noteworthy that here, the number of IGBTs has been compared instead of the number of switches. As is known, bidirectional switches consist of two common emitter IGBTs. In some studies, comparisons are done according to the number of bidirectional switches instead of the number of IGBTs, which caused greater reduction in the number of switches. Therefore, this is not an accurate comparison. In this section, the proposed topology is

compared to two other topologies recommended in [11] and [12]. From Table 5, for a symmetric number of switches and PIV in the proposed configuration, the number can be obtained as follows:

$$N_{switches} = \frac{m}{2} + \frac{5}{2} \tag{9}$$

$$PIV = \frac{13}{6}m + \frac{37}{6} \tag{10}$$

where m is number of output voltage levels.

The number of switches and PIV in [11] is $m + 1$ and $\frac{15}{2}m - \frac{37}{2}$ respectively, where m is the number of levels. The comparison between the proposed topology and [11] prove that not only is the number of switches lower in the suggested configuration, but also that PIV is lower compared to the topology presented in [11]. In [12], a novel configuration constituted from cascade modules is suggested. Each module includes two DC sources and six IGBTs. The number of IGBTs and PIV in [12] is $\frac{3}{2}m + \frac{1}{2}$ and $\frac{15}{2}(m-1)$, respectively. Both the number of IGBTs and PIV is higher in respect to the suggested topology. It should be mentioned that these parameters are compared according to the same number of output voltage levels in [11,12] and the proposed configuration.

The number of DC sources of a multilevel cascade inverter in symmetric and asymmetric mode is exactly the same as that of the suggested inverter. This comparison proves the benefits of the recommended structure in this paper. As illustrated in Table 5, with a lower number of IGBTs, the same output voltage levels could be stepped out in the suggested topology in comparison to a conventional H-bridge (CHB) converter.

Figure 6a shows the number of IGBTs versus the number of output voltage levels for the proposed topology [11,12] and CHB. As the figure shows, for any specific level value, the proposed topology uses a lower number of IGBTs in comparison to [11,12] and CHB. The figure clearly shows that the proposed topology uses a lower number of IGBTs. Figure 6b depicts PIV versus the number of voltage levels for the above-mentioned topologies.
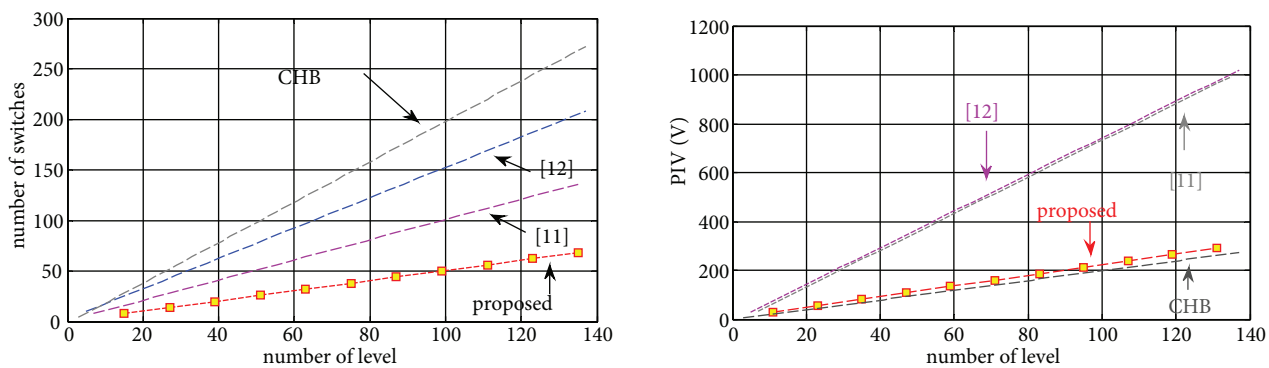

Figure 6. The number of IGBTs and PIV versus the number of voltage levels. (a) The number of IGBTs versus the number of voltage levels. (b) PIV versus the number of voltage levels.

5. Calculation of losses

Generally, power electronic converters have two kinds of losses. On-state resistance and forward voltage of switches produce conduction losses. The switching losses are due to a nonideal operation of switches. Because

of the low number of switches and on-state switches in each level, the power losses of the presented inverter will be lower than those of the conventional cascade inverter. The calculation of power losses of the proposed multilevel inverter is given below.

5.1. Conduction power losses

First, conduction losses for a typical power semiconductor switch and antiparallel diode are calculated, and then extended to the proposed converter. The instantaneous conduction losses for an IGBT ($p_{c,s}(t)$) and antiparallel diode ($p_{c,D}(t)$) can be written as [16]:

$$P_{C,s}(t) = [V_s + R_s\, i^\beta(t)]\ i(t) \tag{11}$$

$$P_{C,D}(t) = [V_D + R_D\ i\ (t)]\ i(t) \tag{12}$$

where V_s and V_D are the on-state voltage of the IGBT and its antiparallel diode, respectively. R_s and R_D are the on-state resistance of the IGBT and its diode, respectively, and β is a constant that depends on the IGBT parameters. Assume that n(t) IGBTs and m(t) antiparallel diodes are "on" at each time in the current path in the proposed multilevel inverter. The values of n(t) and m(t) are determined by the direction of the current and output voltage level. According to the desired voltage level and current direction in the proposed inverter seen in Figure 2, several states may occur in the current path. These states are: two diodes, two transistors, two transistors and one diode, one transistor and one diode, two diodes and one transistor, and two transistors and two diodes in the current route. Therefore, the average conduction power loss of the suggested inverter using Eqs. (11) and (12), can be written as follows:

$$P_C(t) = \frac{1}{\pi} \int_0^\pi \left[\left(\begin{array}{c} n(t)V_s + m(t)V_D + \\ n(t)R_s\, i^\beta(t) + m(t)R_D i(t) \end{array} \right) i(t) \right] d\omega t \tag{13}$$

5.2. Switching power losses

Similar to the calculation for conduction losses, switching losses for one switch are obtained first, and then this amount is applied to the proposed multilevel inverter. The switching power losses have two terms:

1. IGBT switching power loss

2. Antiparallel diodes power losses

The following equations for the above-mentioned terms of switching losses can be written as follows:

$$P_{sw,s} = (E_{on,s} + E_{off,s})\, f_{sw} \tag{14}$$

$$P_{sw,Anti\_D} = (E_{on.Anti\_D} + E_{off.Anti\_D})\, f_{sw} \approx E_{on.Anti\_D}\, f_{sw} \tag{15}$$

where $P_{sw,s}$ is the switching power losses of the IGBT, $E_{on,s}$ is turn-on energy losses in the IGBT, $E_{off,s}$ is the turn-off energy losses in the IGBT, and f_{sw} is the switching frequency.

The switching losses depend on the number of switching transitions, and so they are influenced by the modulation method. Finally, the total switching power losses of a fundamental block can be calculated as follows:

$$P_{sw} = \sum_{i=1}^p P_{sw,s_i} + P_{sw,Anti\_D_i}, \tag{16}$$

where p is determined by the switching pattern and indicates the number of turned-on IGBTs.

Using Eqs. (13) and (16), the total losses of the fundamental multilevel inverter can be obtained as in Eq. (17).

$$P_{loss} = P_{sw} + P_C \tag{17}$$

6. Simulation and experimental results

To evaluate the performance of the suggested multilevel converter shown in Figures 2, 4, and 5, a single-phase 11-, 23-, and 31-level prototype has been modeled and implemented. Simulations were done with MATLAB/Simulink software. The magnitude of DC voltage sources in the implemented prototype symmetric inverter is 30 V. Each switch consists of an IGBT and an antiparallel diode. The IGBTs used in the implemented prototype are BUP406 with internal antiparallel diodes with voltage and current ratings equal to 1000 V and 20 A, respectively. The required switching pulses are produced by the DSPIC30F4011 microcontroller and the Hcpl316j is used as a gate driver. Figure 4 shows a 23-level hybrid cascade-stack (HC-S) inverter in a symmetric form that has two basic units, and so n = 2 and the number of IGBTs according to Table 1 will be 6 n + 2, where the yield is 14 IGBTs. Figure 7 shows a photo of the laboratory prototype.
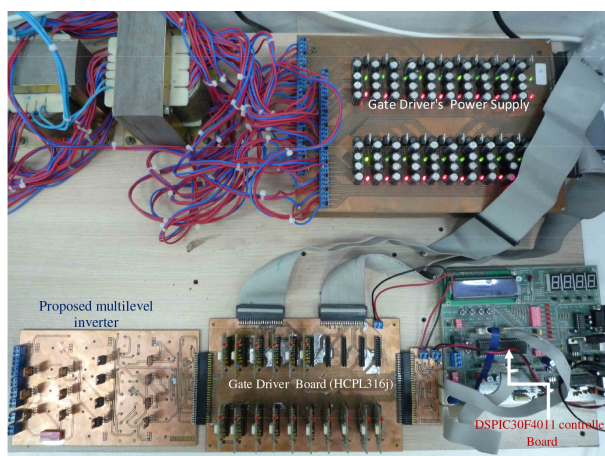

Figure 7. Photograph of the implemented laboratory prototype.

Figure 8 illustrates the simulation and experimental results for an 11-level symmetric topology. The magnitudes of the DC voltage sources in the implemented prototype 11-level symmetric inverter are 30 V, 30 V, and 90 V. As seen in these figures, the results clearly match. The partial difference between the magnitudes of the simulation and the experimental results is because of the voltage drops on switches in the implemented prototype. As shown in Figure 8a, there is a phase difference between the output voltage and the current waveform, which is due to the inductive characteristic of the load. Figure 8a shows the simulation result of the 11-level suggested basic unit. Figures 8b and c depict the experimental results for this case. Figure 9a shows the simulation result for the 23-level symmetric topology that is shown in Figure 4. The magnitudes of the DC voltage sources in the implemented prototype 23-level symmetric inverter are 30 V, 30 V, 30 V, 30 V and 210 V. Figures 9b and 9c illustrate experimental results for a 23-level symmetric configuration under no load and loading conditions. Figure 10a depicts the simulation result for the 31-level asymmetric topology shown in Figure 5. The amplitudes of DC voltage sources in the implemented prototype 31-level asymmetric inverter are 30 V, 30 V, 60 V, 60 V, and 270 V. Figures 10b and 10c show the experimental results of the output voltage
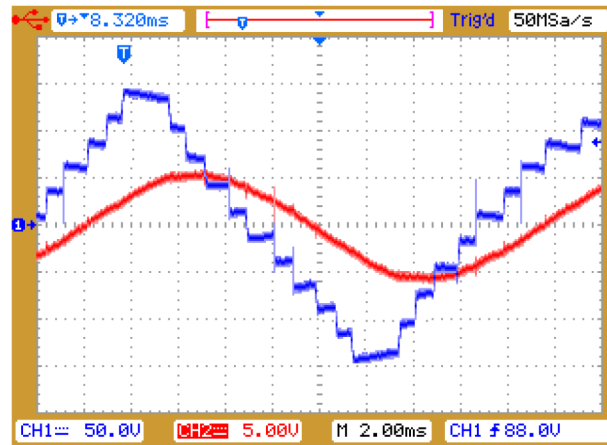
and current for a 31-level asymmetric configuration. Figures 11a and 11b show the FFT analysis of the output voltage of the suggested inverter at 11 and 23 levels, respectively. This figure shows the THD analysis and magnitudes of different harmonics of the output voltage waveforms in the simulation.
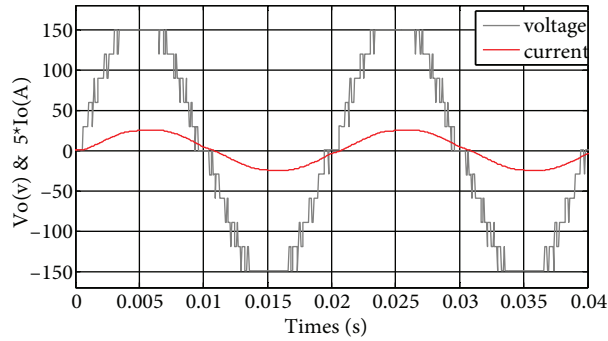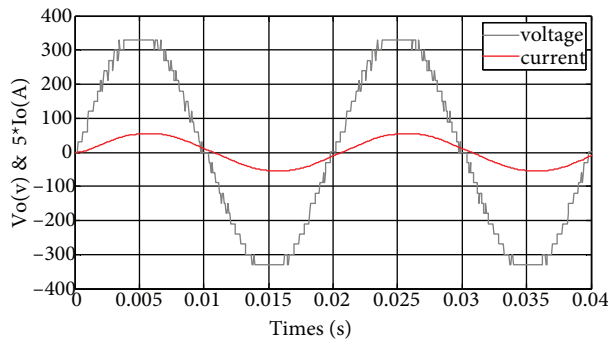

(a)
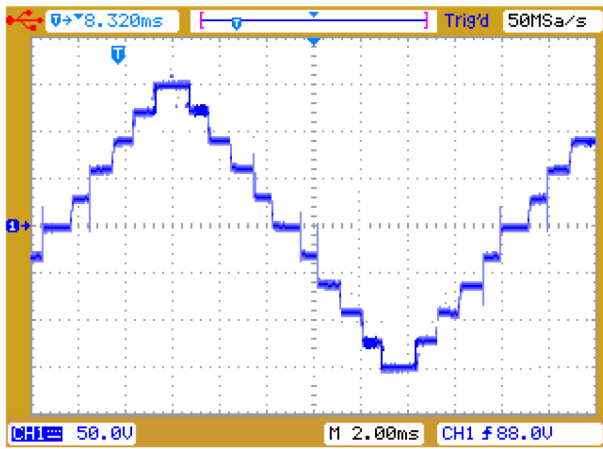
(b)

(c)

Figure 8. Output voltage and current of the 11-level proposed inverter for a basic unit. (a) Simulation results of basic units (output voltage and current). (b) Experimental results of basic units (output voltage in a no-load case). (c) Experimental results of basic units (output voltage and current under load condition).

(a)

Figure 9. Output voltage and current of the 23-level proposed inverter in symmetric mode. (a) Simulation results of a 23-level symmetric topology (output voltage and current).
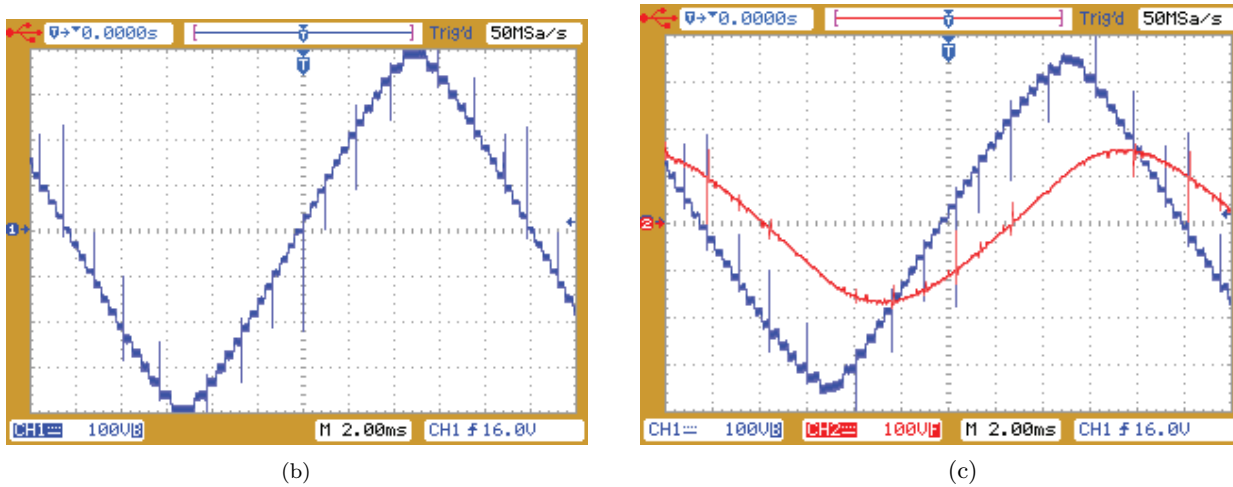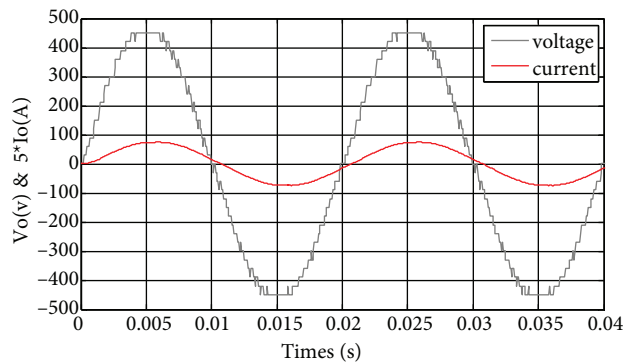
(b)   (c)

Figure 9. Output voltage and current of the 23-level proposed inverter in symmetric mode. (b) Experimental results of a 23-level symmetric topology (output voltage in a no-load case). (c) Experimental results of a 23-level symmetric topology (output voltage and current under load condition).
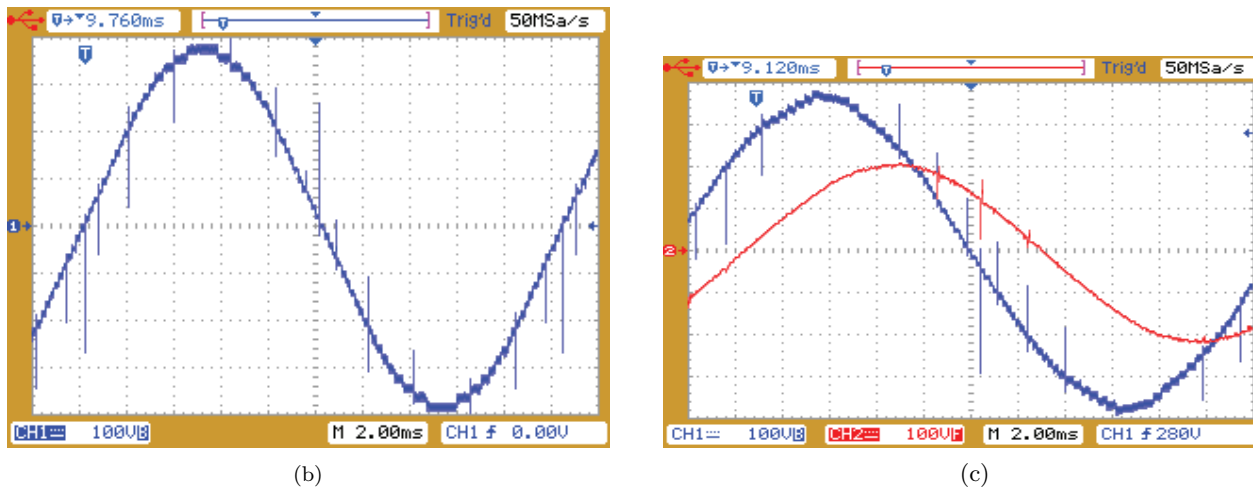

(a)

(b)   (c)

Figure 10. Output voltage and current of the 31-level proposed inverter in asymmetric mode. (a) Simulation results of a 31-level asymmetric topology (output voltage and current). (b) Experimental results of a 31-level asymmetric topology (output voltage in a no-load case). (c) Experimental results of a 31-level asymmetric topology (output voltage and current under load condition).
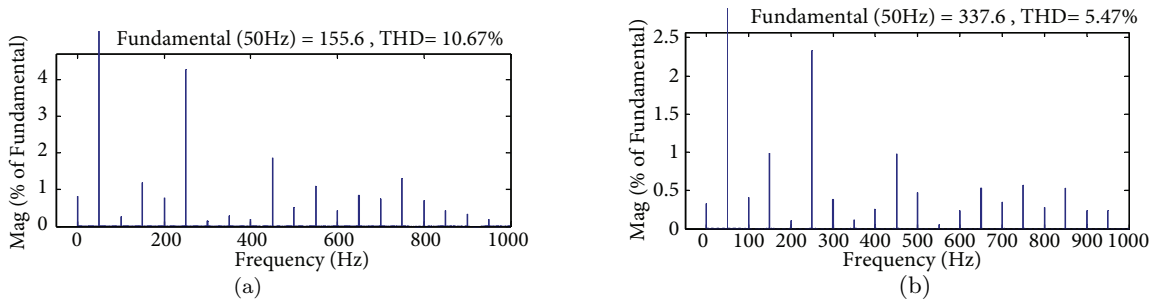
Figure 11. THD analysis and magnitudes of different harmonics in a simulation output waveform. (a) THD analysis and magnitudes of different harmonics in an 11-level output waveform. (b)THD analysis and magnitudes of different harmonics a in a 23-level output waveform.

As seen in Figures 8–10, the output current waveform that resulted from the simulation and experimental tests are like a sinusoidal waveform and have low THD. For the 11-level output voltage case, the THD of the output voltage in the simulation result is 10.67%. In order to generate a desirable output voltage with good power quality, more voltage levels are needed and the other switching pattern should be used in the converter. Decreasing the THD of the output voltage is seen in Figure 11b for the 23-level output voltage case. The FFT analysis in the experimental test for the output voltage waveforms of 11, 23, and 31 levels are shown in Figures 12a–12c.
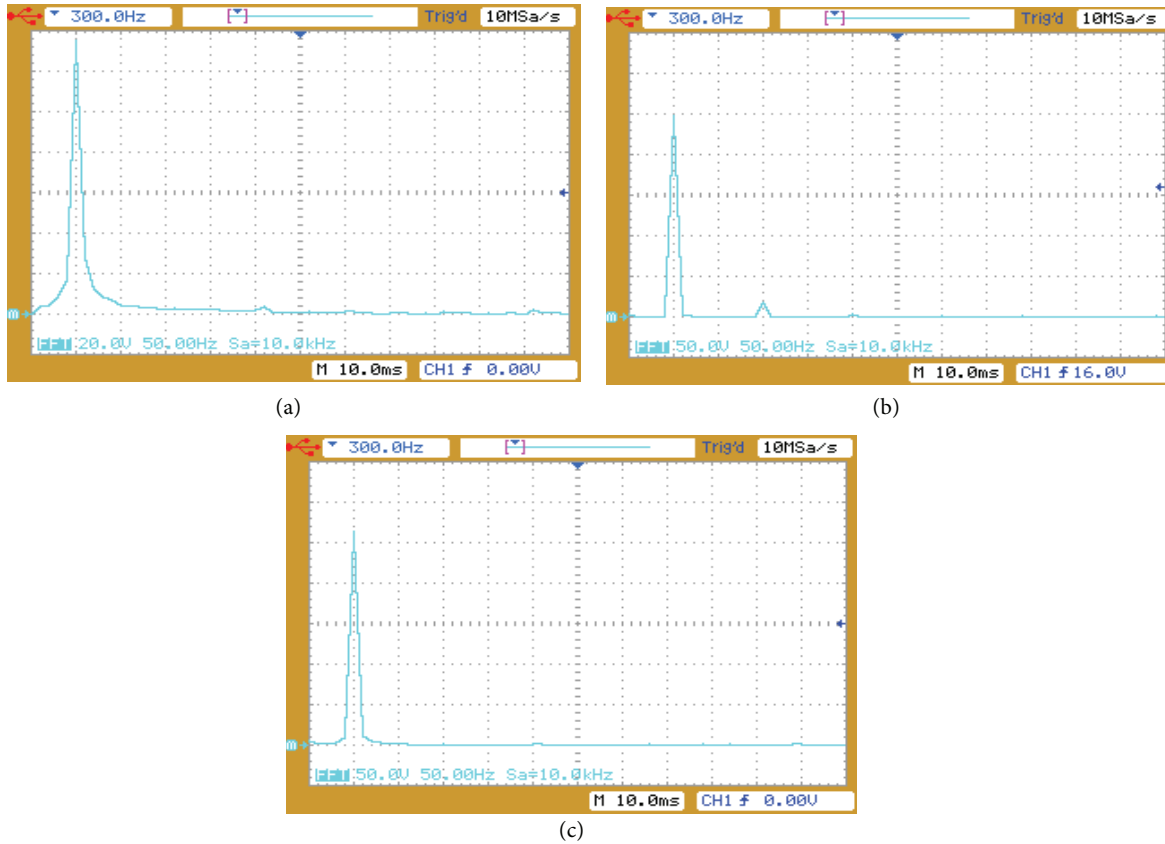

Figure 12. FFT analysis in experimental output waveforms. (a) FFT analysis of the experimental result for the 11-level output voltage waveform. (b) FFT analysis of the experimental result for the 23-level output voltage waveform. (c) FFT analysis of the experimental result for the 31-level output voltage waveform in the in the asymmetric topology.

7. Conclusion

In this paper, a novel configuration has been proposed for a multilevel converter called a HCS converter, which is composed of the series connection of basic units or modules. The proposed converter is compared to other topologies. It has been shown that the proposed topology not only decreases the number of switches and components with respect to a conventional H-bridge multilevel converter, but it also has lower on-state switches in each level. Therefore, the voltage drop in its output will be less. The operation and performance of the proposed topology have been simulated and verified by implementing a single-phase 11- and 23-level symmetric and 31-level asymmetric converter prototype. It has been shown that all levels are produced exactly and the THD of output voltage waveform is low.

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