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Capacitive sensor supporting multiple touch switches using a resistor string

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Abstract: In a low-cost integrated circuit (IC) chip, the packaging cost is a considerable portion of the total manufacturing cost of the chip. As the packaging cost is directly related to the total number of I/O pins, it is highly desirable to minimize the number of I/O pins while maintaining the same functionality. We propose a capacitive sensor that supports multiple touch switches with only two IC pins. The electrode plates of the touch switches are placed at the ends of a resistor string and between every two adjacent resistors in the resistor string. The proposed method measures rise times at each side of the resistor string while driving the opposite side. The capacitive sensor can recognize an electrode plate contacted by a finger using the two rise times and the proposed rise time model. Experimental results with four touch plates show that the proposed capacitive sensor gives 181 fF resolution and can handle four touch switches.

Key words: Capacitive sensor, capacitive touch switch, pin efficiency, resistor string

1. Introduction

Capacitive touch switches are widely used in many electronic devices such as MP3 players, TVs, computers, lamps, and wall switches because they give a soft touch feeling and allow the design of slim products [1].

A capacitive touch switch is an application of a capacitive sensor that converts capacitance to voltage [2–5], frequency [6,7], or time [1,8–11] and then measures the converted values. A capacitive touch switch measures the capacitance induced between a finger and an electrode plate, and then determines if the finger touched the plate [10]. A simple but effective way to measure capacitance is to measure the rise time of the voltage across the capacitance while it is being charged [1,10,11].

In a low-cost integrated circuit (IC) chip, the packaging cost consumes a considerable portion of the total manufacturing cost of the chip. The packaging cost is directly related to the total number of IC pins. Thus, to reduce the total number of IC pins while maintaining the same functionality, i.e. to increase the efficiency of the IC pins, it is quite important to reduce the manufacturing cost of the IC chip. The efficiency of a pin is defined as the inverse of the average number of pins needed to implement a functional block. The pin efficiency of commercial or previous capacitive touch switches [1,10] is less than or equal to one.

Touch screen technology measures the capacitance induced by a finger and a touch panel and then determines the position on the panel that was touched by the finger. The electrodes on a touch screen are usually arranged as a layer of rows and a layer of columns [12]. When a finger comes close to the intersection of two electrodes, a mutual capacitance is induced between the electrodes, wherein the induced mutual capacitance is about several femtofarads [13]. A touch screen read-out circuit measures the induced capacitance and determines

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the touch positions. A touch screen read-out circuit should have the ability to measure a very small capacitance in a high-level noise environment, wherein the noise comes from the display panel while driving the display panel [14]. Thus, touch screen technology requires high precision capacitance measurement circuits working in a high-level noise environment [13,15].

In a touch switch, the induced capacitance between a finger and a plate is on the order of a few picofarads and the noise level is not as high as for much of the touch screen because a touch switch does not have a display panel. Thus, touch screen technology is an expensive and inappropriate solution for touch switch applications, although the technology is highly advanced and could potentially be applicable.

An RC bridge-type capacitive touch switch was proposed in [10] and consists of two touch electrode plates and one resistor between the plates, as shown in Figure 1. In the figure, C_S is the capacitance induced by a finger and a plate. There are also parasitic capacitances C_{P0} and C_{P1} at nodes 0 and 1, respectively. This method measures the rise times at each node while driving the opposite node, and then utilizes the ratio of the two rise times.

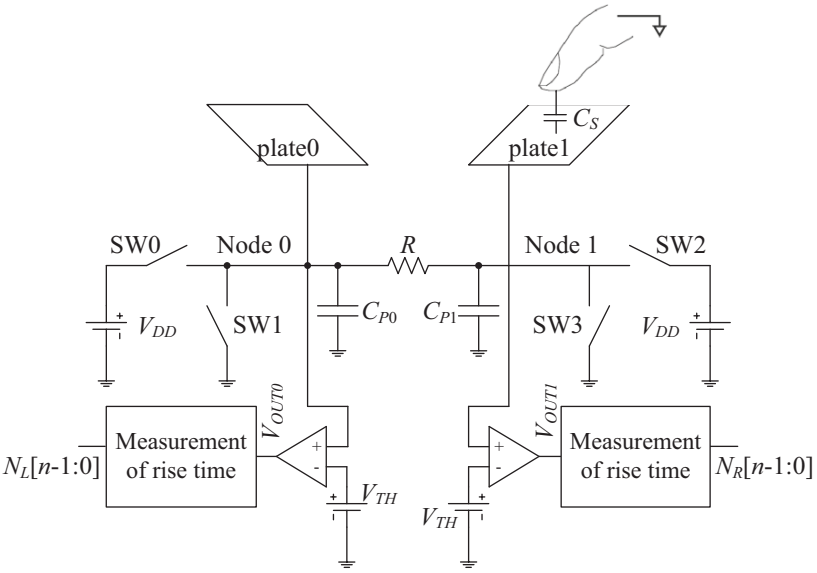

Figure 1. RC bridge-type capacitive touch switch in [10].

The method in Figure 1 initializes capacitance C_S and parasitic capacitances C_{P0} and C_{P1} using switches $SW1$ and $SW3$, and then measures rise time t_R at node 1 while driving node 0 with V_{DD} using switch $SW0$. This method also measures rise time t_L at node 0 using a similar procedure. The ratio of the two rise times is expressed as in Eq. (1), where $k_1 = \ln\left(V_{DD}/\left(V_{DD}-V_{TH}\right)\right)$:

$$\frac{t_L}{t_R}=\frac{k_1RC_{P0}}{k_1R(C_{P1}+C_S)}=\frac{C_{P0}}{C_{P1}+C_S}\approx\frac{N_L}{N_R} \tag{1}$$

The values of N_L and N_R, shown in Figure 1, are the measured values in digital form of the rise times t_L and t_R, respectively. A simple method to measure rise time in digital form is to use a digital counter [10]. A more accurate rise time measurement based on multiphase clock signals is proposed in [1].

We propose a capacitive sensor that improves the efficiency of the pin by implementing multiple touch switches with only two IC pins. The electrode plates of the switches are placed at both ends of a resistor string

and between every two adjacent resistors in the resistor string. The structure of the proposed method is the same as that shown in Figure 1, except the resistor is replaced with a resistor string. The proposed method also measures rise times t_L and t_R, as in the previous method [1,10]. The ratio of the two rise times is also used to determine the position of the induced capacitance if there is no parasitic capacitance. However, parasitic capacitances are unavoidable, and they prohibit the ratio of the two rise times from directly being applied to find the position of the induced capacitance.

We propose a simple rise time model based on the Elmore delay model [16], wherein the rise time is approximately expressed by two terms. One term is due to parasitic capacitances and the other is due to the induced capacitance. The effect of the parasitic capacitances can be removed by subtracting the amount of time due to the parasitic capacitances from the measured rise time. Even though this approximate model is simple, it gives relatively high accuracy. Simulation results show that this model gives an error of only 0.15% using the proposed circuit.

The proposed method was implemented with four touch plates and the performance of the method was measured. The experimental results show that the proposed capacitive sensor gives a 181 fF resolution and can handle four touch switches.

The remainder of this paper is organized as follows. Section 2 describes the basic idea of the proposed capacitive sensor. Section 3 describes the proposed method considering parasitic capacitances. Section 4 discusses our experimental results, and Section 5 concludes the paper.

2. Basic idea of the proposed capacitive sensor

The proposed capacitive sensor is shown in Figure 2, where C_S is the capacitance induced by a plate and a finger, and C_{P0}, C_{P1}, C_{P2}, and C_{P3} are the parasitic capacitances at nodes 0, 1, 2, and 3, respectively. This structure can be easily extended to support $(n + 1)$ touch switches using n resistors. In this case, the efficiency of the pin becomes $(n + 1) / 2$ because two IC pins are required to implement $(n + 1)$ touch switches.

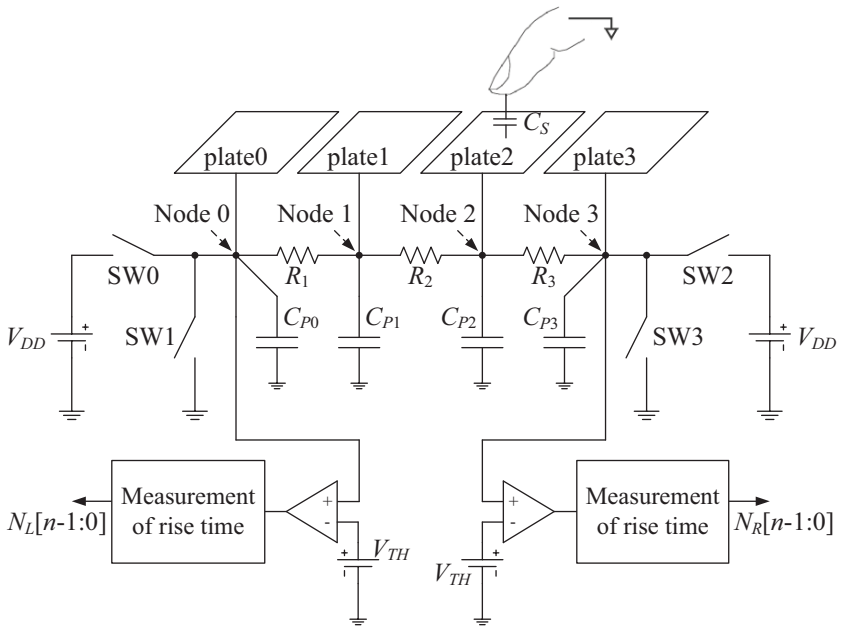

Figure 2. Proposed capacitive sensor with four electrode plates.

The proposed method initializes all capacitors to zero voltage by using switches $SW1$ and $SW3$, and then it measures rise time t_R at node 3 until the voltage of node 3 reaches a threshold voltage V_{TH} while charging capacitors using switch $SW0$. The method also measures rise time t_L at node 0 with a similar procedure. The rise times t_L and t_R are used to find the position of the induced capacitance.

Now we assume that the parasitic capacitances are all zero, and all the resistors have the same resistance R in Figure 2. The rise times become $t_L = k_1 RC_S$ and $t_R = 2k_1 RC_S$ if the induced capacitor C_S is at node 2, as shown in Figure 2. If the induced capacitor is at node i, where $i = 0$–3, then $t_L = (3 - i)k_1 RC_S$ and $t_R = ik_1 RC_S$. The sum of the two rise times is always the same as $t_L + t_R = 3k_1 RC_S$ regardless of the position of C_S. The rise times are summarized in Table 1, where each column has the node name where C_S is placed, the rise time t_L, the rise time t_R, and the sum of the two rise times.

Table 1. Rise times t_L and t_R when all parasitic capacitances are zero.

Position of C_S	Node 0	Node 1	Node 2	Node 3
t_L	$3k_1 RC_S$	$2k_1 RC_S$	$k_1 RC_S$	0
t_R	0	$k_1 RC_S$	$2k_1 RC_S$	$3k_1 RC_S$
$t_L + t_R$	$3k_1 RC_S$	$3k_1 RC_S$	$3k_1 RC_S$	$3k_1 RC_S$

The rise times t_L and t_R are plotted in 2-D space, as shown in Figure 3, where four lines represent the cases where C_S is at nodes 0 to 3, respectively. When C_S is decreased, the corresponding points move toward the origin. The slope of each line does not depend on the value of C_S; rather, it depends on the position of C_S.

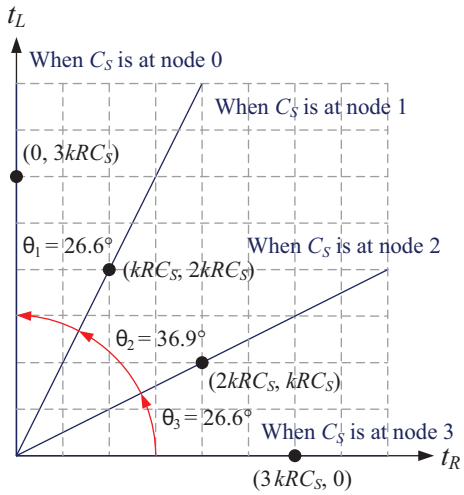

Figure 3. Plot of (t_R , t_L) in 2-D space.

The proposed basic algorithm is shown in Algorithm 1. The threshold angles are defined as $\theta_{TH}(0) = \theta_1 / 2 + \theta_2 + \theta_3$, $\theta_{TH}(1) = \theta_2 / 2 + \theta_3$, and $\theta_{TH}(2) = \theta_3 / 2$, where θ_1, θ_2 and θ_3 are the angles between the adjacent lines shown in Figure 3. The algorithm returns the plate number contacted with a finger, and returns –1 if none are contacted. In step 1, the algorithm measures two rise times, t_L and t_R, and then determines whether the induced capacitance is greater than or equal to the smallest detectable capacitance by comparing the sum of the two rise times and a threshold value λ in step 2. In step 3, the algorithm finds the position of C_S and then returns the number.

Algorithm 1. Proposed basic algorithm

1 Measure rise times t_L and t_R;
2 if $(t_L + t_R < \lambda)$, return –1;
3 for $(i = 0;\ i < 3;\ i = i + 1)$
if $\frac{t_L}{t_R} > \tan(\theta_{TH}(i))$, return i;
return 3;

The algorithm is based on the fact that the slopes of the lines only depend on the position of C_S. This fact is no more valid if all the parasitic capacitances are not zero. Parasitic capacitances are unavoidable in a capacitive sensor; thus, the algorithm cannot be directly applied without removing the effects of parasitic capacitances.

3. Proposed method considering parasitic capacitance

3.1. Proposed rise time model

The Elmore delay model [16] is a simple and fast method used to approximately calculate delays in a very-large-scale integration (VLSI) circuit design area. The concepts of rise time and delay time are the same in an RC circuit except for the threshold voltage. The delay time is defined as the time interval until the output of the RC network reaches 0.5 V_{DD} from zero. Thus, we can approximate the rise time using the Elmore delay model as follows:

$$t_r = k \sum_i R_{is} C_i, \tag{2}$$

where k is a constant determined by simulation, R_{is} is the summed resistance from point i to the power or ground, and C_i is the capacitance at point i.

Now we can express rise times t_L and t_R as in Eqs. (3) and (4), respectively, using the approximate rise time model when C_S is at node 2, as shown in Figure 2:

$$\begin{aligned} t_L &= 3kRC_{P0} + 2kRC_{P1} + kR(C_{P2} + C_S) \\ &= kR(3C_{P0} + 2C_{P1} + C_{P2}) + kRC_S \\ &= t_{L0} + kRC_S, \end{aligned} \tag{3}$$

$$\begin{aligned} t_R &= kRC_{P1} + 2kR(C_{P2} + C_S) + 3kRC_{P3} \\ &= kR(C_{P1} + 2C_{P2} + 3C_{P3}) + 2kRC_S \\ &= t_{R0} + 2kRC_S, \end{aligned} \tag{4}$$

where t_{L0} and t_{R0} are rise times t_L and t_R when C_S is zero, respectively. In Eqs. (3) and (4), the rise times t_L and t_R consist of two parts: one part is due to the induced capacitance, and the other part is due to the parasitic capacitances. The rise times t_L and t_R are calculated with the rise time model and are summarized in Table 2.

Table 2. The rise times t_L and t_R expressed using the proposed rise time model.

Position of C_S	node 0	node 1	node 2	node 3
t_L	$t_{L0} + 3kRC_S$	$t_{L0} + 2kRC_S$	$t_{L0} + kRC_S$	t_{L0}
t_R	t_{R0}	$t_{R0} + kRC_S$	$t_{R0} + 2kRC_S$	$t_{R0} + 3kRC_S$

The adjusted rise times t'_L and t'_R are defined as in Eqs. (5) and (6), respectively:

$$t'_L = t_L - t_{L0}, \tag{5}$$

$$t'_R = t_R - t_{R0}. \tag{6}$$

From Table 2 and Eqs. (5) and (6), we can remove the effects of parasitic capacitances and use the basic algorithm shown in Algorithm 1.

3.2. Analysis of the proposed rise time model

We demonstrate the accuracy of the proposed rise time model using simulation, where $R = 100\ \mathrm{K}\Omega$, $C_{P0} = C_{P1} = C_{P2} = C_{P3} = 100$ pF, $V_{TH} = 0.8\ V_{DD}$, and the range of C_S is 0 to 10 pF. We can express four lines of t_L versus C_S as in Eq. (7) from Table 2, where all lines pass the same y-intercept t_{L0}:

$$\begin{aligned} t_L &= t_{L0} + 3kRC_S \text{ if } C_S \text{ is at node 0;} \\ t_L &= t_{L0} + 2kRC_S \text{ if } C_S \text{ is at node 1;} \\ t_L &= t_{L0} + kRC_S \text{ if } C_S \text{ is at node 2; and} \\ t_L &= t_{L0} \text{ if } C_S \text{ is at node 3.} \end{aligned} \tag{7}$$

Figure 4 shows graphs of t_L versus C_S. The lines on the circles are drawn based on exact solutions obtained using simulation. The lines pass the same y-intercept, whose value is 91.33. The dashed lines on the triangles are drawn based on the proposed rise time model and pass the y-intercept t_{L0}. Since these two y-intercept values are the same, k becomes 1.52. In the range of C_S, the maximum error rate is 0.15% when a C_S of 10 pF is at node 2, where the error is 0.1382 μs and the exact rise time is 92.714 μs.

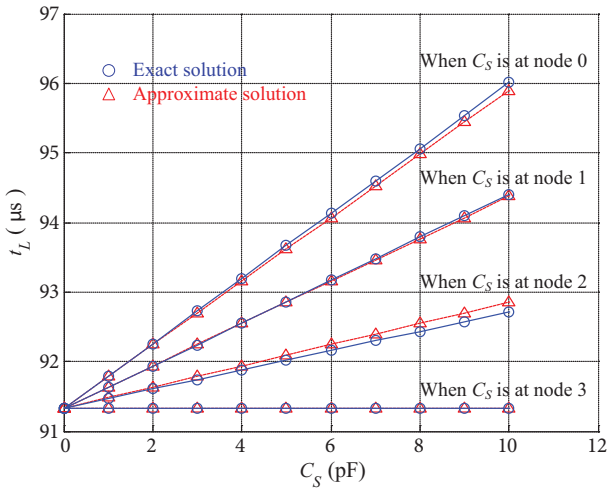

Figure 4. Rise time t_L versus induced capacitance C_S.

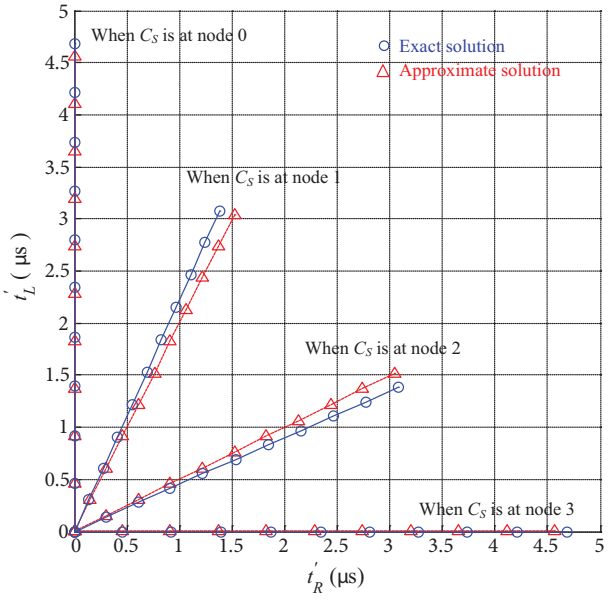

Figure 5. Plot of (t'_R, t'_L) in 2-D space.

Figure 5 shows the adjusted rise time pair t'_L and t'_R, where four groups of lines represent the cases where C_S is at node 0 to node 3. The lines on circles are drawn with exact solutions obtained from simulation, and the

dashed lines on triangles are drawn with approximate solutions obtained using the proposed rise time model. When C_S is at node 0 or 3, the lines and the dashed lines have the same direction but different magnitudes. When C_S is at node 1 or 2, the dashed lines have errors of direction and magnitude. However, the shape of the dashed lines is quite similar to that of the lines in terms of angle and magnitude.

Figure 6 shows the graphs of $t'_L + t'_R$ versus C_S, where the line on the circles represents the exact solution when C_S is at node 0 or node 3. The line on the squares represents the exact solution when C_S is at node 1 or 2. The dashed line on the triangles represents the approximate solution obtained with the approximate rise time model. The approximate solution of $t'_L + t'_R$ only depends on the value of C_S. However, the exact solutions of $t'_L + t'_R$ depend on both the value and position of C_S. The largest error rate of $t'_L + t'_R$ is 3.4% when C_S of 3 pF occurs at node 1 or 2. In the basic algorithm, the sum of the rise times was used to determine whether a finger touches a plate, but the exact solution of $t'_L + t'_R$ implies that we should consider the position of C_S as well as the sum of the adjusted rise times when deciding whether or not a finger touches a plate.

Figure 7 shows the angles of the rise time pair t'_L and t'_R versus C_S, where the line on the circles represents the exact solution and the dashed line on the triangles represents the approximate solution obtained with the approximate rise time model when C_S is at node 1. This figure shows that the angle obtained with the exact solution is changing with the variation of C_S, while the angle with the approximate solution is not changing. However, the largest error angle is 2.39° when C_S is 8 pF.

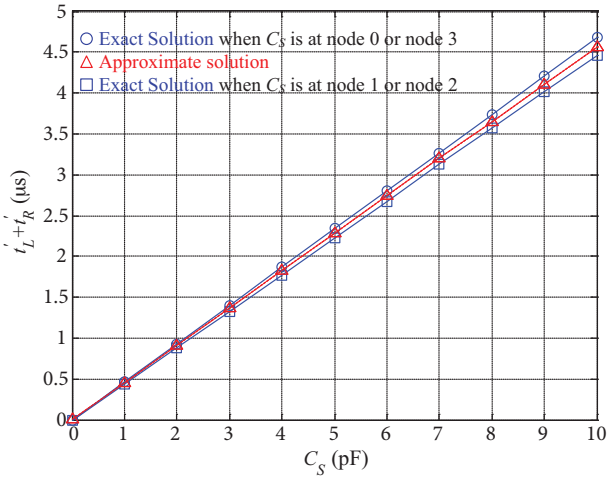

Figure 6. $t'_L + t'_R$ versus C_S.

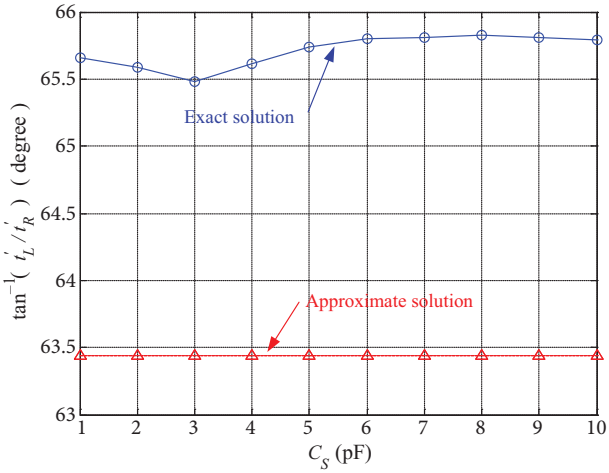

Figure 7. Angles versus C_S when C_S is at node 1.

3.3. Proposed algorithm

The proposed algorithm is shown in Algorithm 2, where N_L and N_R are measured values of t_L and t_R in digital form. We define $E(N_{L0})$ and $E(N_{R0})$ as the average values of N_L and N_R when C_S is zero. In step 1, the proposed method measures rise times N_L and N_R using the method in [1]. In step 2, the algorithm removes the effect of parasitic capacitances by subtracting E(N_{L0}) and E(N_{R0}) from N_L and N_R, respectively.

In Section 2, we described how the basic algorithm checks whether a finger touches a plate with the assumption that the sum of the two rise times only depends on the value of C_S. However, in Section 3.2, the sum of the two adjusted rise times, $t'_L + t'_R$, depends on both the value of C_S and the position of C_S. Thus, the proposed algorithm finds the position of C_S and then determines if the plate is touched by a finger.

Algorithm 2. Proposed algorithm

1 Measure rise times N_L and N_R;
2 $N'_L = N_L - E(N_{L0})$;
$N'_R = N_R - E(N_{R0})$;
3 $p = 0$;
for ($i = 0$; $i < 3$; $i = i + 1$)
If $\frac{N'_L}{N'_R} < \tan(\theta_{TH}(i))$, $p = i + 1$;
4 if ($N'_L + N'_R < N_\lambda(p)$) return –1;
else return p;

In step 3, the proposed algorithm finds the position of C_S. In step 4, the algorithm determines whether a finger touches the plate found in step 3 by comparing the sum of the adjusted rise times and a threshold value $N_\lambda(p)$, where p is the position of C_S.

4. Experimental results

A diagram and a photo of the experimental setup are shown in Figures 8 and 9, respectively. The proposed capacitive sensor with four touch switches was implemented on a field-programmable gate array (FPGA) except for the switches, comparators, resistor string, and some part of the rise time measurement circuit; these were implemented with discrete parts. The microcontroller unit (MCU) on the board controls the capacitive sensor and reads out the measured rise times via an inter-integrated circuit (I2C) interface. The measured rise times are then transferred to a PC for processing. The rise time measurement block, shown in Figure 2, was implemented with a method using multiphase clock signals [1]. In this experiment, 10-phase clock signals at 10 MHz were used. The resistance value of the resistor string was 100 KΩ, and C_S ranged from 0 to 10 pF with about a 1 pF step.

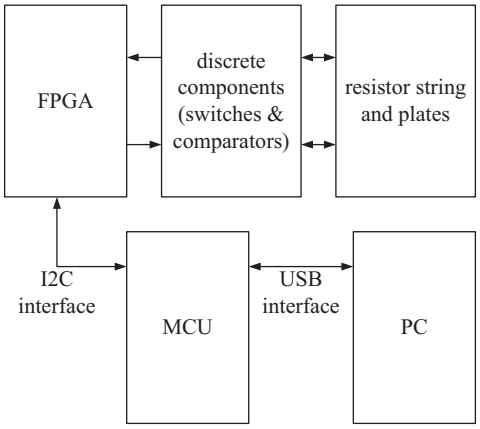

Figure 8. Diagram of the experimental setup.

The measured values of N_L and N_R are plotted in 2-D space in Figure 10, where each point is the average value of 4000 measurements. The average values of N_L and N_R when C_S is zero are $N_{L0} = 52.60$ and $N_{R0} = 55.13$, respectively. The values of N_{L0} and N_{R0} are not the same because the parasitic capacitances

at each node are not the same, and the resistances of the resistors in the resistor string do not match exactly. The four longest points from (N_{R0}, N_{L0}) at each line were measured when C_S was 10 pF.

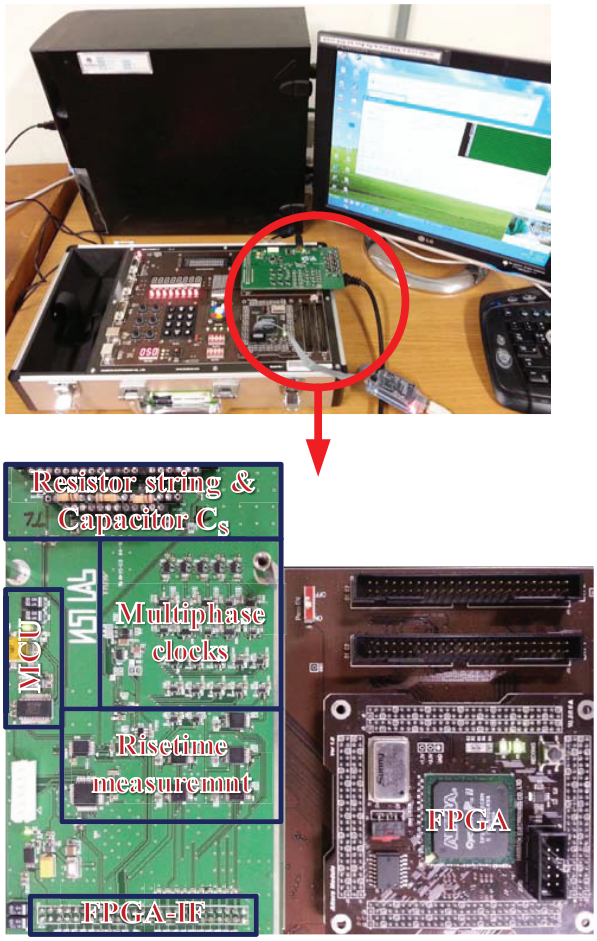

Figure 9. Photo of the experimental setup.

Figure 11 shows plots of adjusted rise times in 2-D space, where each point was obtained by subtracting N_{L0} and N_{R0} from the measured rise times N_L and N_R, respectively. The proposed algorithm is based on the assumption that the angles of the lines only depend on the position of C_S, and not the value of C_S. This experimental result shows that this assumption is quite reasonable.

Figure 12 shows the plots of the sum of the adjusted rise times N'_L and N'_R. In the approximate rise time model, the sum of the adjusted rise times t'_L and t'_R are always the same for a given value of C_S, but the simulation result showed that the sum is not always same. Figure 12 shows that $N'_L + N'_R$ depends on the position of C_S as well as on the value of C_S. The proposed algorithm shown in Algorithm 2 can cover this experimental result with different threshold values of $N_\lambda(p)$ for each node p, where $p = 0$ to 3. The algorithm determines whether C_S is larger than the smallest detectable capacitance by comparing $N'_L + N'_R$ and the threshold value $N_\lambda(p)$.

Figure 13 shows the angles of the lines in Figure 11. The average values of θ_1, θ_2, and θ_3 are 28.9°, 31.5°, and 28.6°, respectively. When the value of C_S is large, the graphs show stable results, but when C_S is

small, the lines on the triangles and squares move slightly upward. However, when $C_S = 1$ pF, the angles θ_1, θ_2, and θ_3 are 25.4°, 33.2°, and 31.0°, respectively, which is also applicable to the proposed algorithm.

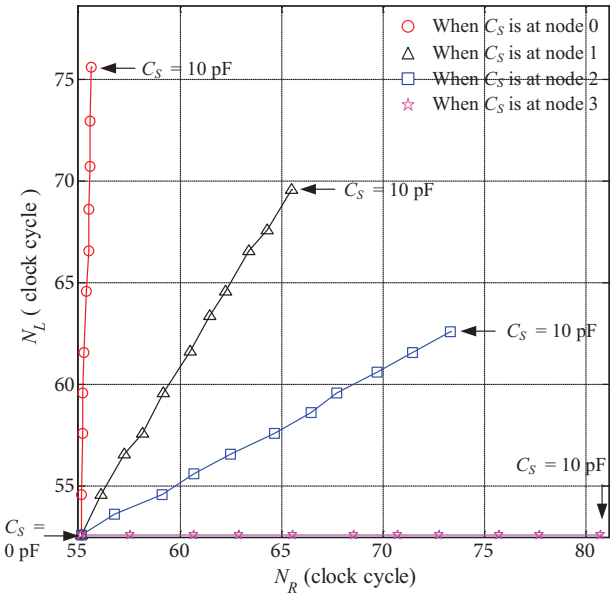

Figure 10. Plot of rise times N_L and N_R.

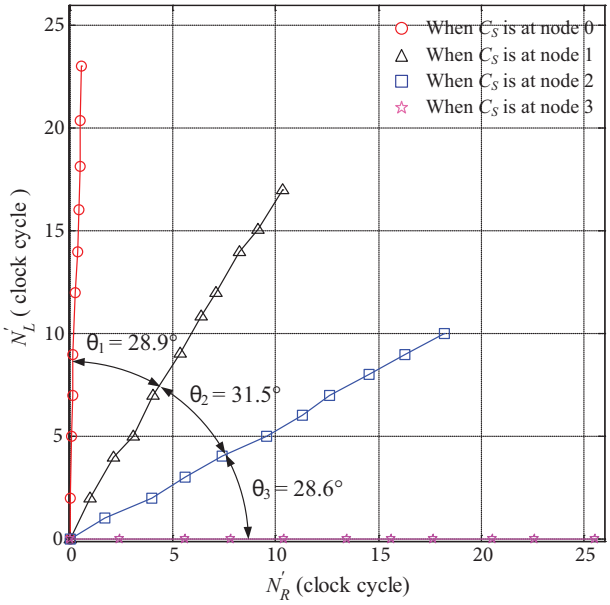

Figure 11. Plot of adjusted rise times N_L' and N_R'.

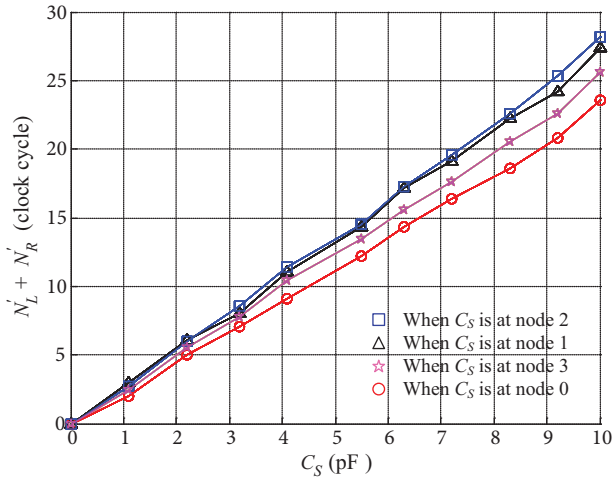

Figure 12. $N_L' + N_R'$ versus C_S.

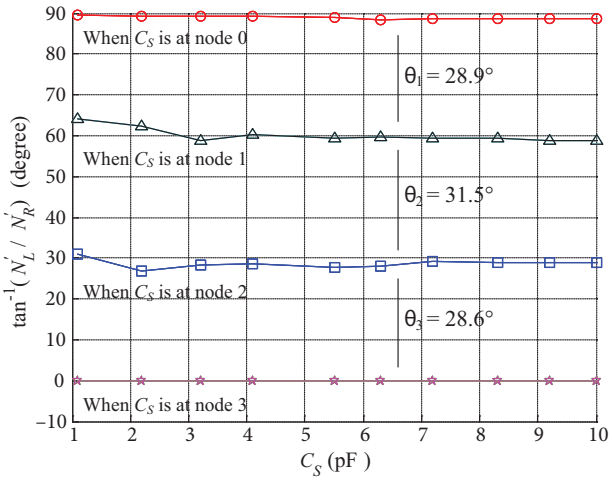

Figure 13. Angles of adjusted rise times versus C_S.

Now we will show the resolution of the proposed capacitive sensor. Figure 14 shows the sum of two measured rise times, N_L and N_R, versus the induced parasitic capacitance C_S when C_S is at node 0. The slope of the regression line obtained with the average values is 2.318 cycles/pF, and the maximum standard deviation is 0.4185 clocks/pF in this region. Thus, the resolution, which is defined as the maximum standard deviation over the slope of the graph, becomes 181 fF. In the same way, we measured resolutions when C_S was at nodes 1, 2, or 3: these are 139, 46, and 76 fF, respectively. Thus, the resolution of the capacitive sensor becomes 181 fF in the worst case.

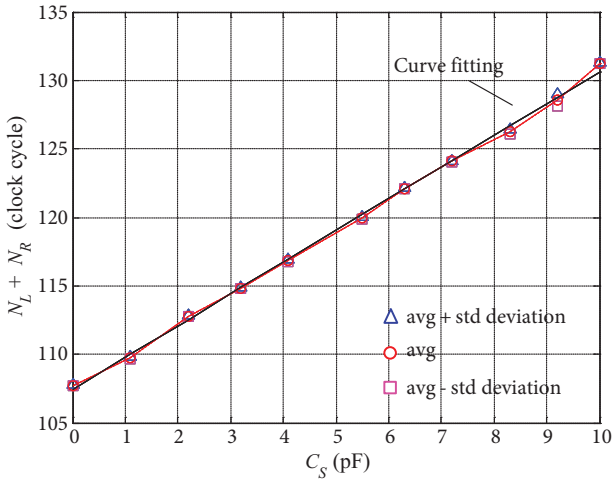

Figure 14. Graph for obtaining resolution when C_S is at node 0.

The proposed method was compared to the two previous works described in [10] and [1]. The summary of the comparison is shown in Table 3. The main focus of this study was to implement multiple touch switches using only two IC pins; thus, the pin efficiency is improved. In the experiment, the pin efficiency of the proposed method becomes two because four touch switches were implemented using two IC pins. However, the pin efficiency of the previous works is one. The rise time measurement method using multiphase clock signals [1] was applied to the proposed method, in which 10-phase clock signals were used. However, the previous work in [10] used a digital counter with a single clock to measure the rise time. The multiphase clock signals, which have the same frequency and are evenly spaced, give multiple rising edges within a clock cycle. Thus, it is possible to measure a rise time more accurately than with an existing single clock-based method. The resolution of a capacitive sensor is defined as the smallest detectable capacitance change. The resolutions of the proposed method and the work described in [1] are much better than that of the work in [10], because they use a more precise rise time measurement method based on multiphase clock signals compared to the other method's rise time measurement method. The resolution of the proposed method is not as good as that of the method described in [1] because the proposed method uses a resister string that generates more thermal noise. However, the resolution of the proposed method is still applicable to touch switch applications because the induced capacitance between a finger and a plate is on the order of a few picofarads and the resolution of the proposed method is 181 fF.

Table 3. Comparison of the proposed method and previous works.

	Ref. [10]	Ref. [1]	Proposed method
Pin efficiency	1	1	2
Rise time	Simple digital	Based on	Based on
measurement method	counter	multiphase clocks	
Resolution	754 fF	118 fF	181 fF

5. Conclusion

We propose a capacitive sensor that supports multiple touch switches with only two IC pins. The proposed method removes the effect of parasitic capacitance based on the proposed rise time model. In the model, the rise time is approximately expressed as two terms: one is due to parasitic capacitance and the other is due

to the capacitance induced by a finger and a plate. After removing the effect of parasitic capacitances, the ratio of the two rise times does not depend on the value of the induced capacitance. Rather, it depends on the position of the plate touched by a finger. The proposed method with four touch plates was implemented and the performance was measured. Our experimental results showed that the proposed capacitive sensor gives a resolution of 181 fF and can handle four touch switches.

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