A new high-performance current-mode fuzzy membership function circuit and its application

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Abstract: A new current-mode fuzzy-membership function circuit is proposed. The circuit has a very compact and simple architecture based on the simultaneous use of winner- and loser-take-all topologies. The circuit has also the advantage of easily adjusting generated membership function characteristics such as center or mean and width with a straightforward application of respective input currents. It is shown that the new circuit outperforms previous counterparts in terms of speed, power consumption, layout area, and robustness to variations in design parameters and errors. As an application, a fuzzy-classifier is designed with a new membership circuit as a seven fuzzy level controller.

Key words: Fuzzy logic, decision-making, current-mode circuit design, winner-take-all circuit, loser-take-all circuit

1. Introduction

A membership function of a fuzzy set is a representative measure for an object of interest as a member [1]. In fuzzy logic it refers to the degree of truth in part between 0 and 1. Fuzzy logic truth takes into account the membership in vaguely defined sets. Although fuzzy membership is not based on likelihood, it is characterized by similar axioms as probabilistic interpretation, e.g., the sum of fuzzy memberships of an object to all respective fuzzy sets is 1. Fuzzy classifiers or controllers assume that an object is assigned to a linguistically defined fuzzy set on the basis of majority.

The design of an analogue membership function circuit (MFC) has drawn considerable attention for accurate, low-cost implementation of fuzzy controllers. Operational transconductance amplifiers (OTA) have been utilized in realizing compact MFCs [2,3]. In OTA-based MFC designs device nonlinearities and biasing conditions limit performance and input range. On the other hand, the current-mode approach provides high-speed, low-switching voltage capabilities for MFC implementations [4]. Most major current-mode MFC designs have resorted to piece-wise linear (PWL) membership functions owing to the immediate simplicity of current summation/subtraction at the nodes, which makes it possible to achieve switching for a desired linguistic fuzzy rule. For example, designs in [4–7] rely on a truncated (or bounded) difference operation with prespecified slopes in linearity. On the other hand, differential-stage based MFC designs in [8,9] take advantage of the cascaded behavior of differential stages toward a Gaussian-like membership function with programmability of mean and width. In the latter the programmability is attained through transistors that operate in the triode region at the output nodes, while in the former it is simply obtained through suitably biasing voltages across the output current.

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However, they have the following common disadvantages: successive wired-arithmetic operations in the form of a current summation/subtraction reduce the maximum dynamic range of output, i.e. random design and process deviations and mismatches add up such that fuzzy sets will need larger intervals; the intense use of current-mirrors makes design discrepancies a serious issue; the choice of mirror type, e.g., the use of cascode mirrors, despite their better output response (i.e. small-signal output resistance), can limit the range of the input current given a supply voltage.

In this study a new current-mode fuzzy MFC is presented by combining both winner-take-all max (WTA-MAX) and loser-take-all min (LTA-MIN) topologies in simultaneous use. New MFC yields a Gaussian-like membership function with direct programmability of the resulting function. It is shown that the proposed design has much better design and performance characteristics compared with previous designs. As an application, a fuzzy controller/classifier with seven sets is designed with MFC.

## 2. Description of the proposed circuit

A new current-mode MFC shown in Figure 1a compares the input current I_{in} to the reference current of the k-th fuzzy set or class, $I_k = kI_b$, where I_b is a base current chosen fictitiously to represent the base fuzzy set, i.e. level 1, or a regular interval between sets. In the circuit with current source I_s, transistors M_A, M_C, M_{sw}, M_o, and M_l constitute a modified version of the LTA-MIN circuit given in [10], while transistors M_A, M_B, M_o and M_h form the well-known WTA-MAX circuit [11]. Transistor M_C in each cell is sized such that it operates with a small saturation voltage for a given I_s so that the output current $I_{k,out} = I_{k,l}$ follows the minimum of the inputs I_{in} and I_k as rapidly and closely as possible. It is seen that $I_{k,h} = \max(I_k, I_{in})$, and $I_{k,l} = \min(I_k, I_{in})$. The output current $I_{k,l}$ flows only when $I_{k,h} = I_{k,l}$; hence $I_{k,out} = I_k$ when $I_{in} = I_k$, otherwise $I_{k,out} = 0$. Because membership lies between 0 and 1, a (normalized) membership of the input for the k-th fuzzy set can be defined as $m_{in,k} = I_{k,out}/I_k$, which could be reproduced by mirroring $I_{k,out}$ by a factor of 1/k. Due to device and design properties, $I_{k,out}$ ($m_{in,k}$) will have nonlinear transition regions around I_k, which can be considered as a fuzzification rule for the respective fuzzy set as shown in Figure 1b. These regions can be adjusted with $M_{B,C}$ and the value of I_s such that neighboring $m_{in,k}$s intersect at a particular value of $m_{in,k}$, e.g., 0.5. It should be noted that transistor M_h can be removed from the circuit and node U can be directly tied up to a power supply (VDD) owing to the selective feature of the MAX circuit. The class label of the input, k_{in}, is determined as $k_{in} = \lceil \max(I_{k,out})/I_b \rceil$ by MAXing all $I_{k,out}$ (or $m_{in,k}$ in case of normalized outputs) terms in classification as shown in Figure 1c, where N is the number of fuzzy sets and '$\lceil\ \rceil$' refers to the nearest greater integer. It should be noted that by suitably choosing $I_{k,h}$ and $I_{k,l}$, the center and width of the membership function can be adjusted, which can also be done by regenerating these currents through mirror circuits externally.

## 3. Application of the new circuit in a fuzzy controller and simulation results

The proposed MFC and its predecessors in [4–7] using the PWL method and the design in [9] based on cascaded differential stages were designed and simulated for a seven-set/level fuzzy controller/classifier with respective membership functions. Simulations were performed using TSMC 0.25 μm HSPICE (level-49) parameters in full postlayout extraction with 1.8V supply voltage. In all designs body-biased effects were included and transistors were sized for optimum DC and transient characteristics with an input current range of 0 through 70 μA. Bias voltages V_{bn} and V_{pn} in [4] were obtained by using adequate voltage reference circuits formed of diode-

Transistor	$M_{l,h}$	$M_{B,C}$	$M_{A,o}$	M_{sw}
W(μm) /L(μm)	2.5 / 0.5	2.75 / 0.25	0.75 / 0.5	3.0 / 0.25
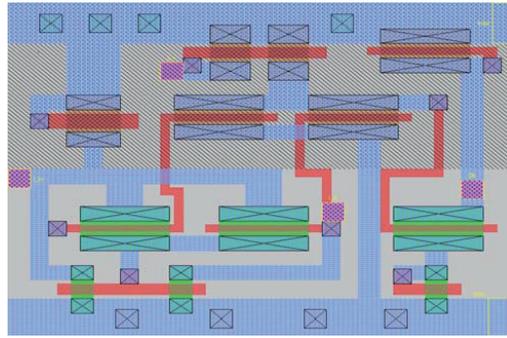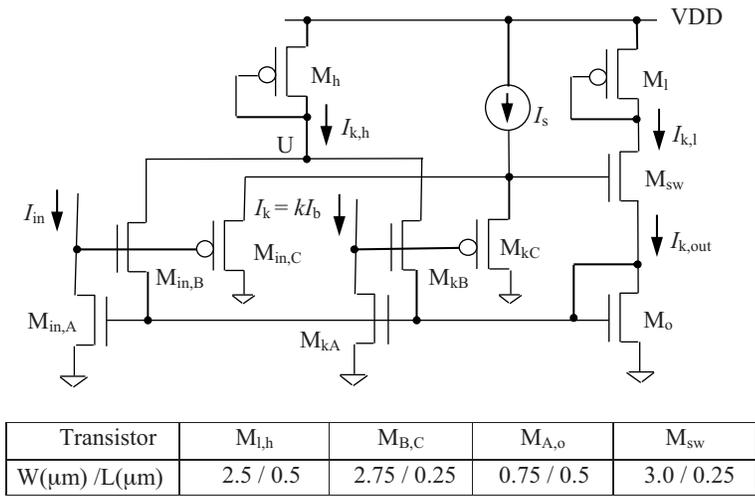
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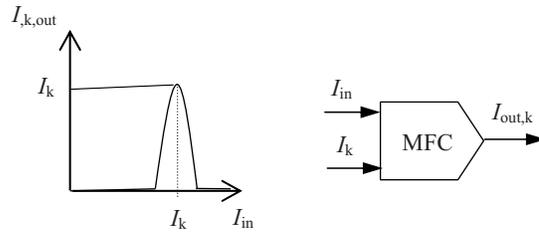
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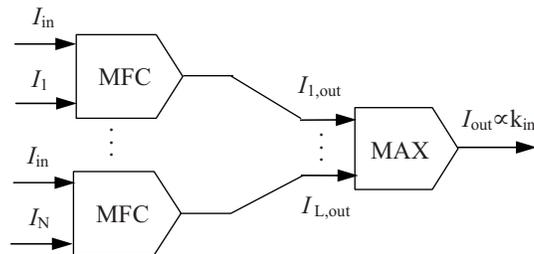
(c)

Figure 1. (a) Proposed MFC cell for the k-th fuzzy set, and its layout with TSMC $0.25\,\mu$m technology for k = 1; (b) its expected DC transfer characteristics and block representation; (c) fuzzy-classifier block representation.

connected PMOS and NMOS transistors, respectively. The base current I_b in this study, the reference current I_{ref} in [4–6], and the modal norm current I_{norm} used in [7] were taken at 10 μA and raised to the respective set reference levels for comparison by mirroring. Circuits in [4–7] were adjusted such that the linear membership functions of neighboring sets intersect at almost 0.5 with a transition slope of 1 at the rising and falling edges. For the design in [9], which employs cascaded differential stages, the bias current was chosen to be 10 μA with PMOS transistors of an aspect ratio W(μm)/L(μm) = 0.75/0.25, while the input transistors of the input stages were fixed to a suitable aspect ratio of W(μm)/L(μm) = 0.75/0.25 such that the mean values have resorted to the respective fuzzy levels described above, which corresponds to the input voltage difference of 1.1 V. The programmability transistors, which operate in the triode region, have been connected to VDD with suitable aspect ratios for the desired fuzzy level. The output of each design was conditioned on a diode-connected NMOS transistor with a dimensional aspect ratio of W(μm)/L(μm) = 0.75/0.25. All inputs were chosen as sourcing and they were reproduced, if necessary, using appropriate mirror circuits.

For the new MFC the sourcing inputs were reproduced and directed to the input nodes by using p-type current mirrors with transistors of a dimensional aspect ratio of W(μm)/L(μm) = 1.5/0.25. Bias current I_s was taken at 1 μA for all sets and it was reproduced by a diode-connected PMOS transistor with an aspect ratio of W(μm)/L(μm) = 0.5/1. Figure 2a illustrates a generic membership function m_{in} versus I_{in} with each curve representing $m_{in,k}$ centered at the respective reference current kI_b. As an application of the proposed MFC, a single-input fuzzy classifier shown in Figure 1c for seven sets was also designed without normalizing the outputs of the MFC cells to visualize the label of the set the input belongs to. Figure 2b illustrates transient simulation results of the designed classifier at k = 2, 4, and 6, i.e. class reference currents were applied at only these levels while reference inputs of other sets were left open. The designed classifier occupied a layout area of 458 μm^2 with 91 transistors and had delays of 2.4, 2.0, and 1.8 ns for k = 2, k = 4, and k = 6, respectively, while the average power drawn from VDD was found to be 6.1 mW for the input waveform shown in Figure 2b.

The designed MFCs were also examined concerning their robustness and reliability against discrepancies due to random design parameter variations and noise effects generated in devices [12] for determining a respective dynamic range. The output current for the k-th fuzzy set then is given by $I_{k,out}$ $(I_{in} = I_k) = I_k + \Delta I_k$, where the first component I_k is the nominal component, while ΔI_k refers to random variations. HSPICE DC simulation results indicated that the nominal component of the output current for the circuit given in Figure 1a satisfies linearity up to max(I_{in}) = 86 μA for all k values. On the other hand, a reliable operation given a fuzzy set/level characteristic of the design is determined by the second component of the output current. From a statistical point of view it is known that more than 90% of possible random occurrences, which obey a particular Gaussian distribution, reside within the range of 3 times the standard deviation around the nominal (mean) value. That is, for a safe operation within a chosen fuzzy set level, $|\Delta I_k| < 3\sigma_{\Delta I,k} < I_b$ / 2 [13]. For this objective, for each design studied I_{in} was varied between 0 and 70 μA, while I_k was kept at 20 μA, 40 μA, and 60 μA for k = 2, 4, and 6, respectively. For each k a set of 100-iteration Monte Carlo DC simulation analysis using a normal Gaussian distribution that represents the relative variations in aspect ratios (W/L) with a standard deviation of $\sigma_{\Delta W/W, \Delta L/L}$ =5% and variations in zero-body-bias threshold voltages (VTO) with a standard deviation of $\sigma_{\Delta VTO}$ =25mV was carried out. In each experiment of the analysis the quantity $\Delta m_{in,k} = (I_{k,out} - I_k)/I_k$, where $I_{k,out}$ is the output current with supplied design parameters of variations computed. As a merit for comparison, a DC dynamic range can be defined as DR$_k$ (dB) = 10log [| max(I_{in} /I_k) |^2/($\sigma_{\Delta m,k}$)^2], which simply illustrates the variation in $\sigma_{\Delta m,k}$ with k. The Table below presents some important characteristics of
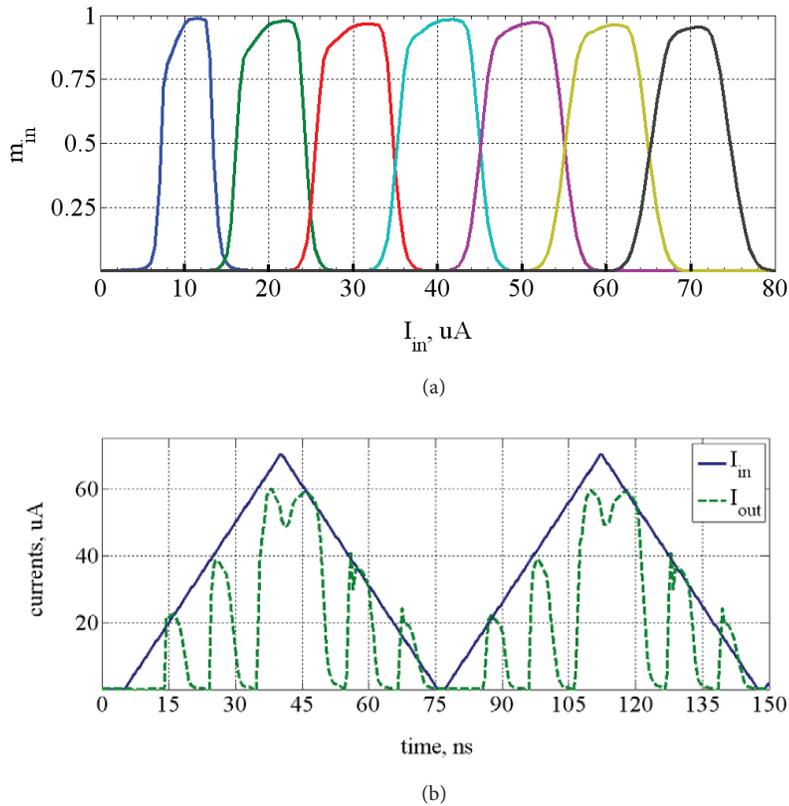
(a)

(b)

Figure 2. (a) Membership function DC characteristics of the proposed MFC for seven fuzzy sets; (b) transient simulation results of the designed classifier with proposed MFC for k = 2, 4, and 6.

the MFCs examined: number of transistors (NTR), layout area, dynamic range (DR_k), as well as the average power drawn from VDD (P_{VDD}) and delay τ_k for the input waveform in Figure 2b.

Table. Design characteristics of the proposed (New) and previous MFCs and their performance measures for input waveform in Figure 2b.

Design	NTR	Layout area $(\mu m)^2$	$DR_k(dB) - \tau_k$ (ns)			P_{VDD} (mW)
			k = 2	k = 4	k = 6	
New	10	91.8	58 − 1.5	56 − 1.2	56 − 1.0	1.6
[4]	16	132.4	54 − 2.1	53 − 1.9	53 − 1.5	2.9
[5]	26	229.6	50 − 2.3	46 − 2.0	47 − 1.9	3.5
[6]	32	269.5	48 − 2.7	44 − 2.4	43 − 2.1	4.2
[7]	28	256.9	51 − 2.7	48 − 2.3	45 − 2.1	4.0
[9]	18	294.6	47 − 3.2	42 − 2.6	41 − 2.4	2.7

4. Conclusions

A new simple-architecture, high-performance current-mode membership-function circuit is described. The new circuit has the architectural advantage that the generated function can be modified in shape externally. It is shown that the new circuit exhibits much better performance characteristics in terms of speed, power consumption, layout area, and robustness to parametric variations than previous designs. These characteristics are expected to make the new MFC a reliable unit for neuro-computational and decision-making applications.

Acknowledgment

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