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Performance evaluation of three phase SRF-PLL and MAF-SRF-PLL

Anirban GHOSHAL*, **Vinod JOHN**
Department of Electrical Engineering, IISc Bangalore, Bangalore, India

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Abstract: Synchronous reference frame phase locked loop (SRF-PLL) is a well established technique used for maintaining synchronism of a grid connected VSI with an electric grid. Many methods of PLL are present in the literature to achieve improved performance under nonideal grid condition. These solutions are based on SRF-PLL structure along with some modification to achieve improved performance. It is observed that faster and better performance are achieved at the expense of more computations. Moving average filter (MAF) SRF-PLL structure is one such solution that consumes less resources and gives a reasonably fast response. In this work the performance of a MAF-SRF-PLL structure is evaluated in terms of unit vector distortion and settling time under various nonideal grid conditions. Its performance is compared with that of two differently designed SRF-PLLs. This evaluation gives a clear idea about possible utilizations of these PLL structures under different possible nonideal grid conditions.

Key words: Phase locked loop, SRF-PLL, MAF-SRF-PLL, Grid connected VSI

1. Introduction

Phase locked loop (PLL) or unit vector generation is an important part of the control unit of a grid connected power converter [1–3]. Open loop type of methods such as zero crossing detection [4] and stationary reference frame PLL [5–7] do not produce accurate phase information when the grid is nonideal. The closed loop approach based on synchronous reference frame (SRF) theory, popularly known as SRF-PLL, shows better phase tracking ability [1,2] under nonideal grid situations. However, its performance in terms of response time and quality of generated unit vectors deteriorates [8,9].

Design methods of SRF-PLL can be based on bandwidth selection as well as unit vector quality in terms of THD [1,2,9]. A SRF-PLL with low bandwidth can show better phase tracking and unit vector generation ability under nonideal grid condition [9]. To achieve a fast response and better quality unit vector under nonideal grid condition several topologies of PLL have been suggested by researchers [8,10,11]. It can be observed that most of the improved solutions use the basic SRF-PLL structure and some modification to address nonideal situations. These PLL structures can be classified as follows:

- SRF-PLL with filters: Different filters such as low pass, notch, and MAF are used to filter out the noise part in the closed loop structure of SRF-PLL generated due to nonideal grid conditions [10,12–15].
- Multiple reference frame based SRF-PLL: DDSRF-PLL structure uses two reference frames, both positive sequence and negative sequence, for extraction of phase and frequency information [8]. In MSRF-PLL topology separate reference frames are used for each phase [16].

*Correspondence: ghoshal.anirban@gmail.com

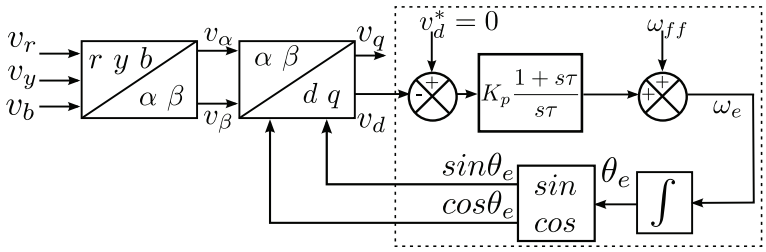


Figure 1. Block diagram structure of a three phase SRF-PLL.

- SRF-PLL with prior signal conditioning: In this method signal conditioning units or filters are used on sensed signals prior to being utilized as input to SRF-PLL. Examples of this method include using resonant integrators for SSI-PLL [17] and DSOGI-PLL [18,19]. Another method, which is known as cascaded delay compensation, uses multiple filter structures for signal conditioning [11].

In general, faster and better results have been shown to be achieved at the expense of more computations [11]. In this regard, MAF-SRF-PLL is a solution that consumes significantly less computational resources and can perform reasonably well under several nonideal grid conditions [12,20].

Performance evaluation of PLL structures has generally been done by observing error in phase angle estimation for different grid conditions. Total harmonic distortion (THD) of generated unit vectors can also be used for performance evaluation and it has been utilized for design of SRF-PLL [9] and SOGI-PLL. However, performance evaluation of MAF-SRF-PLL using THD of unit vectors under different nonideal grid conditions does not exist in the current literature.

In this paper, extensive results, both simulation and hardware utilizing a grid simulating inverter, are presented on the performance of MAF-SRF-PLL under several nonideal grid conditions including fault situations. Its performance is compared with that of two designs of SRF-PLL, one of which is slow in response while the other has a faster response. Such an evaluation gives a clear idea about possible utilizations of these PLL structures considering different possible grid conditions and the possibility of providing ride-through ability to a grid connected converter.

In this paper, Section 1 contains the introduction to the topic addressed. Modeling, design equations, and a brief discussion on SRF-PLL are given in Section 2. Simulation results carried out using MATLAB are provided in Section 4. The experimental results obtained by utilizing a grid simulating inverter are presented in Section 5. The conclusions on this topic are presented in Section 6.

2. Operation of three phase SRF-PLL

A block diagram representation of a three phase SRF-PLL is shown in Figure 1. The inputs to PLL are three phase voltages v_r, v_y and v_b. Under balanced condition, the equations representing three phase voltages are given by (1).

$$v_i = V_m cos(\omega t - \frac{2\pi k}{3}) \qquad for(i,k) = (r,0),(y,1),(b,2) \tag{1}$$

To obtain phase information v_r, v_y, and v_b are transferred into a stationary two phase '$\alpha\beta$' system. The voltages in the '$\alpha\beta$' system, v_α and v_β, are related to v_r, v_y, and v_b by (2).

$$v_\alpha = \frac{3}{2} V_m \, cos(\omega t) \qquad and \qquad v_\beta = \frac{3}{2} V_m \, sin(\omega t) \tag{2}$$

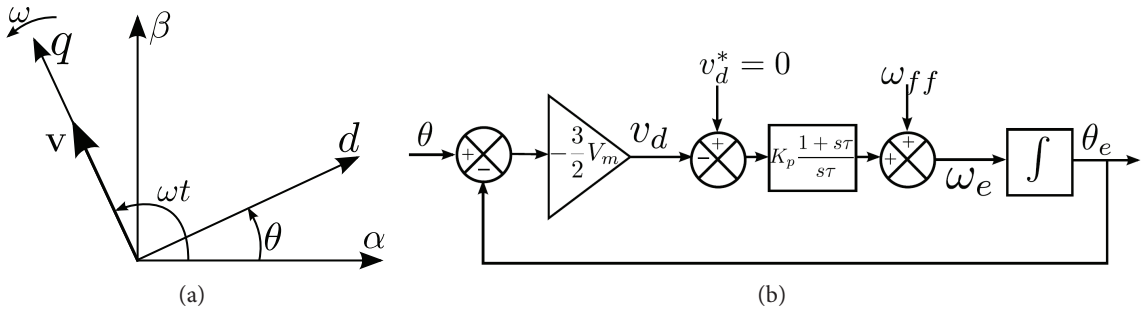


Figure 2. (a) Phase angle estimation by aligning voltage space phasor **V** along 'q' axis. (b) Simplified block diagram of SRF-PLL.

The phase angle θ, shown in Figure 2, can be obtained by synchronizing the voltage space vector **V** either along the q-axis or along the d-axis of a synchronously rotating reference frame. Let us assume that **V** is to be aligned with the q-axis as shown in Figure 2. Then the position of the d-axis that makes an angle θ with the stationary α-axis is related to 'ωt' by (3).

$$\theta = \omega t - \frac{\pi}{2} \tag{3}$$

In the PLL structure, shown in Figure 1, θ gets estimated as θ_e by integrating estimated frequency ω_e, which is the summation of the output of the PI controller and the feed-forward frequency ω_{ff}. Instantaneous voltages in synchronously rotating 'dq' reference frame can be found using θ_e from (4) and (5).

$$v_d = -\frac{3}{2} V_m \, sin(\theta - \theta_e) \tag{4}$$

$$v_q = \frac{3}{2} V_m \, cos(\theta - \theta_e) \tag{5}$$

The controller gains are designed such that v_d follows the reference value, which will result in the estimated frequency ω_e locking to system frequency ω and the estimated phase angle θ_e being equal to the phase angle θ. This is the phase locked situation under balanced condition and θ_e can be related to ωt by (3). Therefore, for balanced grid voltage condition, under the phase locked situation $sin\theta_e = -cos(\omega t)$. Hence under phase locked situation unit vector $sin\theta_e$ will be at phase opposition to R phase voltage v_r.

Now, if $\theta_e \approx \theta$ then the space vector of voltage **V** gets aligned to the q-axis as shown in 2(a). Hence, from (4) the voltage vector along the synchronously rotating d-axis can be linearized to (6).

$$v_d = -\frac{3}{2} V_m \, (\theta - \theta_e) \tag{6}$$

Thus, the overall system in Figure 1 can be simplified to that shown in Figure 2(b) using (6). Detailed analysis and design of PI controller gains can be found in references [1,2,9]. Here values of different loop parameters of SRF-PLL were calculated by using the second order loop model described in [2]. The transfer function between θ_e and θ is given in (7). Comparison of (7) with a standard second order system gives the expressions, shown in (8), for natural frequency (ω_n) of the closed loop SRF-PLL structure and damping coefficient (ζ_{pll}) in terms

Table 1. Value of loop parameters of SRF-PLL.

System	V_m	ζ_{pll}	ω_n	K_p	τ	τ_s
SRF1	$230\sqrt{2}\ V$	0.707	$62.8\ rad/s\ (10\ Hz)$	0.18	0.0225	$90\ ms$
SRF2	$230\sqrt{2}\ V$	0.707	$566\ rad/s\ (90\ Hz)$	1.16	0.0035	$10\ ms$

of other system parameters.

$$\frac{\theta_e(s)}{\theta(s)} = \frac{\frac{3V_mK_p}{2\tau}(1+s\tau)}{s^2 + \frac{3V_mK_p}{2}s + \frac{3V_mK_p}{2\tau}} \tag{7}$$

$$\omega_n = \sqrt{\frac{3V_mK_p}{2\tau}} \qquad and \qquad \zeta_{pll} = \frac{3V_mK_p}{4\omega_n} \tag{8}$$

Further, using (8) the PI controller parameters can be expressed as shown in (9).

$$K_p = \frac{4\zeta_{pll}\omega_n}{3V_m} \qquad and \qquad \tau = \frac{3V_mK_p}{2\omega_n^2} \tag{9}$$

The design criteria for SRF-PLL can be decided in two different ways. The first one is by selecting ζ_{pll} and ω_n, which is also the corner frequency of the closed loop system, to obtain the desired damping and filtering performance. The system parameters under the name SRF1, shown in Table 1, are designed based on $\zeta_{pll} = 0.707$ and $\omega_n = 62.8\ rad/s$. The second approach, named SRF2, is by selecting a settling time (τ_s) and ζ_{pll}. For a second order system the τ_s and ω_n are related by $\tau_s = \frac{4}{\zeta_{pll}\omega_n}$ following the 2 % criterion [21]. In this case, the system parameters are designed based on $\zeta_{pll} = 0.707$ and $\tau_s = 10\ ms$, which results in $\omega_n = 566\ rad/s$. Here the designs were chosen such that SRF1 has better filtering ability but this results in a slower response. In contrast, SRF2 has been designed for faster response time but this makes SRF2 poorer in filtering ability. Parameters of the two SRF-PLLs are listed in Table 1. In Section 4 and Section 5, these two SRF-PLLs are compared with a MAF-SRF-PLL designed to have good filtering ability such that the THD of the unit vector is around 1% with a reasonably fast response time of nearly 60 ms.

3. MAF-SRF-PLL

A moving average filter (MAF) is a simple FIR filter. The purpose of using a MAF along with a SRF-PLL is to attenuate the ripple components in estimated v_d and v_q generated due to the presence of unbalance and harmonics. A simplified block diagram of the MAF-SRF-PLL is shown in Figure 3.

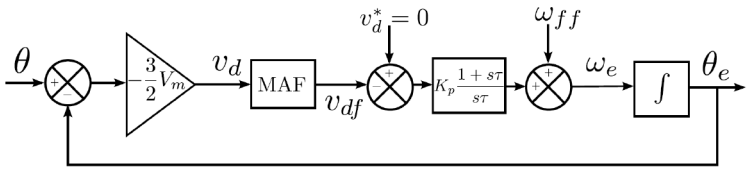


Figure 3. Simplified block diagram of MAF-SRF-PLL.

The unbalance in grid voltage produces a 2nd order ripple, i.e. 100 Hz ripple when grid frequency is 50 Hz, in estimated values of v_d and v_q. Similarly, the harmonic voltages of order $6n \pm 1$ present in the grid are

of concern. Because of transformation into the synchronously rotating reference frame these harmonic voltages appear as $6n$ harmonic. If by using a MAF the $2nd$ harmonic due to negative sequence voltage is cancelled, then the $6n$ harmonics also get cancelled as they are integer multiples of $2nd$ order harmonic. To cancel the $2nd$ harmonic, averaging has to be done over an even number of samples within its period. The settling time of this MAF will be equal to the time period of the $2nd$ harmonic. If the fundamental frequency is f and system sampling frequency is F_s then there would be N number of samples within the period of $2nd$ harmonic where $N = \frac{F_s}{2f}$. Generally, 'N' is a large number and if a MAF is designed to take an average over all these data then a large amount of storage would be necessary. Again N may not be an even number and hence there is a chance of error being introduced in the averaging process. For these reasons the use of a downsampler is proposed here to reduce the amount of data storage and to keep an even number of samples within the $2nd$ harmonic time period. Using a downsampler means that the controller receives information about changes in grid voltage at a slower rate. In this paper the design of the MAF-SRF-PLL and its bandwidth selection is based on [12]. Transfer function of such a filter is given by

$$H(z) = 0.1\sum_{i=1}^{9} z^{-i} \tag{10}$$

Downsampling rate should not be so small such that system dynamics are affected. In this work the system sampling frequency is $10kHz$ and the downsampling rate is at $1kHz$, resulting in only 10 samples necessary for the MAF.

4. Numerical comparison

For verification of the working principles of 3-Φ SRF-PLL and the 3-Φ MAF-SRF-PLL a MATLAB based simulation study was carried out. The performances of the PLL structures in terms of settling time and THD of unit vectors were observed. Both balanced and unbalanced conditions of grid voltage were considered for study.

Table 2. Comparison of simulation results on settling time under balanced grid voltage.

System	Designed Bandwidth in rad/s	Settling time in ms	
		Estimated	Observed
SRF1	62.8	90	90
SRF2	566	10	15
MAF-SRF	158	51	60

4.1. Balanced grid voltage

Under balanced grid voltage condition the settling times of SRF1, SRF2, and MAF-SRF-PLL were observed and compared with expected settling times from designed bandwidth of individual PLL structures.

The start-up performance of SRF1 PLL is shown in Figure 4(a) and Figure 4(b). It can be observed from Figure 4(a) that θ_e is able to follow grid phase angle θ and under phase locked condition $sin\theta_e$ is in phase opposition with R phase voltage v_r. The error in phase angle detection θ_{err}, which is given by $\theta_{err} = \theta - \theta_e$, and estimated frequency f_e show a settling time of nearly 90 ms, as can be observed from Figure 4(b).

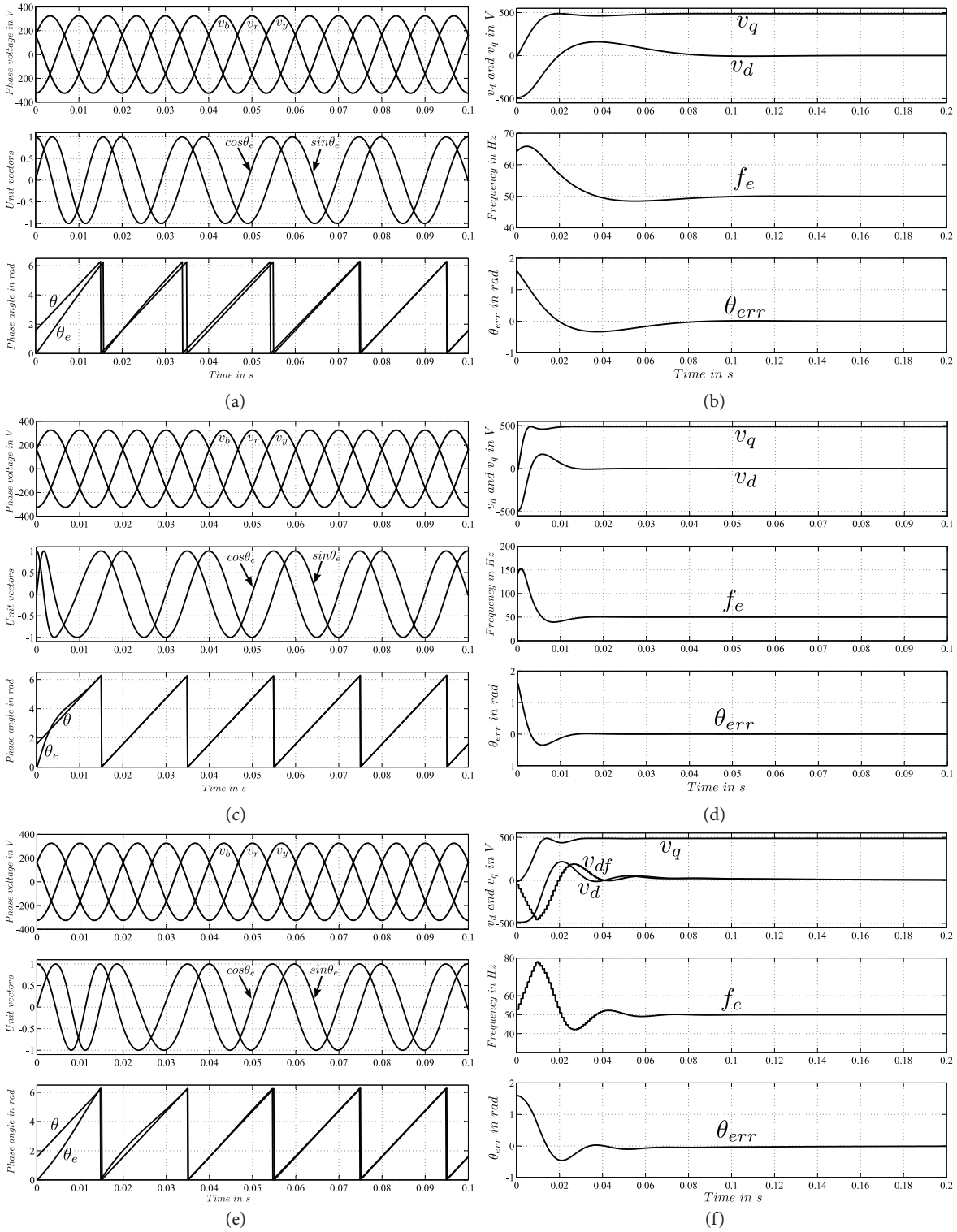


Figure 4. Simulation results of PLL performances under balanced condition. (a) & (b) → SRF1 PLL. (c) & (d) → SRF2 PLL. (e) & (f) → MAF-SRF-PLL. (a),(c) & (e): Start-up performance showing unit vectors and phase angle tracking. (b), (d) & (f): Estimation of v_q and v_d, estimated frequency f_e and error in phase angle tracking θ_{err} during start-up.

The start-up performance of SRF2 PLL is shown in Figure 4(c) and Figure 4(d). The steady state performance is similar to that of SRF1 PLL. However, as in the design condition a lower settling time was selected and so a smaller settling time compared to SRF1 can be observed from θ_{err} and f_e responses as shown in Figure 4(d). Here the settling time can be observed to be within 15 ms.

The simulation results for start-up performance of the MAF-SRF-PLL under balanced grid voltage condition are shown in Figure 4(e) and Figure 4(f). The phase tracking ability of this PLL structure can be observed from Figure 4(e). The settling time of the designed MAF-SRF-PLL is found to be nearly 60 ms from observation on response of θ_{err} as shown in Figure 4(f).

The comparison of settling times along with designed bandwidth is given in Table 2. It can be concluded that a MAF-SRF-PLL with its superior filtering ability can be designed to have a settling time of 60 ms, which is 3 fundamental cycles in a 50 Hz system.

4.2. Unbalanced grid voltage

The performances of SRF1, SRF2, and MAF-SRF-PLL under unbalanced grid voltage condition and during start-up are shown in Figure 5. These results are for an unbalanced grid voltage condition when one phase voltage is at 85% of the nominal voltage and the other two phase voltages are at nominal voltage. By the definition of unbalance given in [22] this condition has nearly an unbalance of 5%. From these results it can be observed that the settling time responses are similar to that for the balanced situation. From Figure 5(b) and Figure 5(d) it can be observed that due to the negative sequence a 100 Hz signal is present in v_d, v_q, f_e, and θ_{err}. However, Figure 5(f) shows that the MAF-SRF-PLL is capable of attenuating the 100 Hz ripple present in v_d sufficiently.

A quantitative assessment of the unit vector qualities in terms of THD for two cases of unbalance are shown in Figure 6. In the first case, R phase voltage is reduced to 85% of its nominal voltage causing a 5% unbalance [9,22]. For the second case, the R phase voltage is reduced to 50% of its nominal voltage, causing around 16% of unbalance. For both cases, SRF1 PLL is able to generate unit vectors with THD of either less than or nearly 1% as shown in Figure 6(a) and Figure 6(b). As SRF2 PLL has a higher bandwidth the unit vectors produced by it are significantly distorted, which can be observed from the THD values shown in Figure 6(c) and Figure 6(d). However, for MAF-SRF-PLL due its ability to provide superior attenuation at 100 Hz the THD of the generated unit vectors are nearly 0% for both the conditions of unbalance, shown in Figure 6(e) and Figure 6(f).

Hence it can be concluded that the MAF-SRF-PLL is capable of generating superior quality unit vectors with reasonably fast time response. However, experimental validation of its operational qualities was done under several nonideal conditions. The results of those experiments are discussed in the next section.

5. Experimental evaluation

The above discussed MAF-SRF-PLL and SRF-PLL methods were implemented and tested for different conditions using Altera's cyclone-II series FPGA boards. For experiments the required three phase voltage signals were either derived from an available three phase grid or created using an inverter with a LCL filter. The FPGA controlled inverter with a LCL filter has been used to generate different nonideal conditions such as unbalanced grid voltage, distorted grid voltage, and voltage sag. At the output terminals of the LCL filter a balanced set of three phase resistor was connected. The neutral point of the star connected resistor was connected to the mid point of the DC bus capacitor of the inverter. Voltage drop across the resistors was sensed and taken as

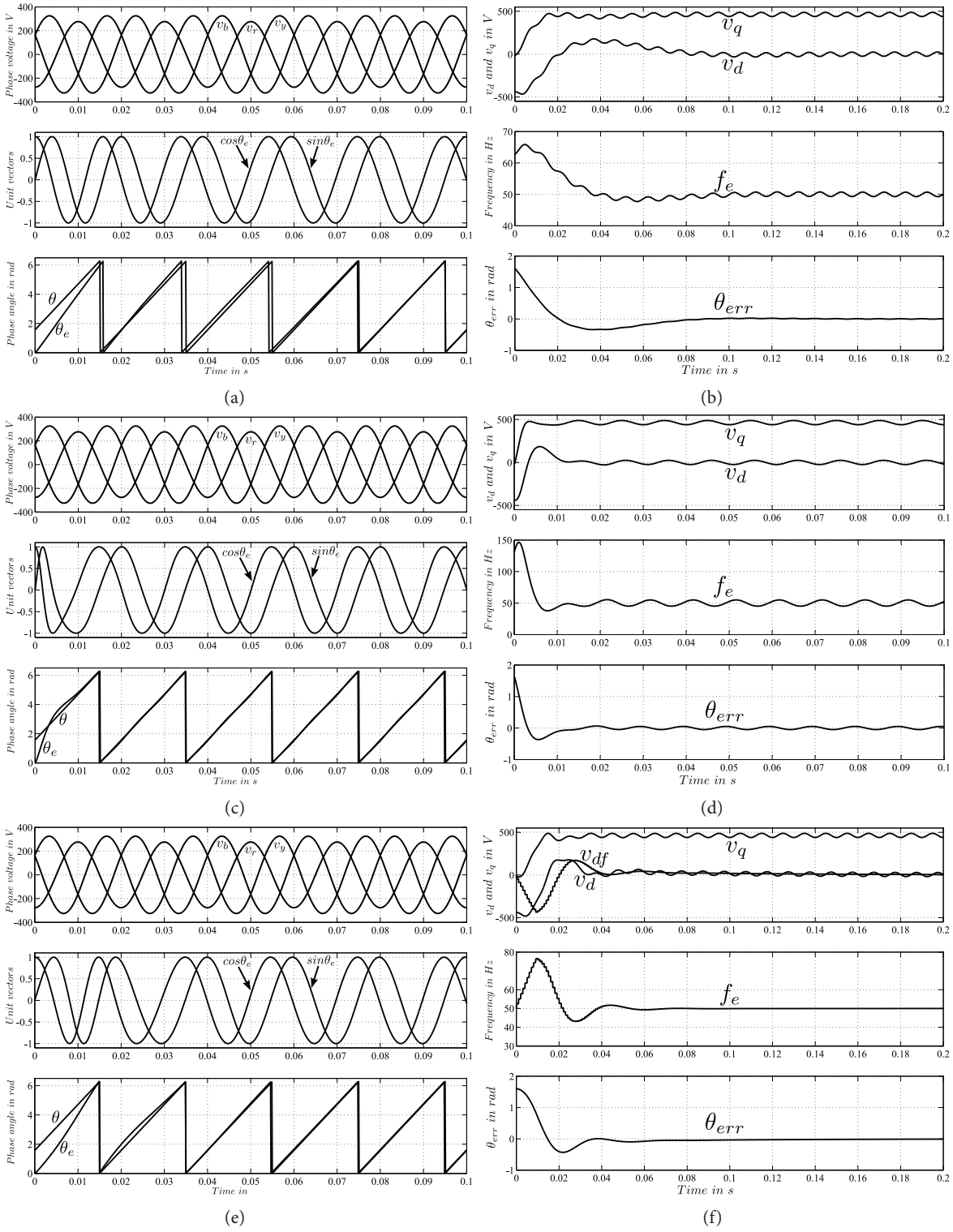


Figure 5. Simulation results of PLL performances under unbalanced condition. (a) & (b) → SRF1 PLL. (c) & (d) → SRF2 PLL. (e) & (f) → MAF-SRF-PLL. (a),(c) & (e): Start-up performance showing unit vectors and phase angle tracking. (b), (d) & (f): Estimation of v_q and v_d, estimated frequency f_e and error in phase angle tracking θ_{err} during start-up.

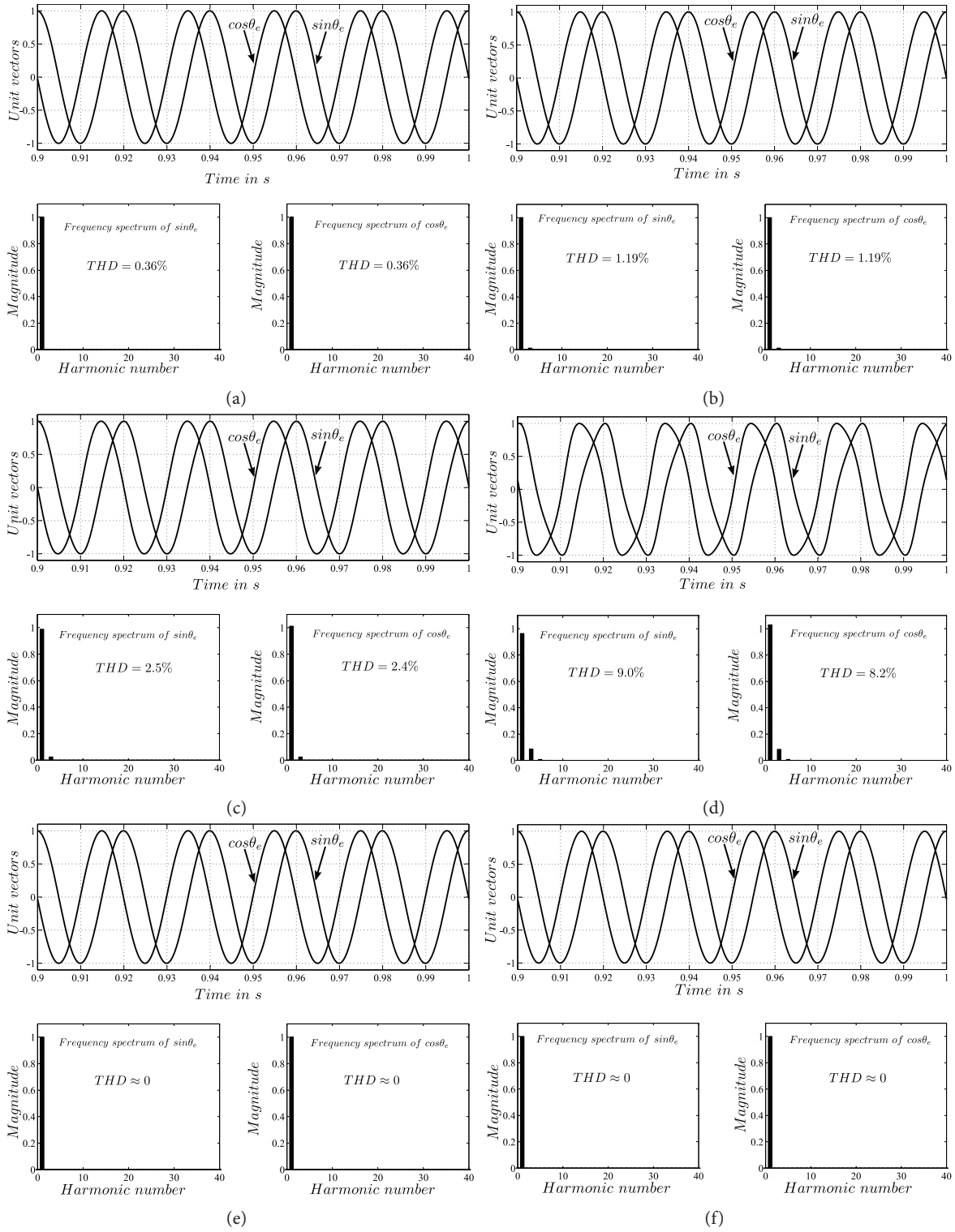


Figure 6. Generated unit vector quality under unbalanced condition. SRF1 PLL with one phase at (a) 85% of nominal voltage and (b) 50% of nominal voltage. (c) SRF2 PLL with one phase at (c) 85% of nominal voltage and at (d) 50% of nominal voltage. MAF-SRF-PLL with one phase at (e) 85% of nominal voltage and at (f) 50% of nominal voltage.

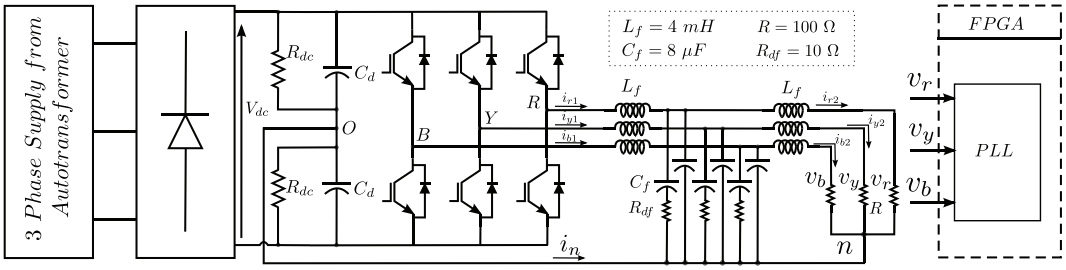


Figure 7. Hardware configuration for experimental verification of PLL algorithms.

Table 3. Comparison of PLL performances under balanced grid voltage condition.

System	THD of unit vector		Settling time
	$cos\theta_e$	$sin\theta_e$	
SRF1	0.89%	0.85%	100 ms
SRF2	1.08%	1.02%	10 ms
MAF-SRF	0.88%	0.95%	60 ms

input for testing PLL performance. This hardware system, shown in Figure 7, was utilized to produce several nonideal grid conditions to assess the PLL structures. The PLL algorithms were implemented in FPGA. The computation was carried out in the fixed point arithmetic method with a register size of 16 bit. The clock frequency of the FPGA was set at 20 MHz and the total execution time of the MAF-SRF-PLL was found to be 2.5 μs. Settling time and quality of produced unit vectors in terms of THD were chosen as the performance assessment indices. The tabulated values of THD of both $sin\theta_e$ and $cos\theta_e$ were calculated from the stored data on generated unit vectors. An off-line frequency spectrum analysis was carried out on each set of data and from which THD of unit vectors was calculated. Each of the tabulated results on THD is actually an average of 20 such sets of data.

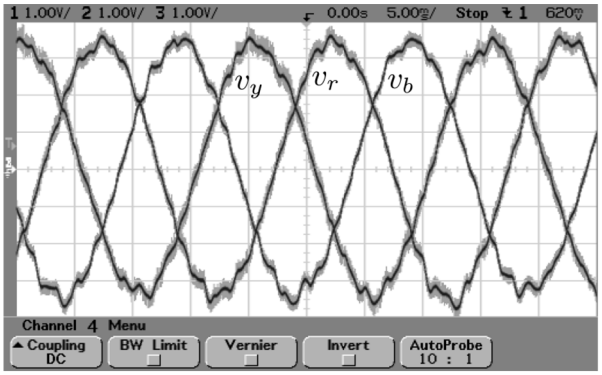
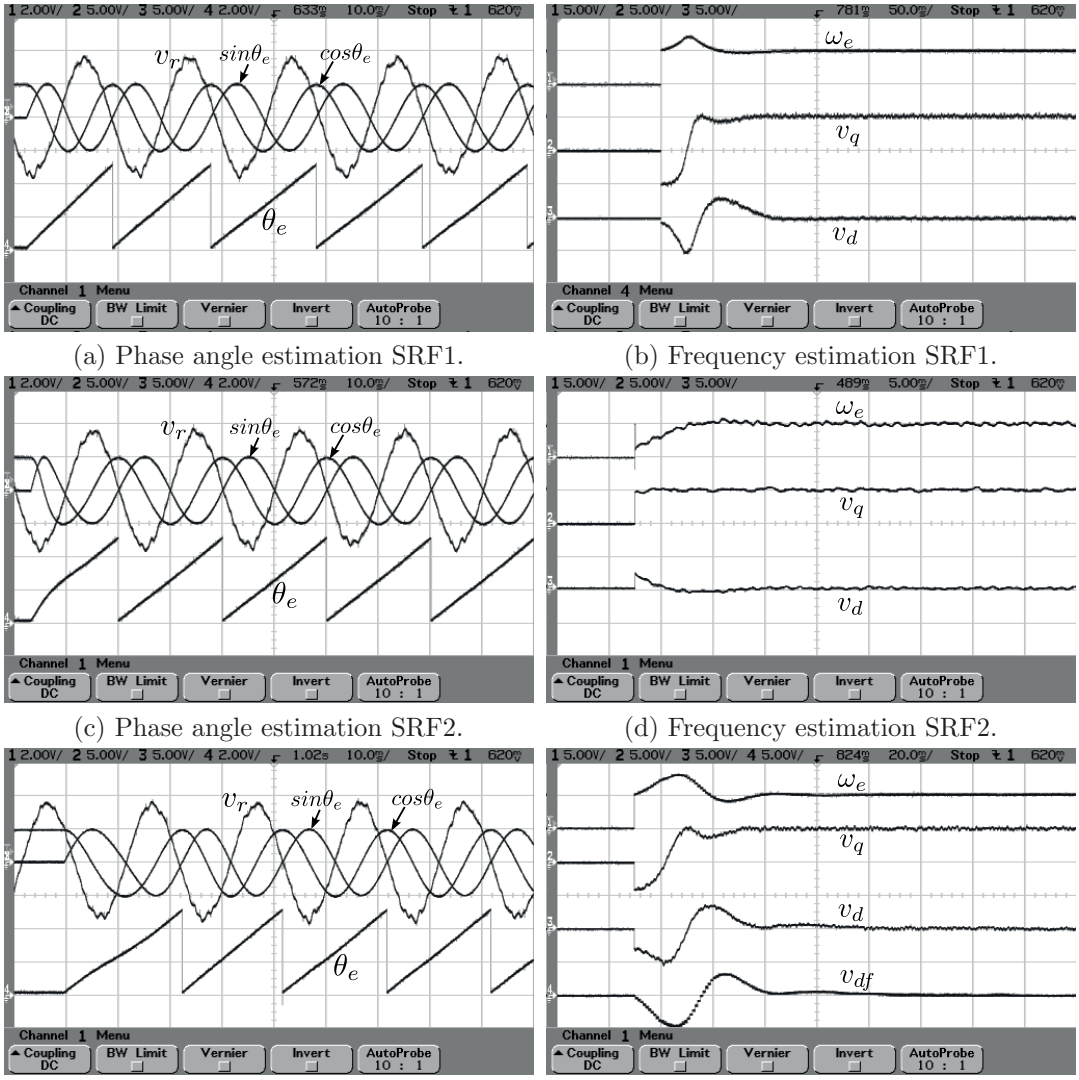


Figure 8. Three phase balanced voltage waveform generated using LCL filter with inverter for testing of PLL schemes. Scale: X-axis: 5 ms/div and Y-axis: 90 V/div.

5.1. Balanced condition

The performance of the MAF-SRF-PLL was tested under balanced condition of three phase grid voltage and compared with SRF1 and SRF2 PLL. The applied test voltage waveforms are shown in Figure 8. The start-up performance of SRF1 is shown in Figure 9. Under phase locked condition the R-phase voltage v_r and unit



(a) Phase angle estimation SRF1. (b) Frequency estimation SRF1.

(c) Phase angle estimation SRF2. (d) Frequency estimation SRF2.

(e) Phase angle estimation MAF-SRF. (f) Frequency estimation MAF-SRF.

Figure 9. Experimental results on phase tracking under balanced grid voltage condition.

vector $sin\theta_e$ maintains a 180° phase relationship, shown in Figure 9(a), as explained in Section 2. The frequency estimation shown in Figure 9(b) has a settling time of nearly 100 ms, which is close to the designed settling time. The THD of unit vectors, tabulated in Table 3, were found to be 0.89% and 0.85%, respectively, for $cos\theta_e$ and $sin\theta_e$. Similar observations in Figure 9(c) and Figure 9(d) show that the settling time for SRF2 PLL is nearly 10 ms and the unit vector THDs are 1.08% amd 1.02%. Figure 9(e) shows the start-up performances of the MAF-SRF-PLL. The settling time for the MAF-SRF-PLL is around 60 ms, which can be observed from Figure 9(f). The THD of unit vectors for the MAF-SRF-PLL was found to be 0.88% and 0.95% for the sine and cosine unit vectors, respectively. These data are tabulated in Table 3. Hence it can be concluded that the MAF-SRF-PLL is capable of giving similar performance in terms of unit vector THD under balanced condition of grid voltage as that of SRF1 and SRF2. The PLL method SRF2 has the fastest response time among the three PLLs and the MAF-SRF PLL is capable of giving a faster response compared to SRF1, which is a low bandwidth PLL.

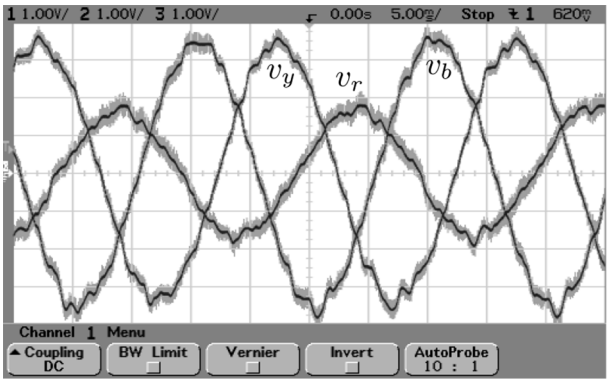


Figure 10. Three phase unbalanced voltage waveform generated using LCL filter with inverter for testing of PLL schemes. Scale: X-axis: 5 ms/div and Y-axis: 90 V/div.

Table 4. Comparison of PLL performances under unbalanced grid voltage condition.

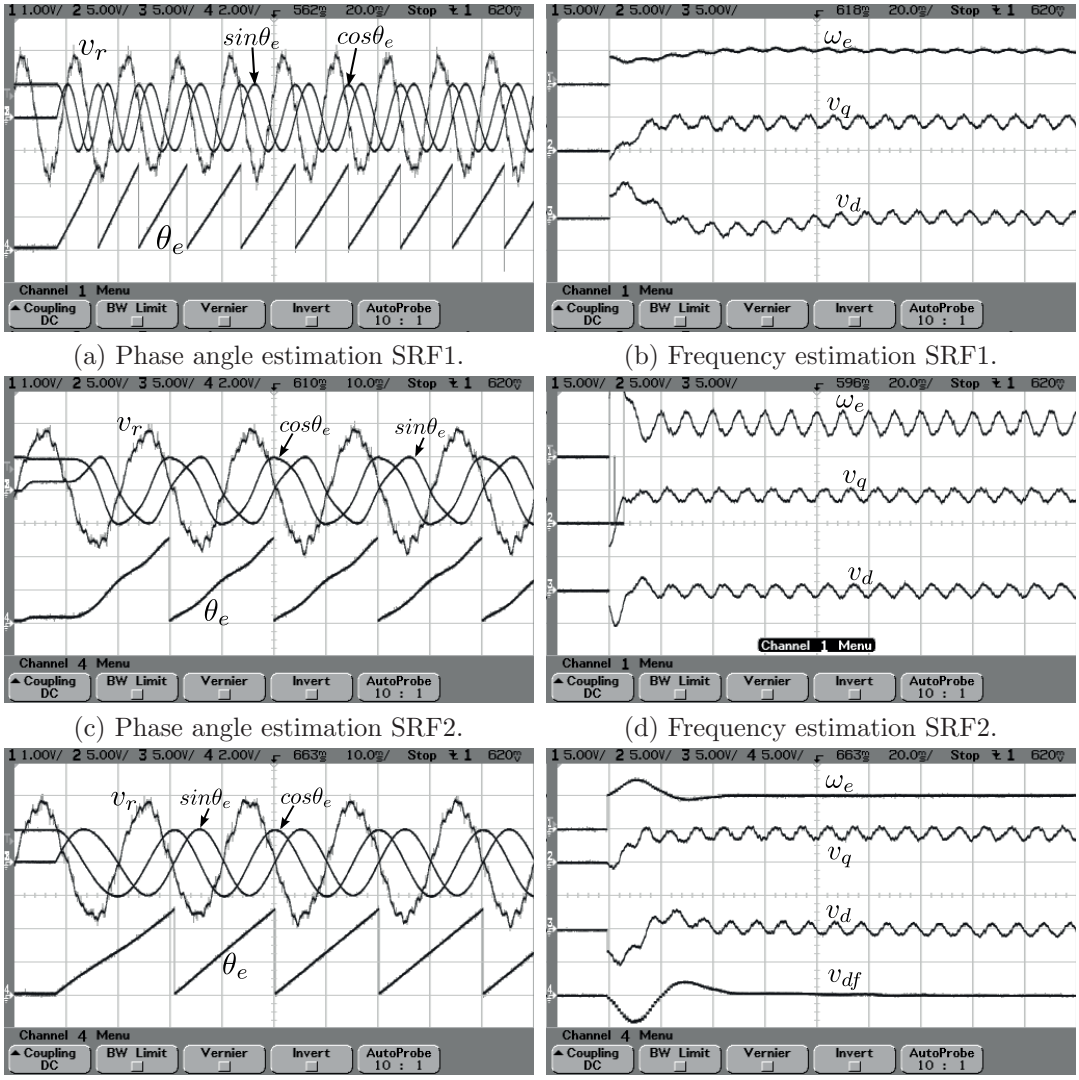
System	THD of unit vector		Settling time
	$cos\theta_e$	$sin\theta_e$	
SRF1	1.59%	1.52%	100 ms
SRF2	8.71%	8.64%	15 ms
MAF-SRF	0.89%	1.12%	50 ms

5.2. Unbalanced condition

To test the performance of the MAF-SRF-PLL and compare it with SRF1 and SRF2 PLL under unbalanced grid voltage condition, an unbalanced set of voltages was generated using previously described inverter hardware. The generated test voltage waveforms, as shown in Figure 10, have a 50% reduced voltage at R-phase and nominal voltages at other phases. Start-up performance under unbalanced condition for SRF1 PLL is shown in Figure 11(a). It can be observed that $sin\theta_e$ is in phase opposition to v_r at steady state, which is an indication of phase locked condition according to the conventions assumed. Frequency estimation, shown in Figure 11(b), by SRF1 PLL shows that the system has a settling time of about 100 ms. Also the presence of 100 Hz ripple due to unbalanced grid voltages can be observed from ω_e, v_d, and v_q shown in Figure 11(b). For the case of SRF2 PLL, shown in Figure 11(c) and Figure 11(d), though the response time is quicker the presence of 100 Hz ripple is more prominent due to its higher bandwidth. As for the MAF-SRF-PLL the response time is similar to that during balanced grid condition as can be observed from Figure 11(e) and Figure 11(f). However, the unit vector quality assessment shown in Table 4 shows that the unit vector THDs of SRF1 are close to 1.5% and of SRF2 are close to 8.6%, whereas for the MAF-SRF-PLL the THDs are close to 1.0%. This is the experimental verification of the ability of the MAF-SRF-PLL to produce better quality unit vectors under unbalanced grid condition compared to normal designs of SRF-PLL.

Table 5. Comparison of PLL performances under balanced grid voltage condition at 47.5 Hz.

System	THD of unit vector		Settling time
	$cos\theta_e$	$sin\theta_e$	
SRF1	0.84%	1.09%	100 ms
SRF2	1.19%	1.15%	10 ms
MAF-SRF	0.99%	0.97%	60 ms



(a) Phase angle estimation SRF1. (b) Frequency estimation SRF1.

(c) Phase angle estimation SRF2. (d) Frequency estimation SRF2.

(e) Phase angle estimation MAF-SRF. (f) Frequency estimation MAF-SRF.

Figure 11. Experimental results on phase tracking under unbalanced grid voltage condition.

5.3. Frequency variation

Grid frequency may vary from the nominal value because of load change and this is prominent in a weak grid such as a micro-grid. A FPGA based simulation was carried out first to test performance of the MAF-SRF-PLL during frequency variation. A separate FPGA board was used to create a three phase balanced variable frequency source for this purpose. As the supply frequency was given a step change from 50 Hz to 40 Hz the estimated frequency took about 60 ms, as seen in Figure 12, to settle to the newer value.

To test the performance of the MAF-SRF-PLL and compare it with SRF1 and SRF2 at a frequency other than the nominal value of 50 Hz, a $3-\Phi$ source was created with a frequency of 47.5 Hz. Under this condition the PLL structures were tested and their performance in terms of settling time and unit vector THD were evaluated. The results in Figure 13(a) and Figure 13(b) show the ability of SRF1 to lock to the grid phase of a 47.5 Hz system within 100 ms. Similar observations from Figure 13(c) and Figure 13(d) for SRF2 PLL

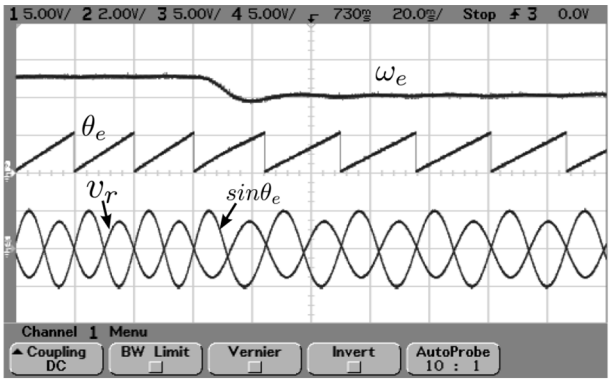


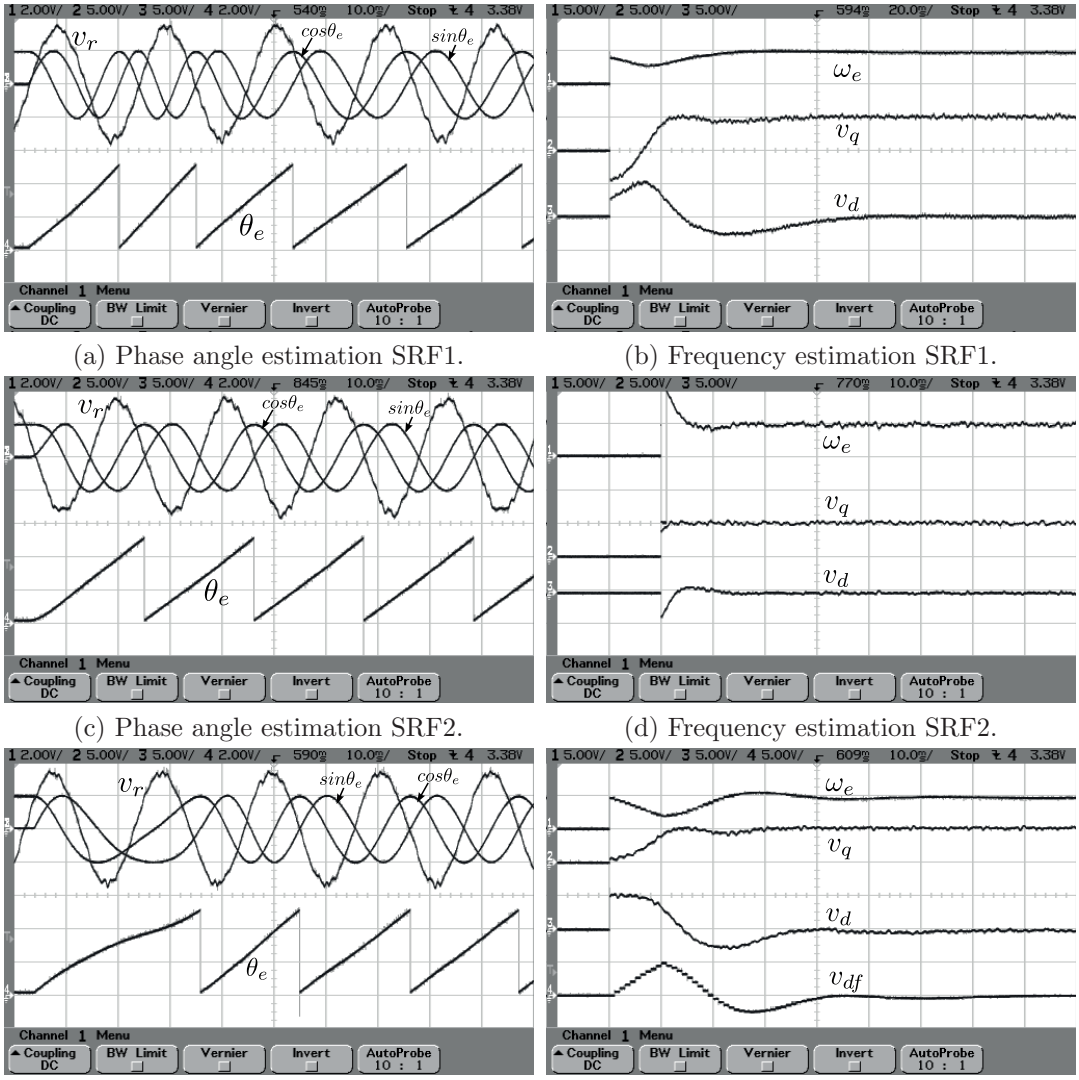
Figure 12. Frequency tracking for a step change of 10 Hz. Ch2 $\rightarrow \omega_e$: $5V \equiv 50Hz$.

show that it has a settling time of nearly 10 ms. From Figure 13(e) and Figure 13(f) it can be observed that the settling times of the MAF-SRF-PLL structure are nearly 60 ms. The analysis on unit vector quality in terms of THD, listed in Table 5, show that all the PLL structures produce similar quality of unit vectors with THD close to 1 % under balanced grid voltage condition at 47.5 Hz.

Hence it can be concluded that the MAF-SRF-PLL can work satisfactorily at a frequency other than the nominal supply frequency of 50 Hz.

5.4. Harmonics under balanced condition

The presence of harmonics can deteriorate the performance of a PLL. Therefore, a PLL should definitely be designed to extract positive sequence fundamental phase angle from a set of harmonic rich grid voltage. For a SRF-PLL because of transformation into the synchronously rotating reference frame odd harmonic voltages present in grid voltage would be seen as even harmonic voltage in d and q axes. Similarly, even harmonic voltages, if present in grid voltages, shows up as odd harmonic voltages in d and q-axis voltages. The MAF used here has a Nyquist frequency of 500 Hz and it is able to provide high attenuation at multiples of 100 Hz. Hence it would be able to provide high attenuation to a 300 Hz or 1884 rad/s component, which can possibly be generated because of 5^{th} and 7^{th} harmonic voltage present in the grid. To test the performance of the MAF-SRF-PLL and compare it with SRF_1 and SRF_2 under distorted voltage condition a three phase voltage source was created by the FPGA controlled inverter with a LCL filter. The fundamental component is kept at a RMS voltage equivalent to 230 V per phase. To create a distorted grid condition, 5^{th} and 7^{th} harmonic voltages were added to all the phases with RMS voltage of $\frac{1}{5}$th and $\frac{1}{7}$th of nominal fundamental frequency voltage respectively. The start-up transient of SRF1 PLL can be observed from Figure 14(a) and Figure 14(b). For SRF2 PLL the start transients are shown in Figure 14(c) and Figure 14(d). The start-up transients for the MAF-SRF-PLL under balanced distorted grid voltage condition are shown in Figure 14(e) and Figure 14(f). The dynamic performance in terms of settling time can be observed to remain the same as that during balanced undistorted grid voltage (Table-6). The unit vector quality assessment listed in Table 6 shows that the MAF-SRF-PLL is able to produce a unit vector with THD of less than 1%. In comparison, unit vectors produced by SRF1 and SRF2 have higher THD. Also it can be observed from Figure 14(a), Figure 14(c), and Figure 14(e) that the MAF-SRF-PLL can produce a cleaner estimation of frequency compared to SRF1 and SRF2 PLL. These observations prove the effectiveness of the MAF-SRF-PLL under distorted grid conditions.



(a) Phase angle estimation SRF1. (b) Frequency estimation SRF1.

(c) Phase angle estimation SRF2. (d) Frequency estimation SRF2.

(e) Phase angle estimation MAF-SRF. (f) Frequency estimation MAF-SRF.

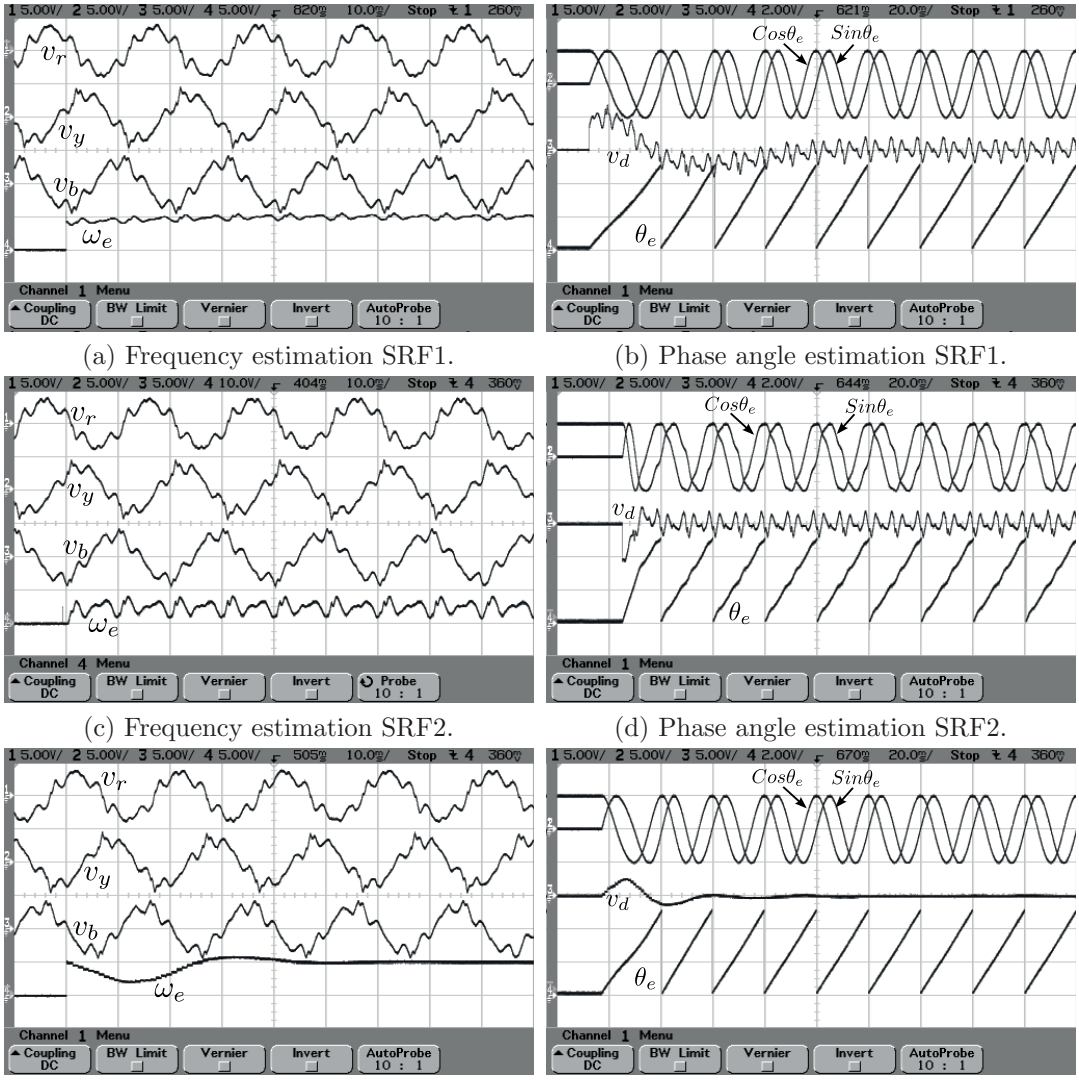
Figure 13. Phase tracking under balanced grid voltage condition at 47.5 Hz.

Table 6. Comparison of PLL performances under balanced distorted grid voltage condition.

System	THD of unit vector		Settling time
	$cos\theta_e$	$sin\theta_e$	
SRF1	1.28%	1.62%	100 ms
SRF2	6.27%	8.06%	10 ms
MAF-SRF	0.91%	0.89%	60 ms

5.5. Harmonics under unbalanced condition

The performance of the MAF-SRF-PLL was tested under unbalanced and distorted grid condition also. To create unbalance R-phase voltage v_r was reduced to 50% of its nominal value while other phase voltages were kept at nominal values. To create a distorted grid condition, 5^{th} and 7^{th} harmonic voltages were added to all



(a) Frequency estimation SRF1. (b) Phase angle estimation SRF1.

(c) Frequency estimation SRF2. (d) Phase angle estimation SRF2.

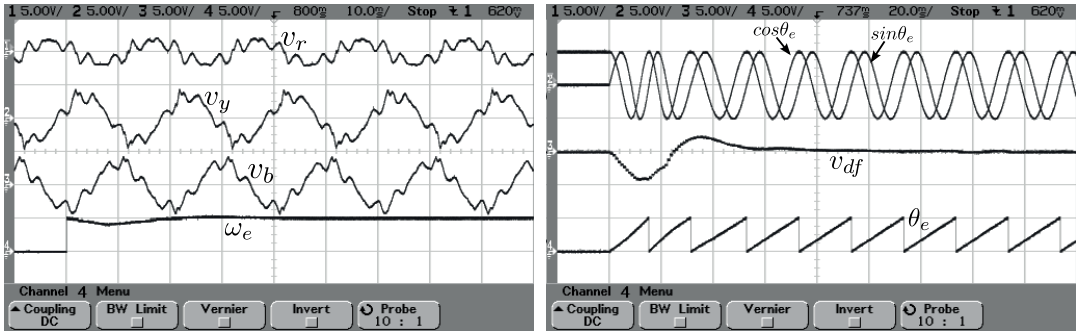
(e) Frequency estimation MAF-SRF. (f) Phase angle estimation MAF-SRF.

Figure 14. Phase tracking under distorted but balanced voltage condition.

Table 7. MAF-SRF-PLL performances under unbalanced distorted grid voltage condition.

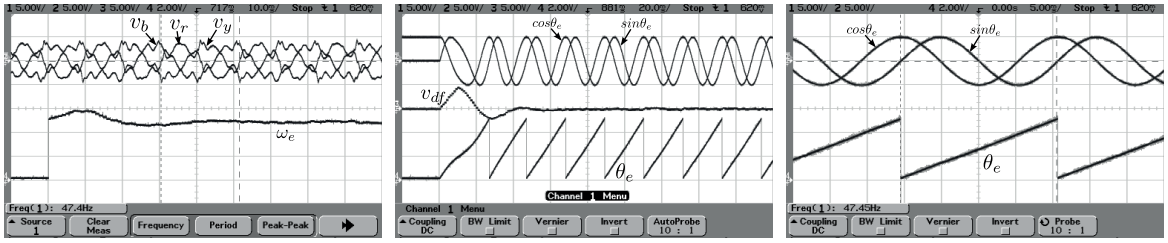
System	THD of unit vector		Settling time
	$cos\theta_e$	$sin\theta_e$	
MAF-SRF	1.19%	1.13%	50 ms

the phases with rms voltage of $\frac{1}{5}$th and $\frac{1}{7}$th of fundamental frequency nominal voltage, respectively. Figure 15 shows the capability of the MAF-SRF-PLL to extract frequency information and generated unit vectors locked to grid phase under the above described grid conditions. The THDs of unit vectors are tabulated in Table 7; they are 1.19% and 1.13%, which are close to 1%. This indicates the capability of the MAF-SRF-PLL to work under unbalanced and harmonic rich grid voltage condition.



(a) Frequency estimation. (b) Phase angle estimation.

Figure 15. Phase tracking under unbalanced and distorted grid voltage condition with MAF-SRF-PLL.



(a) Frequency estimation. (b) Phase angle estimation. (c) Unit vectors.

Figure 16. Phase tracking under balanced and distorted grid voltage condition with MAF-SRF-PLL at 47.5 Hz.

Table 8. MAF-SRF-PLL performances under balanced distorted grid voltage condition at 47.5 Hz.

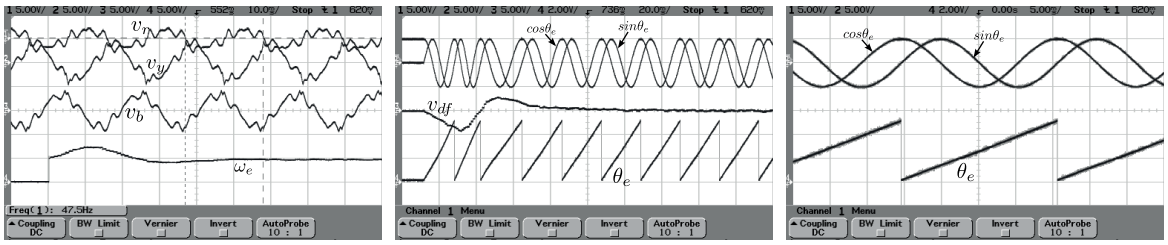
System	THD of unit vector		Settling time
	$cos\theta_e$	$sin\theta_e$	
MAF-SRF	1.13%	1.15%	50 ms

5.6. Harmonics at 47.5 Hz under balanced condition

Performances of the MAF-SRF-PLL were studied at 47.5 Hz under balanced condition with presence of harmonics at multiples of 47.5 Hz. Here also 5^{th} and 7^{th} harmonics considering 47.5 Hz as fundamental have been assumed to be present in the grid. The respective magnitudes of 5^{th} and 7^{th} harmonics are chosen as $\frac{1}{5}$ and $\frac{1}{7}$ of the fundamental component. The results are shown in Figure 16. Figure 16(a) and Figure 16(b) show the start-up transients with the MAF-SRF-PLL. The steady state results showing unit vectors and phase angle estimation at 47.5 Hz are shown in Figure 16(c). The THDs of generated unit vectors are found to be 1.13% and 1.15%. It can be concluded that the MAF-SRF-PLL is capable of generating good quality unit vectors and perform frequency estimation at the above described grid voltage situation.

5.7. Harmonics at 47.5 Hz under unbalanced condition

The performance of the MAF-SRF-PLL was studied in the presence of harmonics at 47.5 Hz under unbalanced condition. Here also the MAF-SRF-PLL is able to show satisfactory performance in terms of frequency estimation and good quality unit vector generation. These can be observed from the results shown in Figure 17 and listed in Table 9.



(a) Frequency estimation. (b) Phase angle estimation. (c) Unit vectors at steady state.

Figure 17. Phase tracking under unbalanced and distorted grid voltage condition at 47.5 Hz with MAF-SRF-PLL.

Table 9. MAF-SRF-PLL performances under unbalanced and distorted grid voltage condition at 47.5 Hz.

System	THD of unit vector		Settling time
	$cos\theta_e$	$sin\theta_e$	
MAF-SRF	1.13%	0.90%	50 ms

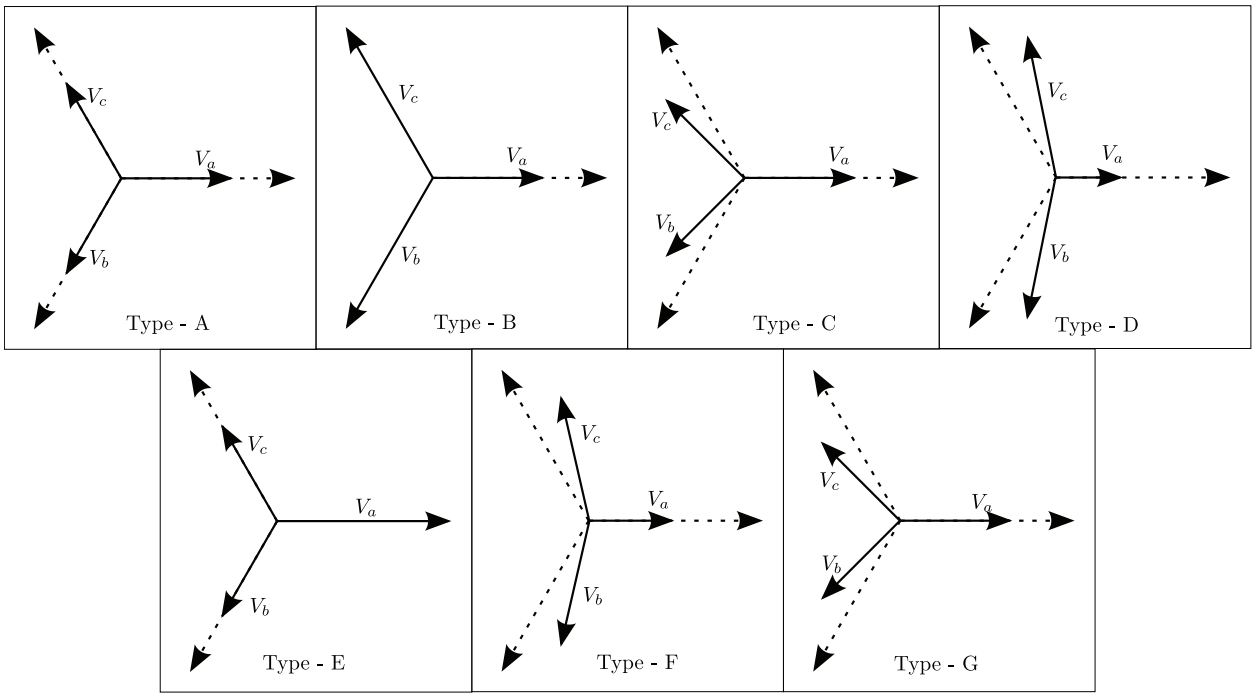


Figure 18. Phasor diagram representation of different types of voltage sag.

5.8. Voltage sag

Voltage sag can occur in a grid due to faults, load change, induction motor starting etc [22]. Generally they last a few cycles and, depending on the severity of the cause, a significant drop in voltage magnitude can be experienced by equipment connected to the grid. Typically a voltage sag creates an unbalanced set of grid voltage that can potentially cause disruption in operation or damage to the equipment connected. According to [22], voltage sag can be classified into seven different categories. The phasor diagram representation of different types of voltage sags is shown in Figure 18. It has been shown by researchers that the type of voltage sag seen at the terminals of a piece of equipment is also influenced by transformer connections. However, in this

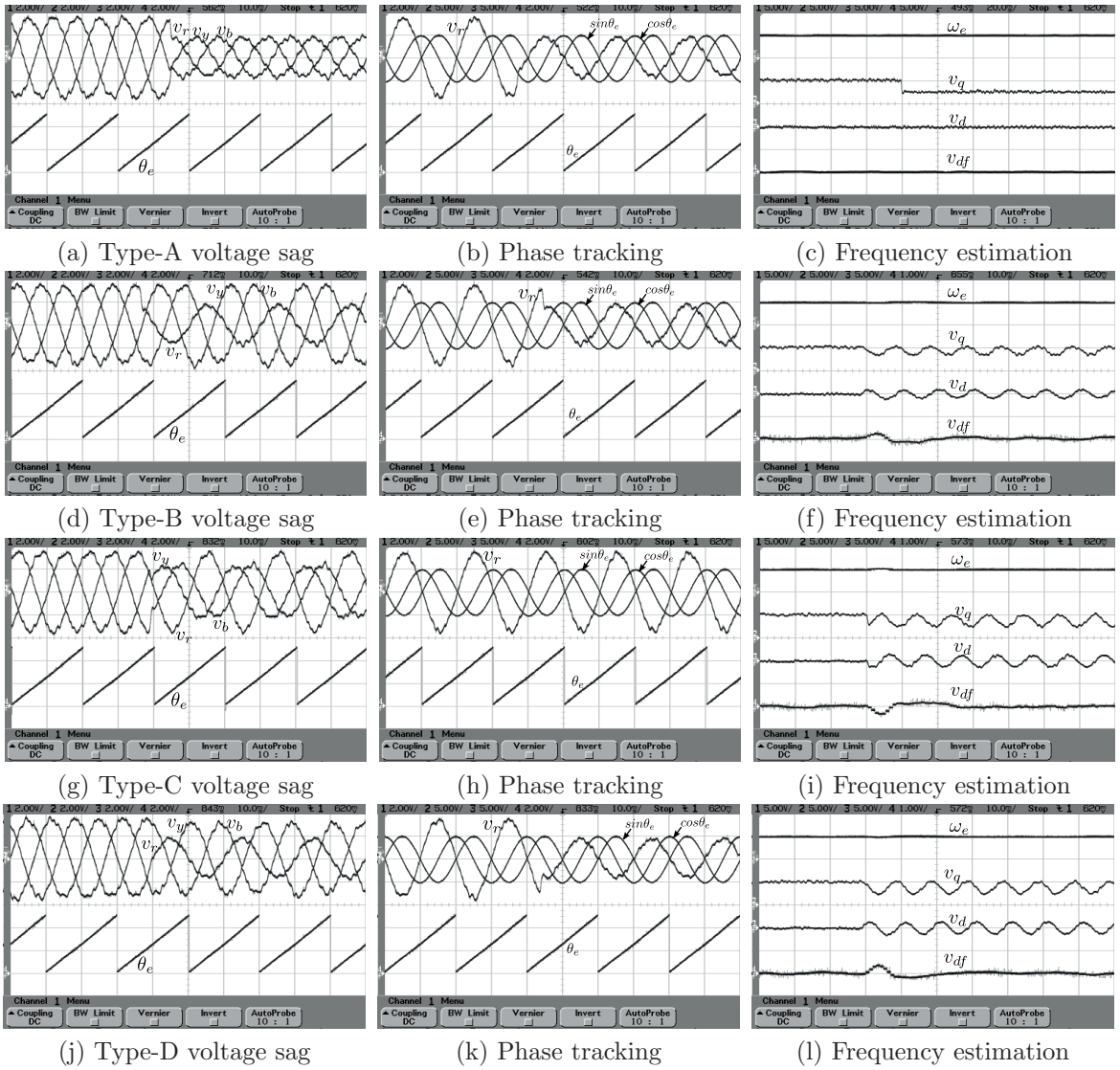


Figure 19. Performance of MAF-SRF-PLL during voltage sags. (a), (b) & (c): Type-A, (d), (e) & (f): Type-B, (g), (h) & (i): Type-C and (j), (k) & (l): Type-D voltage sag.

section the test results for MAF-SRF-PLL performance under seven different types of sag are discussed. Also the quality of the generated unit vector was assessed in terms of THD during voltage sag causing unbalance in the grid voltage. The performances of SRF1, SRF2, and MAF-SRF-PLL were also compared for generated unit vector quality.

The performance of the MAF-SRF-PLL for a Type-A voltage sag, which is basically a three phase balanced sag, is shown in Figure 19. From the responses shown in Figure 19(a), Figure 19(b), and Figure 19(c) it can be observed that there is no significant disturbance during or after the voltage sag in estimation of phase angle, frequency, and generation of unit vectors. As it is a balanced sag, estimations are fast and do not contain 100 Hz ripple in v_d and v_q.

For a Type-B voltage sag where one phase voltage is affected only the performance of the MAF-SRF-PLL is also shown in Figure 19. This has similarity with the earlier discussed performance considering the operation

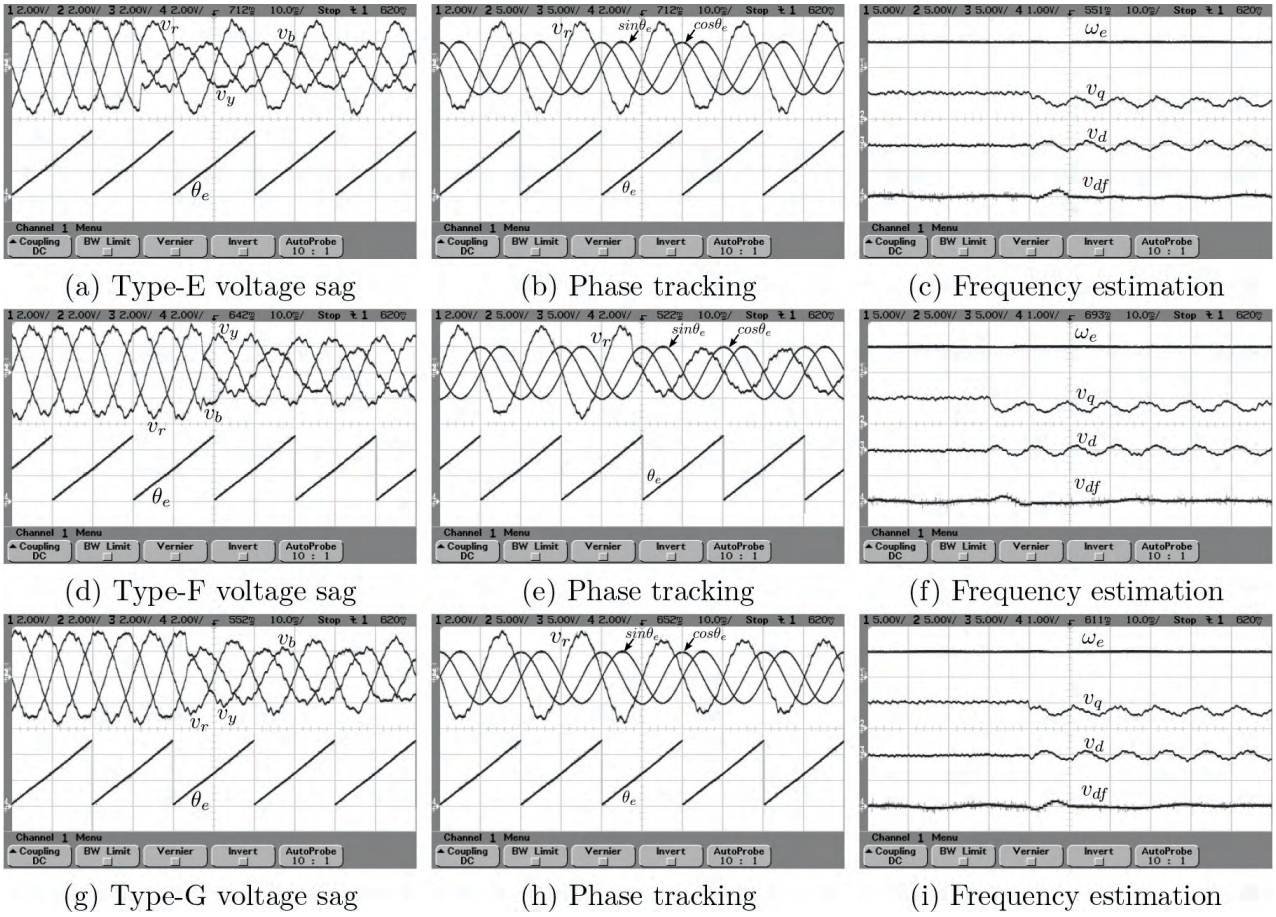


Figure 20. Performance of MAF-SRF-PLL during voltage sags. (a), (b) & (c): Type-E, (d), (e) & (f): Type-F and (g), (h) & (i): Type-G voltage sag.

of the MAF-SRF-PLL under an unbalanced grid. Here also the MAF-SRF-PLL shows its capability to produce quality unit vectors phase locked to positive sequence fundamental voltage of R phase, shown in Figure 19(e). The settling time can be observed to be within 60 ms from v_{df}.

Type-C voltage sag produces a situation where two phase voltages are affected in both magnitude and phase angle and the other phase voltage remains unaffected. The results for this case are shown in Figure 19(g), Figure 19(h), and Figure 19(i). The settling time can be observed to be within 60 ms from v_{df}. It can readily be observed that the MAF-SRF-PLL is capable of working under this condition also.

For Type-D voltage sag all three phase voltages are affected differently, creating an unbalanced sag. The performance of the MAF-SRF-PLL under this condition is also shown in Figure 19. Its ability to track positive sequence fundamental phase angles and generate quality unit vectors can be observed from Figure 19(j) and Figure 19(k). The settling time is also within 60 ms, which can be observed from Figure 19(l).

In similar experiments Type-E, Type-F, and Type-G voltage sags were generated by the hardware setup. The MAF-SRF-PLL was tested under these conditions also and the results are shown in Figure 20. All the results confirm that the MAF-SRF-PLL structure is capable of producing unit vectors phase locked to fundamental positive sequences within 60 ms from the time of starting of a voltage sag.

A comparison of quality assessment of generated unit vectors amongst SRF1, SRF2, and MAF-SRF-PLL

Table 10. Comparison on unit vector THD between SRF1, SRF2, and MAF-SRF-PLL for different types of voltage sag.

Type of sag	THD of unit vector in %					
	SRF1		SRF2		MAF-SRF	
	$cos\theta_e$	$sin\theta_e$	$cos\theta_e$	$sin\theta_e$	$cos\theta_e$	$sin\theta_e$
Type-A	1.14	0.92	0.96	1.38	1.02	1.0
Type-B	1.41	1.58	8.41	8.33	1.21	0.98
Type-C	1.85	1.77	13.1	11.7	1.07	0.97
Type-D	1.99	1.98	12.5	13.2	0.90	0.90
Type-E	1.47	1.51	8.68	8.09	0.87	0.84
Type-F	1.48	1.55	8.97	9.09	0.95	1.01
Type-G	1.43	1.44	8.42	8.11	0.80	0.94

is tabulated in Table 10. From these data it can be observed that the MAF-SRF-PLL can generate a superior quality unit vector in terms of THD under all seven types of sag conditions. Only under balanced sag situation, that is for Type-A sag, all three PLL designs produce nearly the same quality unit vector with THD of nearly 1%. SRF2 PLL produces unit vectors with high THD for all the remaining cases, which is not desirable. SRF1 design produces unit vectors with THD of slightly higher value for a few cases, which could be tolerable. For Type-C and Type-D sag conditions SRF1 design generates unit vectors with THD with nearly 2%, which is also on the higher side. However, the MAF-SRF-PLL is capable of producing unit vectors with THD below 1% for nearly all the cases.

Therefore, it can be concluded that the MAF-SRF-PLL has superior phase tracking ability under different types of voltage sag considering quality of unit vectors and settling time.

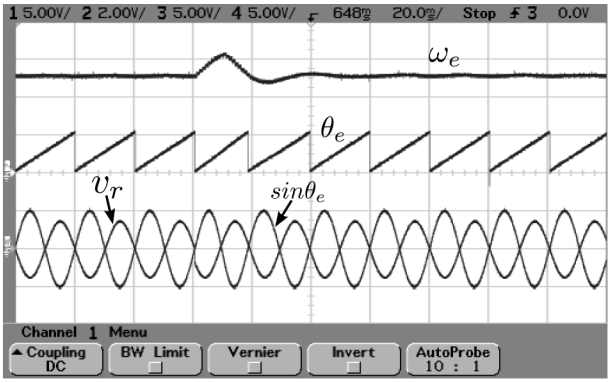
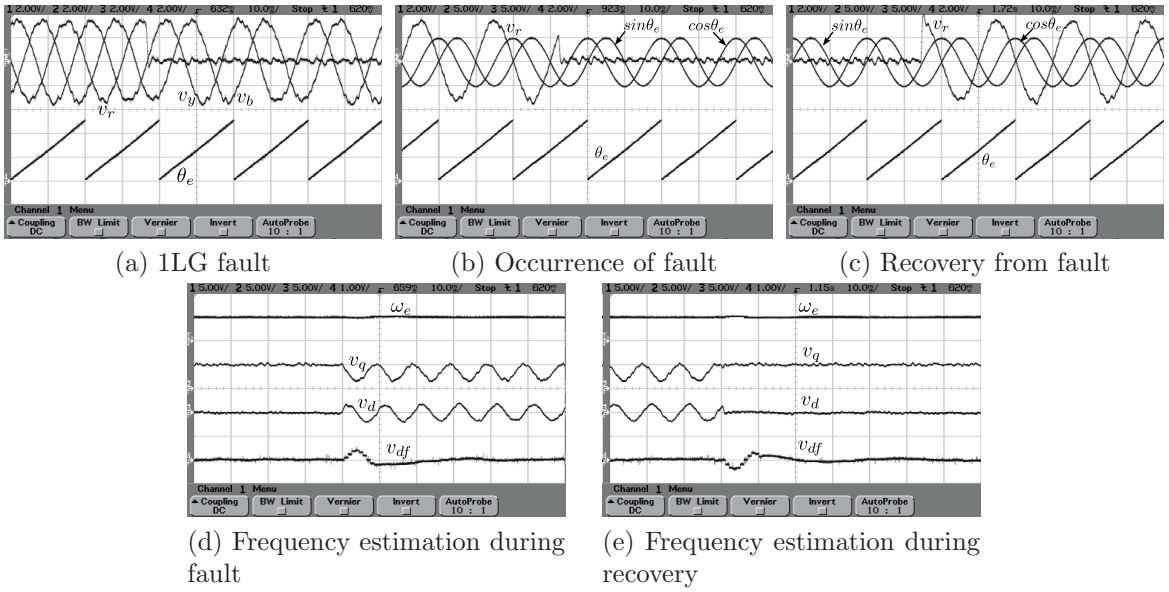


Figure 21. Frequency tracking during a phase jump of 30°. Ch2$\rightarrow \omega_e$: $5V \equiv 50Hz$.

5.9. Phase jump

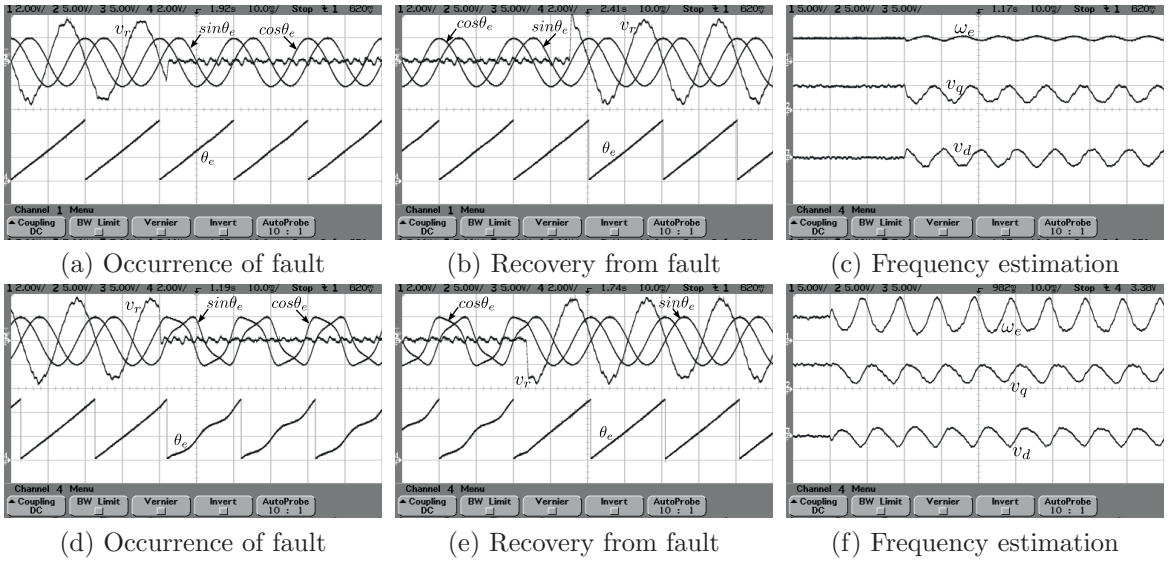
Sudden phase change in load terminal voltage may occur if a large load is withdrawn from the supply system or due to faults in the grid. To observe the performance of the MAF-SRF-PLL under this situation again a FPGA based simulation was carried out. Application of a step change of 30° in the system phase resulted in a disturbance in frequency estimation. The estimated frequency as observed from Figure 21 shows a settling time of nearly 60 ms.



(a) 1LG fault (b) Occurrence of fault (c) Recovery from fault

(d) Frequency estimation during fault (e) Frequency estimation during recovery

Figure 22. Performance of MAF-SRF-PLL during single phase line to ground fault.



(a) Occurrence of fault (b) Recovery from fault (c) Frequency estimation

(d) Occurrence of fault (e) Recovery from fault (f) Frequency estimation

Figure 23. Performance of SRF1 and SRF2 PLL during single phase line to ground (1LG) fault. (a), (b) & (c) SRF1 PLL. (d), (e) & (f) SRF2 PLL.

5.10. Single phase LG fault

During a single phase LG fault, voltage of the faulty phase may become almost zero. The voltage is restored after the fault is cleared. During the experiment R-phase voltage was made zero as shown in Figure 22(a) to emulate a single phase LG fault situation. Figure 22(b) shows generation of $sin\theta_e$ and $cos\theta_e$ and phase angle estimation during the occurrence of a fault. Generation of unit vectors during recovery from a fault is shown in Figure 22(c). Both Figure 22(b) and Figure 22(c) indicate that the PLL is able to track grid phase angle at single phase LG fault condition. It can also be observed that the filtered output of d-axis voltage, shown in

Figure 22(d), reaches zero within 50 ms. The estimated frequency also settles within 50 ms. Accurate tracking of grid phase angle under fault condition can enhance fault ride through capability of a power converter. The performance of SRF1 and SRF2 PLL is shown in Figure 23. A visual inspection shows that the estimated frequency has 100 Hz ripple as expected, shown in Figure 23(c) and Figure 23(f). The estimations of phase angle and unit vectors are shown in Figure 23(b) and Figure 23(e), respectively, for SRF1 and SRF2 PLL. The effect of severe unbalance can prominently be observed from the phase angle estimation and generated unit vectors by SRF2 PLL from Figure 23(d) and Figure 23(e). From the quality assessment of unit vectors in terms of THD, tabulated in Table 11, the superior performance of the MAF-SRF-PLL structure compared to SRF1 and SRF2 designs can be observed under 1LG fault situation.

Therefore, it can be concluded from the above sets of experiments that a $3-\Phi$ MAF-SRF-PLL is capable of producing good quality unit vectors at different nonideal grid conditions with a reasonably fast response time compared to standard designs of SRF-PLL.

Table 11. Comparison of PLL performances under 1LG fault condition.

System	THD of unit vector		Settling time
	$cos\theta_e$	$sin\theta_e$	
SRF1	2.44%	2.38%	–
SRF2	16.4%	17.7%	–
MAF-SRF	1.02%	0.96%	50 ms

6. Conclusion

In this work a performance evaluation of a MAF-SRF-PLL was carried out in terms of unit vector THD and response time. The MAF-SRF-PLL structure is an improved version of the SRF-PLL structure capable of providing quality unit vector and an assessment of grid phase and frequency. In this work the evaluation was carried out by creating several nonideal grid conditions such as unbalance, voltage sag, frequency variation, harmonic distortion, and fault condition. The experimental results clearly show the superiority of the MAF-SRF-PLL under all the conditions. They also show the limitation of a fast SRF-PLL under nonideal grid condition and the use of a slow SRF-PLL for a few limited cases considering their abilities to generate good quality unit vectors.

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