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Model-reference sliding mode control of a three-phase four-leg voltage source inverter for stand-alone distributed generation systems

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Abstract: This paper proposes a discrete-time model-reference sliding mode control of three-phase four-leg voltage source inverters for stand-alone distributed generation systems. Three-phase four-leg voltage source inverters (VSIs) are used in a broad area. A discrete-time model-reference sliding mode controller, having superior advantages such as insensitivity to external disturbances, system parameter variations, and modeling errors, is applied to control the output voltage of three-phase four-leg VSIs. As a new study, the discrete-time model-reference sliding mode control with a supplemented output feedback integral controller is proposed so that the controlled output voltages of the VSI tracks the input reference signal. The controller is designed using the augmented discrete-time error dynamics presented in this paper and is applied to control the output voltage control of a three-phase four-leg based uninterruptable power supply. It is shown that the output voltage of the VSI controlled by the proposed method is accurately regulated for various load conditions such as linear balanced/unbalanced, nonlinear balanced/unbalanced, and instantaneous load changes. The robustness of the proposed method against variations by 20%–50% in R, L, and C filter parameters and 5 different cases are showed.

Key words: Voltage source inverter, sliding mode controller, four-leg inverter, model reference, distributed generation systems, stand-alone

1. Introduction

Renewable energy sources (such as wind turbines, photovoltaic arrays, biomass, and fuel cells) are increasingly preferred in distributed generation systems (DGSs) in order to reduce global warming gas emissions [1]. In recent years, since the grid connection of rural villages or remote islands has higher costs than the stand-alone operations, stand-alone DGSs applications for those cases are gaining more attention [1–7]. The inverter of the DGS can be considered as an uninterruptible power supply (UPS) for its local loads in stand-alone applications [1]. Stand-alone DGS or UPS discrete-time control methods have been a popular research area in the last decades. Although in rural villages a stand-alone application phase-neutral load connection is also important, a single phase load cannot be connected according to the studies given in [1,4–6], because the inverter topologies given in those studies are three-phase and three-wire. The inverter topology of this study is four-leg and four-wire, which provides a single phase load connection in stand-alone rural village applications.

In many of the industrial and commercial electrical power systems, power is distributed through a three-phase four-wire system. In this type of system, when the three-phase load is unbalanced and/or single phase

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loads are unequally configured, a zero-sequence current appears. If the compensation of the neutral current is inadequate, it can damage the neutral cable and the transformer and reduce energy efficiency [8–10].

Three-phase voltage source inverters (VSIs), used in many applications such as active power filters [9,11], distributed generation systems [8], and PWM rectifiers [12], have two main ways of providing a neutral connection for three-phase four-wire systems [8,10,13]: 1) a relatively simple approach of using two capacitors to split the DC link and tie the neutral point to the midpoint of the two capacitors [14,15]; and 2) using a four-leg inverter topology and tying the neutral point to the midpoint of the fourth leg [13,16,17].

In the literature, there are many valuable studies comparing split-center capacitors and four-leg VSIs [12,18]. The former suffer from an insufficient utilization of the DC link voltage due to the neutral currents caused by unbalanced loads and need large DC link capacitors to maintain an acceptable voltage ripple across the DC link [8,18]. The four-leg topology presents advantages such as better DC link utilization, smaller DC link capacitors, a more precise control of the neutral current, and flexibility in control over the split capacitor topology [9,12]. Although the fourth-leg topology increases the complexity of the phase voltage control, it gives better controllability because of the increase in the number of switches [19].

The studies found in the literature on the three-phase four-leg VSIs can be classified into two groups when the main issues are considered: 1) modulation method studies [12,14,20,21] and 2) control method studies [8,22–25]. In this study, a new simplified mathematical model and a new control approach is offered for three-phase four-leg VSIs. Therefore, this study can be considered in the scope of the second group.

A pole assignment-based method was offered to regulate the output voltage of the three-phase four-leg inverter [23]. In [24], the current control of a grid-connected four-leg inverter was carried out by using a predictive controller. A sliding mode controller (SMC) was applied to three-phase four-leg shunt active power filters to compensate the effects of the distorted nonlinear loads [25]. In [8], using two different synchronous reference frames (positive and negative), a three-phase output voltage and current decomposed into positive, negative, and homopolar sequence components, and then a PI controller was designed for each component. In [22], the three-phase currents of the three-phase four-leg VSI were regulated independently via a PI controller. In [14], only an open-loop control was considered in simulation and experimental studies. A Fourier decomposition-based selective harmonic elimination method was offered to deal with unbalanced loads in three-phase four-leg inverters in the open-loop control mode in [26]. A minimally switched control algorithm was proposed in [9] to compensate zero-sequence currents caused by unbalanced and nonlinear loads in three-phase four-leg VSIs.

As can be seen from the literature review [8,22–25], many different control methods, including modern control techniques, were used to control the three-phase four-leg inverter. However, in most of the studies, the conventional PI (proportional + integral) controller was preferred [8,22]. In a number of studies only an open-loop control is examined and a closed-loop control is not considered [14,16,26].

2. Modeling the three-phase four-leg VSI

In this study, a robust discrete-time model-reference sliding mode controller (RD-MRSMC) is applied to control the output voltage of a three-phase four-leg based UPS for the stand-alone DGS system shown in Figure 1 with a dotted line.

The objective of the model-reference control is to develop a control algorithm that forces the plant to follow the dynamics of a desired model, also called a reference model. The controller should ensure that the error between the reference model and the plant states is zero when time tends to infinity, i.e. $e(t) = 0$. Thus,

the plant output follows the reference model output accurately. Although the model-reference system does not need to be practically feasible, it should be, as much as possible, similar to the plant [27,28]. In this study, the discrete-time model-reference sliding mode control with a supplemented output feedback integral controller is proposed as a new approach. The controller is designed using the augmented discrete-time error dynamics presented in this paper. The main advantages of the SMC are that when the sliding mode is ensured, then the system is insensitive to external disturbances, system parameter variations, and modeling errors, and a relative simplicity of implementation is achieved. These properties of the SMC make it a popular and suitable method for the design of a robust controller [28–30].

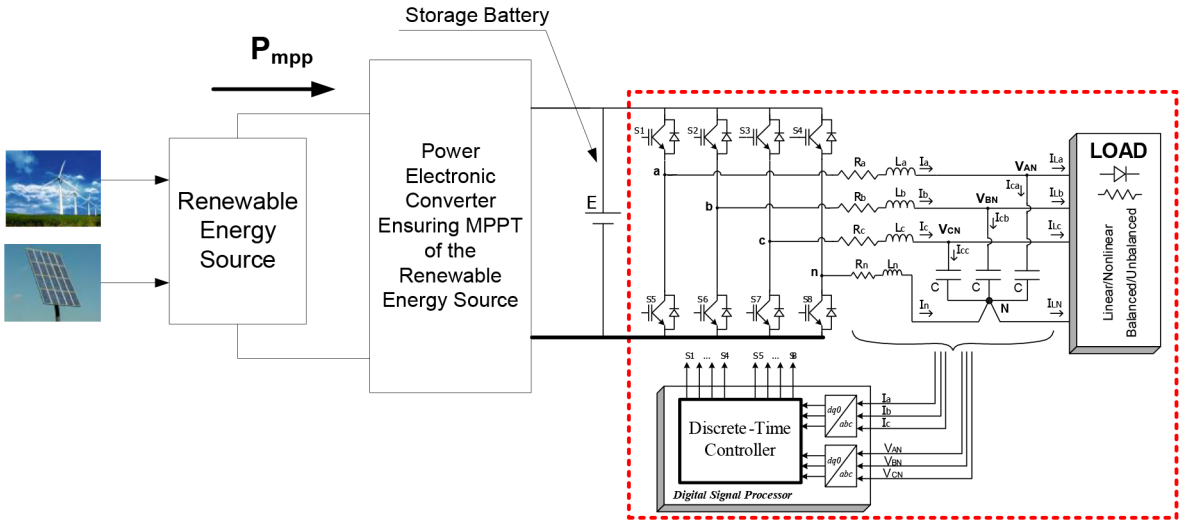

Figure 1. Simplified block diagram of the stand-alone DGS system.

A three-phase four-leg VSI will be modeled and controlled because of the focus of this paper. The mathematical model of the three-phase four-leg VSI with a filter, shown in Figure 2, in the *dq0* coordinate is obtained as below.

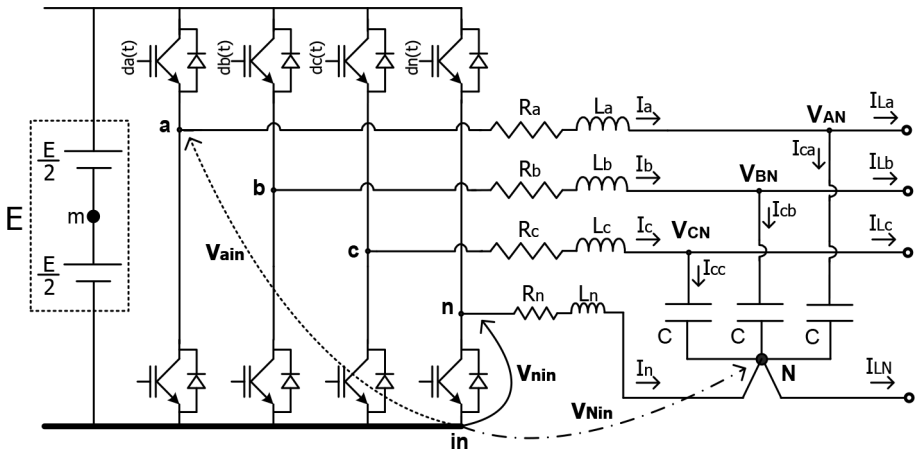

Figure 2. The basic topology of the three-phase four-leg VSI connected to the load through a filter.

From Figure 2, the voltage equations for the three phases (a,b,c) can be written, using the Kirchhoff voltage laws (KVLs), as:

$$V_{jin}(t) = L_j \frac{di_j(t)}{dt} + R_j i_j(t) + V_{JN}(t) + V_{Nin}(t), \tag{1}$$

where $j \epsilon \{a,b,c\}$ and $J \epsilon \{A,B,C\}$.

Similarly, the voltage equation of the neutral-leg (n) is:

$$V_{nin}(t) = L_n \frac{di_n(t)}{dt} + R_n i_n(t) + V_{Nin}(t) \tag{2}$$

The following equalities can easily be obtained from Figure 2:

$$V_{im}(t) = \frac{E}{2} d_i(t), \tag{3}$$

$$V_{jn}(t) = V_{jm}(t) - V_{nm}(t), \tag{4}$$

$$V_{jn}(t) = \frac{E}{2} \{d_j(t) - d_n(t)\}, \tag{5}$$

$$V_{nn}(t) = \frac{E}{2} d_n(t), \tag{6}$$

where $i \epsilon \{a,b,c,n\}$ and $d_i(t)$ is the modulation indices taking values in $-1 < d_i(t) < 1$, and m is the midpoint of the DC link voltage E as shown in Figure 2.

Eqs. (7) and (8) are valid in the case of symmetric output voltage and unbalanced load conditions.

$$V_{AN}(t) + V_{BN}(t) + V_{CN}(t) = 0 \tag{7}$$

$$i_n(t) = -(i_a(t) + i_b(t) + i_c(t)) \tag{8}$$

Expressions describing the dynamics of three-phase and neutral currents in an *abc* coordinate system in continuous-time state space equations are as in Eq. (9) if $L_j = L_n = L$ and $R_j = R_n = R$ are chosen, and the intermediate steps come out in Eqs. (1) through (8).

$$\frac{d}{dt}\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \\ i_n(t) \end{bmatrix} = -\frac{R}{L}\begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix}\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \\ i_n(t) \end{bmatrix} + E\begin{bmatrix} \frac{3}{8L} & \frac{-1}{8L} & \frac{-1}{8L} & \frac{-1}{8L} \\ \frac{-1}{8L} & \frac{3}{8L} & \frac{-1}{8L} & \frac{-1}{8L} \\ \frac{-1}{8L} & \frac{-1}{8L} & \frac{3}{8L} & \frac{-1}{8L} \\ 0 & 0 & 0 & \frac{-1}{2L} \end{bmatrix}\begin{bmatrix} d_a(t) \\ d_b(t) \\ d_c(t) \\ d_n(t) \end{bmatrix} - \begin{bmatrix} \frac{3}{4L} & \frac{-1}{4L} & \frac{-1}{4L} \\ \frac{-1}{4L} & \frac{3}{4L} & \frac{-1}{4L} \\ \frac{-1}{4L} & \frac{-1}{4L} & \frac{3}{4L} \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} V_{AN}(t) \\ V_{BN}(t) \\ V_{CN}(t) \end{bmatrix} \tag{9}$$

In the above model, given in an *abc* coordinate system for four-leg currents, $i_i(t)$ can be transformed into a *dq0* plane by using the 4×4 transformation matrix [31] T_r defined in Eq. (10). The result is given in Eq. (11).

$$T_r = \sqrt{\frac{2}{3}}\begin{bmatrix} cos(\theta) & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) & 0 \\ -sin(\theta) & -sin(\theta - \frac{2\pi}{3}) & -sin(\theta + \frac{2\pi}{3}) & 0 \\ \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & \frac{1}{2\sqrt{2}} & -\frac{3}{2\sqrt{2}} \\ \frac{3}{2\sqrt{2}} & \frac{3}{2\sqrt{2}} & \frac{3}{2\sqrt{2}} & \frac{3}{2\sqrt{2}} \end{bmatrix} \tag{10}$$

$$\frac{d}{dt}\begin{bmatrix} i_q(t) \\ i_d(t) \\ i_0(t) \\ i_{nz}(t) \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & w & 0 & 0 \\ -w & -\frac{R}{L} & 0 & 0 \\ 0 & 0 & -\frac{R}{L} & 0 \\ 0 & 0 & 0 & -\frac{R}{L} \end{bmatrix}\begin{bmatrix} i_q(t) \\ i_d(t) \\ i_0(t) \\ i_{nz}(t) \end{bmatrix} + \frac{E}{2L}\begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & -\frac{1}{4} \\ 0 & 0 & 0 & \frac{1}{4} \end{bmatrix}\begin{bmatrix} d_q(t) \\ d_d(t) \\ d_0(t) \\ d_{nz}(t) \end{bmatrix} + \frac{1}{L}\begin{bmatrix} -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & -\frac{1}{16} & -\frac{1}{16} \\ 0 & 0 & -\frac{3}{16} & -\frac{3}{16} \end{bmatrix}\begin{bmatrix} V_q(t) \\ V_d(t) \\ V_0(t) \\ V_{nz}(t) \end{bmatrix} \tag{11}$$

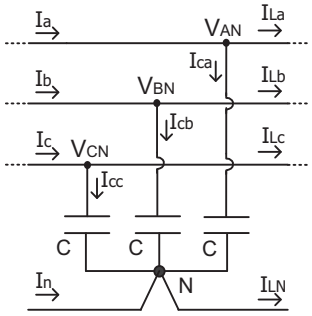

Figure 3. The circuit part containing output voltages taken from Figure 2.

By the same token, from Figure 3, the *dq0* model for VSI output voltages $V_{AN}\,V_{BN}\,V_{CN}$ is obtained using the KVLs and Kirchhoff current law.

$$i_j(t) = i_{cj}(t) - i_{Lj}(t) \tag{12}$$

$$i_{La}(t) + i_{Lb}(t) + i_{Lc}(t) + i_{LN}(t) = 0 \tag{13}$$

$$V_{AN}(t) + V_{BN}(t) + V_{CN}(t) = 0 \text{ and } V_{NN}(t) = 0 \tag{14}$$

$$C\frac{dV_{JN}(t)}{dt} = i_j(t) - i_{Lj}(t) \tag{15}$$

$$\frac{d}{dt}\begin{bmatrix} V_q(t) \\ V_d(t) \\ V_0(t) \end{bmatrix} = \begin{bmatrix} 0 & w & 0 \\ -w & 0 & 0 \\ 0 & 0 & \frac{-1}{4C} \end{bmatrix}\begin{bmatrix} V_q(t) \\ V_d(t) \\ V_0(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{C} & 0 & 0 \\ 0 & \frac{1}{C} & 0 \\ 0 & 0 & \frac{1}{4C} \end{bmatrix}\begin{bmatrix} i_q(t) \\ i_d(t) \\ i_0(t) \end{bmatrix} - \begin{bmatrix} \frac{1}{C} & 0 & 0 \\ 0 & \frac{1}{C} & 0 \\ 0 & 0 & \frac{1}{4C} \end{bmatrix}\begin{bmatrix} i_{Lq}(t) \\ i_{Ld}(t) \\ i_{L0}(t) \end{bmatrix} \tag{16}$$

As can be seen from the *dq0* models of the current and voltage given in Eqs. (11) and (16) respectively, the d and q axis circuits are coupled through wi_q and wi_d, wV_q and wV_d terms, while the axis circuit is completely decoupled from the d and q axis circuits. In order to simplify the controller design procedure, this coupling effect is neglected and a simplified model is obtained for the *dq0* coordinate as follows:

$$\begin{bmatrix} \frac{di_k(t)}{dt} \\ \frac{dV_k(t)}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}\begin{bmatrix} i_k(t) \\ V_k(t) \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_k(t) + \begin{bmatrix} 0 \\ -\frac{1}{C} \end{bmatrix} I_0(t), \tag{17}$$

where $V_k(t) = \frac{E}{2}d_k(t)$ and $k \epsilon \{d, q, 0\}$

2.1. Discretization of a continuous time model

The state-space model of the three-phase four-leg VSI given in Eq. (17) is in continuous time. In this study, however, a discrete-time controller is proposed for a three-phase four-leg VSI control. For this reason, the continuous time model of the plant given in Eq. (17) must be discretized. The discretization of a continuous time state-space model with a zero-order hold is described below.

Recall that the continuous time state-space model of a linear time-invariant system is:

$$\dot{x}(t) = Ax(t) + Bu(t) \tag{18}$$

where $x(t)\,\epsilon\,R^n$ is the state vector, $u(t)\,\epsilon\,R^m$ is the input vector, A is the $n \times n$ state matrix, and B is the $n \times m$ input matrix. Its discrete-time model can be obtained as [32]:

$$x[k+1] = Gx[k] + Hu[k], \tag{19}$$

where

$$G = \phi(t)|_{t=T}, \tag{20a}$$

where $\varphi(T)$ is a discrete-time state transition matrix and is calculated as:

$$\phi(T) \triangleq e^{AT}, \tag{20b}$$

$$H = \Gamma B \text{ and } \Gamma \triangleq \int_0^T e^{A\tau} d\tau, \tag{21}$$

T : sampling period.

3. Design procedure of the proposed controller

The proposed RD-MRSMC based controller consists of two parts: the classical control part, D-MRSMC, and the proposed discrete-time augmented controller part. The design procedure for the two parts of the controller is explained below.

Consider a discrete-time linear time invariant plant (Eq. (22)) and a corresponding referenced model (Eq. (23)) that are given respectively as:

$$x[k+1] = Gx[k] + Hu[k], \tag{22}$$

$$x_m[k+1] = G_m x_m[k] + H_m r[k], \tag{23}$$

where $x \in R^n$, $x_m \in R^n$ are the state vectors of the system and the reference model respectively. $u \in R$ is the control input, $r \in R$ is the reference input, and G, H, G_m and H_m are compatibly dimensioned matrices. It is assumed that the pair (GH) is controllable and the reference model in Eq. (23) is stable.

When the conditions given in Eq. (24) are fulfilled, the system given in Eq. (22) can track the reference model in Eq. (23) [28,29].

$$G - G_m = H\Gamma_g \text{ and } H_m = H\Gamma_h, \tag{24}$$

where $\Gamma_g \in R^{1xn}$ and $\Gamma_h \in R$.

The tracking error between the system and the reference model, required to be zero when time tends to infinity, can be determined from Eqs. (22) and (23) as:

$$e\left[k\right] = x\left[k\right] - x_m\left[k\right], \tag{25}$$

and the dynamics of the tracking error are as follows:

$$e\left[k+1\right] = x\left[k+1\right] - x_m\left[k+1\right]. \tag{26}$$

When the right-hand side of Eq. (26) is rewritten using Eqs. (22) and (23), and adding and subtracting terms $Gx_m\left[k\right]$ it yields:

$$e\left[k+1\right] = \left\{Gx\left[k\right] + Hu\left[k\right]\right\} - \left\{G_m x_m\left[k\right] + H_m r\left[k\right]\right\} + Gx_m\left[k\right] - Gx_m\left[k\right]$$

$$e\left[k+1\right] = e\left[k\right] + \left(G - G_m\right)x_m\left[k\right] + Hu\left[k\right] - H_m r\left[k\right]. \tag{27}$$

Finally, using the conditions specified in Eq. (24), the dynamics of the tracking error can be rearranged as follows;

$$e\left[k+1\right] = Ge\left[k\right] + H\Gamma_g x_m\left[k\right] + Hu\left[k\right] - H\Gamma_h r\left[k\right],$$

$$e\left[k+1\right] = Ge\left[k\right] + H\left\{\Gamma_g x_m\left[k\right] + u\left[k\right] - \Gamma_h r\left[k\right]\right\}. \tag{28}$$

The design process of the SMC consists of two phases [28–30]: 1) design of a switching function $\sigma\left[k\right]$ such that the reduced-order dynamics of the system in the sliding mode, where $\sigma = \dot{\sigma} = 0$, are stable; and 2) derivation of a control law $u\left[k\right]$ that guarantees that the system's trajectory moves on to the sliding mode in a finite time and remains on it thereafter.

In this study, the SMC will be designed using a regular form-based approach defined in [28–30]. Therefore, the system error model given in Eq. (28) is transformed into the regular form using a nonsingular transformation matrix $T_r \in R^{nxn}$.

By using the coordinate transformation,

$$e\left[k\right] \leftrightarrow T_r e\left[k\right] = \begin{bmatrix} e_1[k] \\ e_2[k] \end{bmatrix}, \tag{29}$$

where $e_1 \in R^{n-1}$ and $e_2 \in R^1$, the model given in Eq. (28) can be written in regular form as:

$$e_1\left[k+1\right] = G_{11}e_1\left[k\right] + G_{12}e_2\left[k\right], \tag{30}$$

$$e_2\left[k+1\right] = G_{21}e_1\left[k\right] + G_{22}e_2\left[k\right] + H_2\left\{\Gamma_g x_m\left[k\right] + u\left[k\right] - \Gamma_h r\left[k\right]\right\}. \tag{31}$$

The transformation matrix T_r can be computed in many ways, such as 'QR' decomposition, Gaussian elimination, etc., providing that [28–30]:

$$T_r H = \begin{bmatrix} 0 \\ H_2 \end{bmatrix}, \tag{32}$$

where $H_2 \neq 0$.

Once the system model is transformed into the regular form, the switching function and the control law can be designed as follows.

The switching function, based on linear reaching law [29,30] is defined as:

$$\sigma[k] = S\{x[k] - x_m[k]\} = Se[k]. \tag{33}$$

From Eq. (29), the switching function can be rewritten as:

$$\sigma[k] = S_1 e_1[k] + S_2 e_2[k]. \tag{34}$$

When the tracking error dynamics are in the sliding mode, that is $\sigma = \dot{\sigma} = 0$, $e_2[k]$ can be arranged as:

$$e_2[k] = -S_2^{-1} S_1 e_1[k] \tag{35}$$

When Eq. (35) is inserted into Eq. (30), the reduced-order dynamics in the sliding mode are obtained as follows:

$$e_1[k+1] = \begin{bmatrix} G_{11} & -G_{12}S_2^{-1}S_1 \end{bmatrix} e_1[k]. \tag{36}$$

In order to have stable dynamics in the sliding mode all of the eigenvalues of the matrix $[G_{11} - G_{12}K]$, where $K = S_2^{-1}S_1$, must be inside the unit circle [32]. Therefore, K can be considered as a state feedback matrix and can be determined by one of the state feedback design techniques such as the linear quadratic regulator (LQR), pole placement, etc., as long as the prescribed performance of the reduced-order system (30) is satisfied. When K is determined, the switching function coefficient matrix S in the original coordinates can be obtained as [29,33]:

$$S = S_2 \begin{bmatrix} K & 1 \end{bmatrix} T_r. \tag{37}$$

In Eq. (37), S_2 only acts as a scaling factor, so it can be chosen arbitrarily as long as it is invertible [28,29,33].

In SMC design the second phase, as stated above, is deriving a control law that drives the closed-loop system trajectory in the sliding mode and holds it there once reached.

By using the linear reaching law technique [29,33],

$$\sigma[k+1] = \emptyset\sigma[k], \tag{38}$$

where $\emptyset \in R$ and satisfying $0 \leq \emptyset < 1$.

When Eqs. (27), (33), and (38) are rearranged,

$$\emptyset\sigma[k] = \sigma[k+1] = Se[k+1] = S\{x[k+1] - x_m[k+1]\},$$

$$\emptyset\sigma[k] = S\{Ge[k] + (G - G_m)x_m[k] + Hu[k] - H_m r[k]\}, \tag{39}$$

and then the control law $u[k]$ can be derived from Eq. (39) as:

$$u[k] = (SH)^{-1}\{-SGe[k] - S(G - G_m)x_m[k] + \emptyset\sigma[k] + SH_m r[k]\}. \tag{40}$$

With the help of Eq. (40), the block diagram of the D-MRSMC controlled three-phase four-leg VSI is shown in Figure 4a.

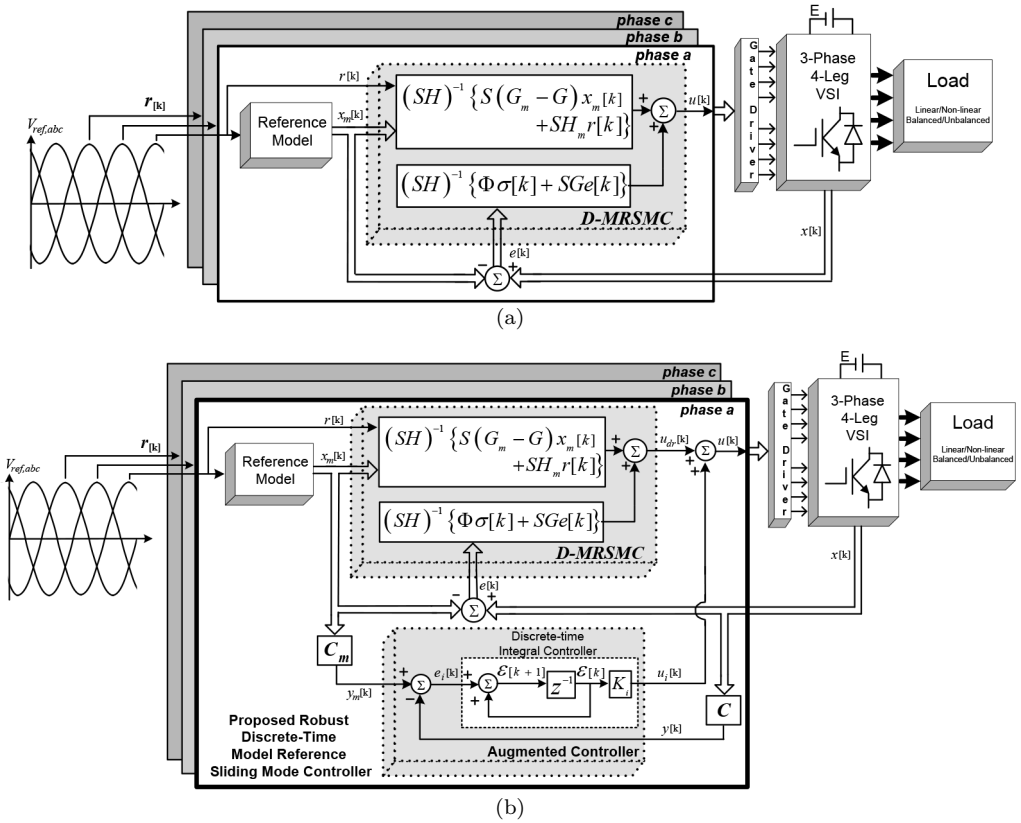

Figure 4. a) Block diagram of the D-MRSMC controlled VSI. b) Servo system with robust D-MRSMC and an integral controller for the three-phase four-leg VSI.

In this study the purpose is to design a servo system so that the output voltage of the VSI can follow the reference input. However, the controller designed in Section III and given in Figure 4a only regulates the dynamics of the system.

Therefore, it is necessary to add integrators within the loop to eliminate steady-state errors [34]. In Figure 4b, a block diagram of the designed servo system with D-MRSMC and an integral controller for the three-phase four-leg VSI is given.

From Figure 4b,

$$\varepsilon\left[k+1\right]=e_i\left[k\right]+\varepsilon\left[k\right], \tag{41}$$

where $e_i\left[k\right]=C_m x_m\left[k\right]-Cx\left[k\right]$, when $C_m=C$ is selected, and then

$$e_i\left[k\right]=C\left[x_m\left[k\right]-x\left[k\right]\right]=Ce\left[k\right] \tag{42}$$

is obtained.

The dynamics of the tracking error given in Eq. (28) can be written in a simplified form as:

$$e\left[k+1\right]=Ge\left[k\right]+H\vartheta\left[k\right]. \tag{43}$$

Then, using Eqs. (41), (42), and (43), the augmented error dynamics are obtained as:

$$\left[\begin{array}{c} e\left[k+1\right] \\ \varepsilon\left[k+1\right] \end{array}\right]=\left[\begin{array}{cc} G & 0 \\ C & 1 \end{array}\right]\left[\begin{array}{c} e\left[k\right] \\ \varepsilon\left[k\right] \end{array}\right]+\left[\begin{array}{c} H \\ 0 \end{array}\right]\vartheta\left[k\right]. \tag{44}$$

The design procedure of the control signal for the augmented error dynamic given in Eq. (44) is the same as stated in Eqs. (29)–(40). As seen from Figure 4b, the whole control signal of the designed discrete-time controller can be written as:

$$u\left[k\right] = u_{dr}\left[k\right] + u_i\left[k\right], \tag{45}$$

where $u_{dr}\left[k\right]$ is the dynamic regulator control signal as given in Eq. (40), and $u_i\left[k\right]$ is the integral controller signal that zeroes the steady-state error as given in Eq. (41). The control signal $u[k]$ in Eq. (45) will be implemented for each phase (a,b,c) independently as shown in Figure 4b.

4. Controller design

The design procedure of the controller and parameters are the same for each coordinate, *dq0*. Therefore, here, only the q-axis controller design procedure, as explained in Section 3, is given in detail. As stated in Section 2, the disturbance I_0 in Eq. (17) is neglected in the design of the controller. The parameters of the system used in the simulation studies are given in Table 1.

Table 1. Parameters of the three-phase four-leg VSI used in simulations.

Parameters	Value
DC-link voltage (E)	700 V
Rated output voltage ($V_{AN}V_{BN}, V_{CN}$)	$220\sqrt{2}$ V
Rated output frequency	50 Hz
Filter resistance	0.279 Ω
Filter inductance	1.2 mH
Filter capacitance	100 μF

The corresponding discrete-time system model is obtained below through discretization of the continuous-time system with a zero-order hold and a sampling period of $T = 50\,\mu s$:

$$\begin{bmatrix} i_q\left[k+1\right] \\ V_q\left[k+1\right] \end{bmatrix} = \begin{bmatrix} 0.8876 & -0.0397 \\ 4.8016 & 0.8987 \end{bmatrix} \begin{bmatrix} i_q\left[k\right] \\ V_q\left[k\right] \end{bmatrix} + \begin{bmatrix} 0.0397 \\ 0.1013 \end{bmatrix} V_{nin}[k].$$

The reference model is chosen as

$$\begin{bmatrix} i_{qm}\left[k+1\right] \\ V_{qm}\left[k+1\right] \end{bmatrix} = \begin{bmatrix} 0.8877 & -0.4035 \\ 0.4727 & 0.8987 \end{bmatrix} \begin{bmatrix} i_q\left[k\right] \\ V_q\left[k\right] \end{bmatrix} + \begin{bmatrix} 0.0410 \\ 0.0103 \end{bmatrix} V_{nin}[k].$$

Remembering that $x = \begin{bmatrix} i_q & V_q \end{bmatrix}$, $x_m = \begin{bmatrix} i_{qm} & V_{qm} \end{bmatrix}$, and $e = x - x_m$, the augmented error dynamics are obtained as:

$$\begin{bmatrix} e\left[k+1\right] \\ \varepsilon\left[k+1\right] \end{bmatrix} = \begin{bmatrix} 0.8876 & -0.0397 & 0 \\ 4.8016 & 0.8987 & 0 \\ 0 & 1.0 & 1.0 \end{bmatrix} \begin{bmatrix} e\left[k\right] \\ \varepsilon\left[k\right] \end{bmatrix} + \begin{bmatrix} 0.0397 \\ 0.1013 \\ 0 \end{bmatrix} \vartheta[k].$$

The transformation matrix T_r, provided in Eq. (32), is calculated as: $T_r = \begin{bmatrix} 0.3652 & 0.9309 & 0 \\ 0.9309 & -0.3652 & 0 \\ 0 & 0 & 1.0 \end{bmatrix}$.

The system model is transformed to regular form by using a transform matrix T_r:

$$\begin{bmatrix} e_{T_r}\left[k+1\right] \\ \varepsilon_{T_r}\left[k+1\right] \end{bmatrix} = \begin{bmatrix} -0.7299 & 0 & -0.6787 \\ -0.3652 & 1.0 & 0.9309 \\ 4.1626 & 0 & 2.5162 \end{bmatrix} \begin{bmatrix} e_{T_r}\left[k\right] \\ \varepsilon_{T_r}\left[k\right] \end{bmatrix} + \begin{bmatrix} 0 \\ 0 \\ 0.1088 \end{bmatrix} \vartheta_{T_r}[k].$$

The submatrices G11 and G12 described in Section 3 can be written from this regular formed matrix as:

$$G_{11} = \begin{bmatrix} -0.7299 & 0 \\ -0.3652 & 1.0 \end{bmatrix} \text{ and } G_{12} = \begin{bmatrix} -0.6787 \\ 0.9309 \end{bmatrix}.$$

Choosing closed-loop poles as $p_{1,2} = 0$ leads to a dead-beat controller, and then the state feedback matrix $K = S_2^{-1} S_1$ in Eq. (36) is obtained using the LQR technique:

$$K = \begin{bmatrix} 0.3401 & 0.5381 \end{bmatrix}$$

Then, using Eq. (37), as $SS = S_2 \begin{bmatrix} K & 1 \end{bmatrix} T_r$, and choosing $S_2 = H_2^{-1}$,

$$SS = \begin{bmatrix} 6.2685 & 7.4160 & 4.9472 \end{bmatrix}$$

is derived. After intermediate computations, the switching function coefficient matrix S, the gain of the integral controller K_i, and the coefficients needed for calculating $u[k]$ are obtained as follows.

$$S = \begin{bmatrix} SS(1) & SS(2) \end{bmatrix} = \begin{bmatrix} 6.2685 & 7.4160 \end{bmatrix}$$

$$K_i = [SS(3)] = 4.9472,$$

$$(SH)^{-1} = 1.0,$$

$$SG = \begin{bmatrix} 41.1725 & 6.4160 \end{bmatrix},$$

$$S(G - G_m) = \begin{bmatrix} -41.1725 & -6.4160 \end{bmatrix},$$

$$SH_m = 6.2685.$$

5. Simulation studies

The performance and robustness of the three-phase four-leg inverter controlled by the proposed discrete-time controller is investigated through computer simulations for different load conditions such as linear balanced/unbalanced, nonlinear balanced/unbalanced, and parameter variations. The performance of the proposed control method was simulated using the topology given in Figure 5 and the load conditions for the related simulations are shown in Table 2.

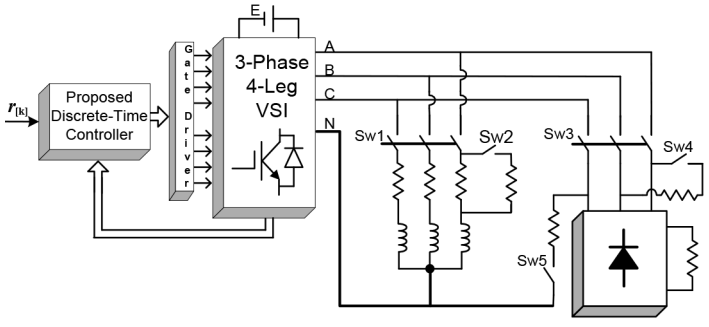

Figure 5. Block diagram of the load connection during simulation.

The simulation studies were conducted with the simplified VSI model given in Section 2. The three-phase load current samples used in the simulation studies were obtained from a real time experimental setup with sampling period $T = 50\,\mu s$

5.1. Simulations for different load conditions

The simulation studies for different load conditions, configured by switches as given in Table 2, are investigated below.

Case 1–2: The inverter was operated without a load at the beginning. Then, at t = 0.012 s the Sw1 was turned on and it was loaded with a linear-balanced load. Figure 6a shows the inverter output current-voltage variations for this case. The experiment was also repeated for a balanced nonlinear load and its result is given in Figure 6b. Here, a resistive loaded three-phase diode bridge rectifier without using a DC side filter capacitor was used as a nonlinear load.

Case 3: The performance of the proposed method in the case of an instantaneous and unbalanced load change is given in Figure 7. Here, the inverter was loaded with a linear balanced load at the beginning. Then a heavily linear unbalanced load was connected to the inverter by turning an Sw2 switch at t = 0.032 s.

Table 2. Switching table for different load condition.

Case	Description	Sw1	Sw2	Sw3	Sw4	Sw5
1	Linear balanced	On	Off	Off	Off	Off
2	Nonlinear balanced	Off	Off	On	Off	Off
3	Linear unbalanced	On	On	Off	Off	Off
4	Nonlinear unbalanced	Off	Off	On	Off	On
5	Nonlinear unbalanced	Off	Off	On	On	Off

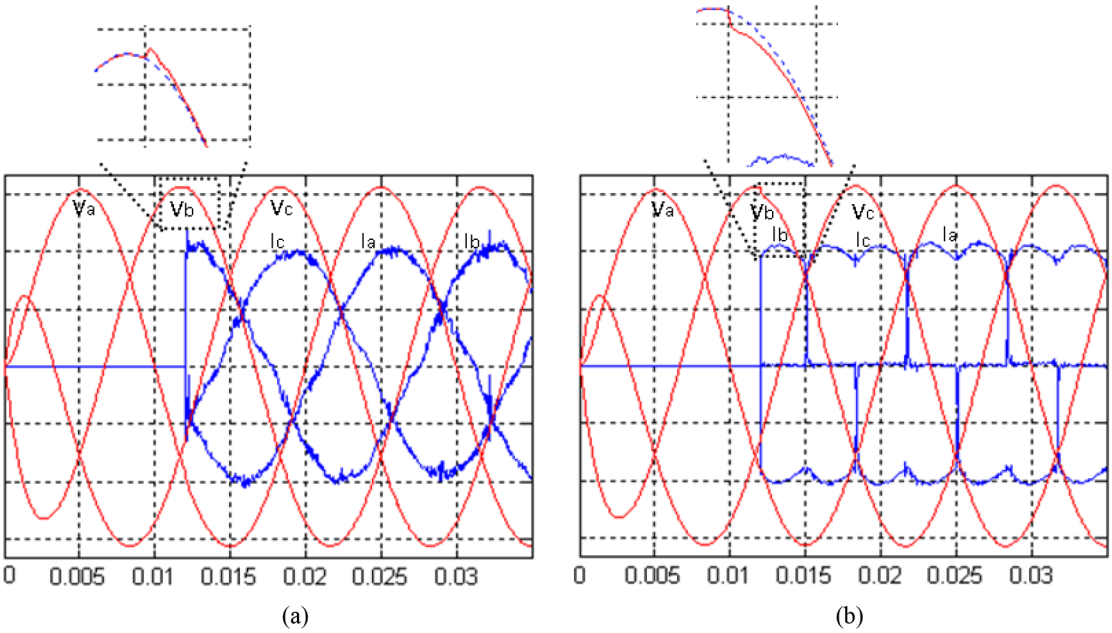

Figure 6. VSI output voltage (100 V/div) and current (10 A/div) waveforms with: a) a balanced linear load; b) a nonlinear (resistive loaded three-phase rectifier) load.

Case 4: Similar to Case 3, Figure 8 shows the inverter output current-voltage variations for transition from a nonlinear balanced load to a nonlinear unbalanced load. Here, the nonlinear load is the same as the one used in Case 2. The unbalanced load performances of the available methods are usually investigated for the case in which unbalancedness is introduced by using a load addition to any phase to neutral. Such an unbalanced load addition is the most frequent application for real-time applications of UPS.

Case 5: For this case, an unbalanced nonlinear load was created by turning on Sw3 and Sw4 switches. The performance of the proposed control method was investigated for this special case and the results are given in Figure 9.

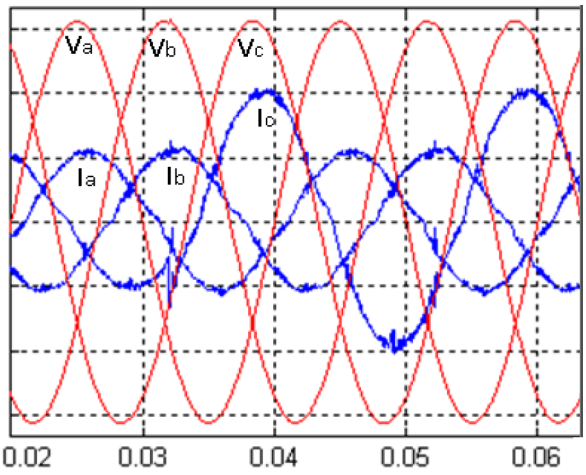

Figure 7. VSI output voltage (100 V/div) and current (10 A/div) waveforms during instantaneous linear unbalanced load variation.

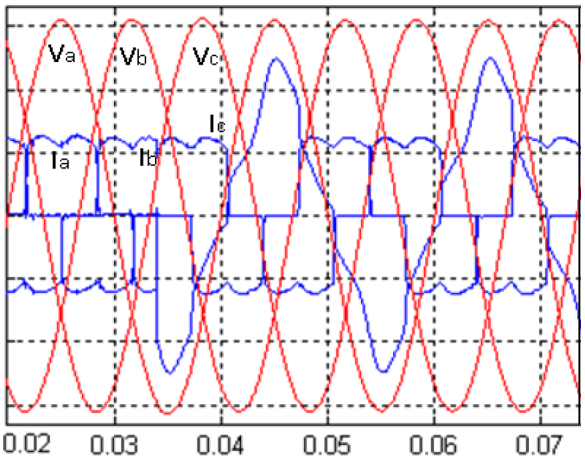

Figure 8. VSI output voltage (100 V/div) and current (10 A/div) waveforms during instantaneous nonlinear (phase-to-neutral) unbalanced load variation.

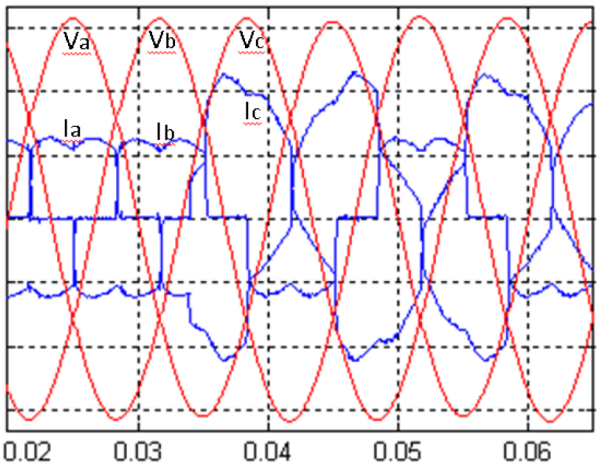

Figure 9. VSI output voltage (100 V/div) and current (10 A/div) waveforms during instantaneous nonlinear (phase-to-phase) unbalanced load variation.

From the simulation results given in Figures 6–9, it has been shown that the three-phase output voltages of the inverter controlled by the proposed RD-MRSMC method are accurately regulated in spite of the serious unbalanced linear/nonlinear load conditions and instantaneous unbalanced load variations.

The results in Cases 1–5 are investigated to make a comparison with similar studies in the literature. In Case 1 the inverter was loaded with a linear balanced load and the deviation of the output voltage of VSI was $\Delta V = 20\,V$, while the recovery time was 2 ms. In Case 2 the inverter was loaded with a nonlinear balanced load and the deviation of the output voltage of VSI was $\Delta V = 25\,V$, while the recovery time was 4 ms. In Case 1 and Case 2 the loads are switched on from no-load to full-load in step. In [35] the deviation of the

output voltage of VSI was $\Delta V = 25\ V$, and the recovery time was 2 ms. Furthermore, in that study the load was switched on softly. In [36] the inverter had huge changes under nonlinear unbalanced load conditions, the deviation of the output voltage of the VSI was approximately $\Delta V = 80\ V$, and the recovery time was 20 ms. In [37] the deviation of the output voltage of the VSI was $\Delta V = 30\ V$. Briefly, the results show that the proposed method improves the performance of the VSI output voltage dynamics under different load conditions.

5.2. Robustness test

In this special case the robustness of the designed system against system parameter variations was investigated. For this purpose, parameters of the LC filter connected to the inverter output were varied by 20%–50% as indicated in Table 3. Then simulations were carried out with nominal values and varied values of the parameters under the same nonlinear unbalanced load conditions. The simulation results given in Figure 10 confirm the robustness of the proposed method against parameter variations in a wide range.

Table 3. LC filter parameter variations.

Parameter	Nominal value	New value	% variation
L	1.2 μF	0.96 μF	20
C	100 μF	50 μF	50
R	0.2798 Ω	0.168 Ω	40

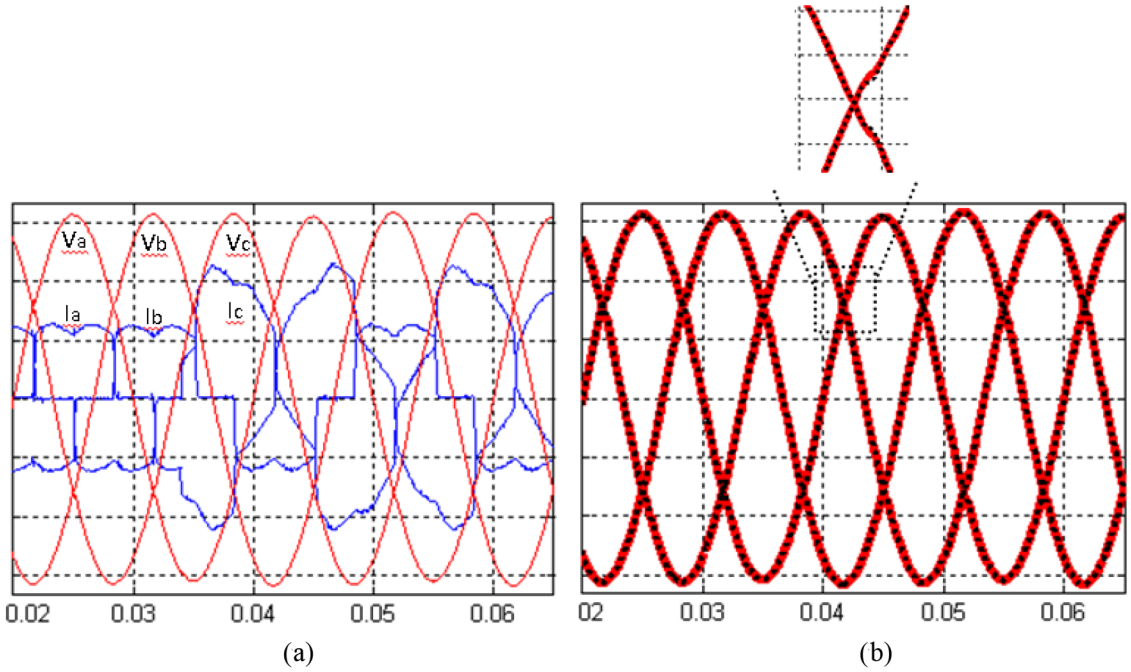

Figure 10. a) VSI output voltage (100 V/div) and current (10 A/div) waveforms after filter parameters are changed; b) VSI output voltage (100 V/div) waveforms with nominal (solid thick line) and changed (dashed line) parameters.

In Figure 10a the voltage and current waveforms are given for the nonlinear unbalanced load condition with nominal parameters. In Figure 10b the voltage waveforms are generated with nominal values (solid thick line) and varied values (dashed line) parameters for the same load condition. As seen from Figure 10b, although the system parameters varied in a wide range, the output voltages were almost unaffected.

6. Conclusions

In this study, a new RD-MRSMC based control method is proposed to increase the performance of the three-phase four-leg based UPS for stand-alone DGSs when loaded with linear balanced/unbalanced and nonlinear balanced/unbalanced loads. Simulation results show that the VSI controlled by the proposed method exhibits a remarkable performance. Furthermore, the proposed RD-MRSMC is shown to lead to robust characteristics of the VSI in spite of system parameter variations in a wide range and the omission in deriving a mathematical model of the system. The proposed controller's coefficients and gains are calculated offline. In real-time applications, the designed controller can be implemented only by simple algebraic operations. The output voltage of the VSI has been robust against variations by 20%–50% in R, L, C filter parameters and in 5 different cases. The results obtained in this study were compared with those of other studies in the literature and it was shown that the proposed method improves the performance of the VSI output voltage dynamics under different heavy load conditions.

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