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RLC circuit extraction with the differential evolution algorithm for conducted electromagnetic emission model of integrated circuits

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Abstract: This paper examines the modeling of conducted electromagnetic emissions of integrated circuits. In this study, test circuits were designed and printed circuit boards were prepared to measure the input impedance at the power supply pin of the microcontroller. After S-parameter measurements of the test circuit were performed in a frequency range of 10 MHz to 2 GHz, Z-parameters were obtained via S-parameters. Next, the impedance–frequency curve of the test circuit's power supply pin, which consists of a microcontroller core, printed circuit board, conductive trace, and SMA connector global impedances, was obtained. Therefore, all the traces, printed circuit board, and SMA connector impedance effects were eliminated with the deembedding technique. After all other impedance effects were deleted with the deembedding technique, the input impedance at the power supply pin of the microcontroller was obtained and shown with impedance–frequency characteristics. The passive (RLC) circuit was modeled from this curve and the results were compared to the measurements. The differential evolution algorithm was used to extract the optimal RLC passive elements. Finally, sensitivity analyses were successfully performed to ensure the accuracy of the extracted circuit.

Key words: Conducted emissions, electromagnetic, differential evolution algorithm, integrated circuits

1. Introduction

At the present time, silicon die can contain several hundred million transistors on a small chip area due to ongoing advances in semiconductor technology. On the other hand, increased work performance is progressively more difficult for the requested equipment due to the distortionary impact of the electromagnetic environment [1]. Electromagnetic interference (EMI) protection, which is particularly important in order to fulfill the functions of electronic systems, is becoming even more complex with the increasing integration efforts of electronic systems. Although integrated circuits (ICs) often play a critical role in the electromagnetic compatibility of an electronic system, most electromagnetic compatibility (EMC)-related problems have been focused on the external part of the IC core. EMC of the circuits prior to production is required to predict the performance of EMC. Researchers have been developing methods of measurement and designing techniques to improve the performance of ICs [1–14]. EM compatibility testing is usually performed after the design stage and before placing the IC on the printed circuit board. If the emission level is higher than the expected value, it leads to redesign, which may cause loss of time and money. For this reason, a model is needed to accurately and rapidly presume EM compliance. Several measurement methods for the emission of ICs have been created [1–14]. One method is the linear equivalent circuit and current source (LECCS) model, which has been used for the prediction

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of emissions and immunity tasks [6]. IC emission model-conducted emission is the method used to predict the electromagnetic emission at the IC [2,3]. Another emission model is the input/output buffer information specification (IBIS), which is used for printed circuit board (PCB) analysis [7,8]. An I/O interface model for integrated circuit (ICIM) model is also used in board design [3,9].

It is important to understand the reasons why EMC has become so important. Modern design relies increasingly on the processing of digital signals, which have very short rise and fall times. This gives them a very broad frequency spectrum, and they are thus more likely to interfere with other systems. Increasing the complexity of ICs and dynamic current consumptions is an important reason. Increasing the operating frequency and high clock speed also adds to the significance of EMC.

In this study, the layout of a printed circuit board was designed and a test circuit was prepared to measure the input impedance at the power supply pin of the microcontroller. After the measurement of the designed test circuit, the passive RLC circuit was modeled. The main advantage of such a model is to reduce the complexity of a digital IC by reducing the power network to a few passive elements. Then, a high density IC can be simulated on a basic analog simulator. As a result, internal and external conducted noises can be evaluated early in the design phase, and solutions can also be applied for the reflected specifications and requirements.

A test circuit containing the PIC16F628 microcontroller was designed and measurements were made. Network analysis was performed using the prepared test circuit measurement, and no voltage was applied to the circuit during the measurements. In this way, the global impedance of the PCB board, conducted path, SMA connector, and microcontroller core was obtained. Then the impedances of the PCB board, conductive path between the power supply pin and SMA connector, and SMA connector were removed with the deembedding technique, which is described in Section 2. After applying the deembedding technique, the Z-parameters were obtained by conversion of the S-parameters. Afterwards, obtained impedance values were shown by the impedance–frequency curve. The passive circuit element (RLC) model was obtained from the measured curve. The differential evolution algorithm used for the model shows high agreement with the results. Finally, sensitivity analyses were performed in order to ensure the appropriateness and accuracy of the extracted circuit.

2. Integrated circuit emission model

In this study, the entire standardization phase IC emission model has been used [2,3,10,12]. The basic structure of the model is shown in Figure 1. The IC emission model consists of 3 components: power distribution network, internal activity, and interblock coupling. The power distribution network is a circuit that consists of resistor, capacitor, and inductor elements. Internal activity is the independent current source or voltage source, and interblock coupling provides the coupling impedances between blocks and can be resistive, capacitive, and magnetic [13–16]. In this section, the test circuit design, measurement, and passive RLC circuit modeling will be discussed.

The test circuit shown in Figure 2 was designed to measure the impedance of a power supply pin. This double-sided printed circuit board, used in measurement, is made of FR4 material. Traces are made of copper with a thickness of 35 μm and static relative permittivity (r) of 4.6. Trace distance from the inner conductor of the SMA connector to the power supply pin is 19 mm. As shown in Figure 2, a subminiature version A (SMA) connector and PIC16F628 microcontroller were mounted on the board for measurement. The SMA connector enabled the test board to connect to the network analyzer. The PIC16F628 microcontroller, used in the test circuit, was fabricated in a 0.7-μm CMOS process and has an 18-pin DIP package. The operating voltage of the microcontroller ranges from 3 V to 5.5 V. The measurement was achieved by connecting the coaxial cable directly to the SMA connector. Before carrying out the measurement over the component, the short, open,

load, and thru (SOLT) calibration method was used to remove the effects of the connectors and coaxial cables connected to the network analyzer and to the test circuit. Due to the fact that the results were required for a wide frequency range, the measurements were made in different frequency ranges, making a new calibration for each range to ensure better accuracy. Hence, a frequency range from 10 MHz to 2 GHz was used in this study.

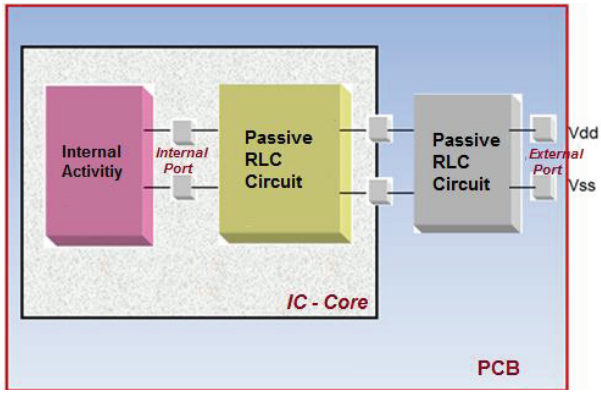


Figure 1. Integrated circuit emission basic macroblock.

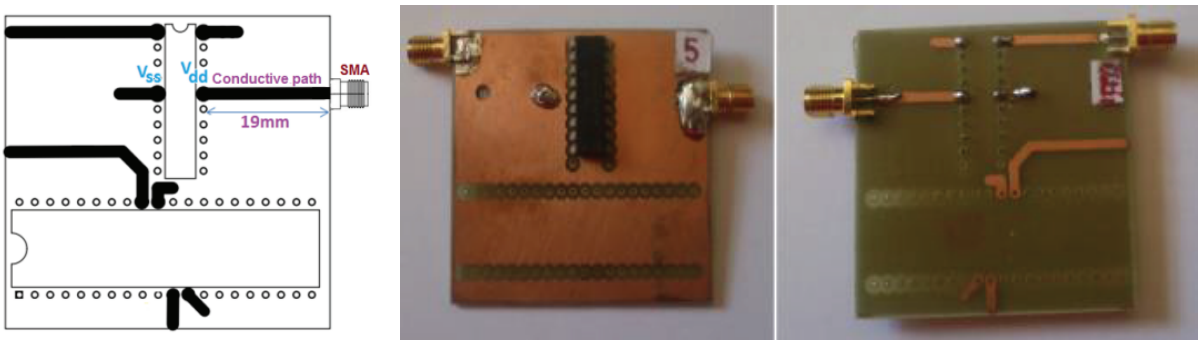


Figure 2. Designed and measured test circuit.

After designing the test circuit for measuring input impedance, a network analyzer was used to measure the global impedances of the device. A passive RLC circuit was extracted from this measurement result. At this stage, the following guidelines were followed:

- S-parameters were measured by network analyzer, and the results were then translated into impedance Z from which R, L, and C elements were tuned manually.
- The impedance of the SMA connector was deleted with the deembedding technique.
- The impedance of the path and board between the power supply pin and SMA connector was deleted with the deembedding technique.
- The passive RLC circuit was extracted once more by using the differential evolution algorithm.

The S_{11} parameter was translated into Z impedance values by using Eqs. (1)–(5). R is the real part of the value of S_{11}, and X is the imaginary part of the value of S_{11}.

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix} \tag{1}$$

$$S_{11} = R + jX \tag{2}$$

$$Z_{in(real)} = Z_0 \left(\frac{1 - R^2 - X^2}{(1-R)^2 + X^2} \right) \tag{3}$$

$$Z_{in(imag)} = Z_0 \left(j \frac{2X}{(1-R)^2 + X^2} \right) \tag{4}$$

$$|Z_{in}| = \sqrt{Z_{in(real)^2 + Z_{in(imag)^2}}} \tag{5}$$

3. Deembedding

Deembedding is a mathematical process that removes the effects of unwanted portions of the structure that are embedded in the measured data by subtracting their contribution. Traces on the board contribute a larger measured impact than the device under test [16]. The SMA connector, trace, and PCB board that cause the impedance effects that were eliminated by the deembedding method are shown in Figure 3.

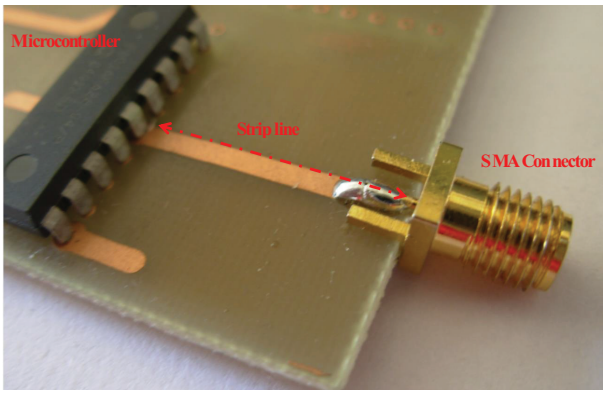


Figure 3. Deleted impedances caused by SMA connector, trace, and PCB board.

When processing the series circuit, the T parameter is more convenient, whereas for the parallel connection the Y parameter is easier. Therefore, the object extraction process in the form of series-connected circuits can be modeled as in Figure 4. The relationship between the T- and S-parameters is shown in the following equations. With some algebra, each T element can be translated from the S-parameter matrix, and each S-parameter element can be converted into the T-parameter matrix.

$$(T_{total}) = (T_a)\,(T_b) \tag{6}$$

$$(T_a) = (T_{total})\,(T_b)^{-1} \tag{7}$$

$$(T_b) = (T_a)^{-1}\,(T_{total}) \tag{8}$$

$$\begin{pmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{pmatrix} = \left(\frac{1}{S_{21}} \right) \begin{bmatrix} S_{12}S_{21} - S_{11}S_{22} & S_{11} \\ -S_{22} & 1 \end{bmatrix} \tag{9}$$

$$\begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} = \left(\frac{1}{T_{22}} \right) \begin{bmatrix} T_{12} & T_{11}T_{22} - T_{12}T_{21} \\ 1 & -T_{21} \end{bmatrix} \tag{10}$$

$$[T_m] = [T_A]\,[T_D]\,[T_B] \tag{11}$$

$$[T_D] = [T_A]^{-1}\,[T_m]\,[T_B]^{-1} \tag{12}$$

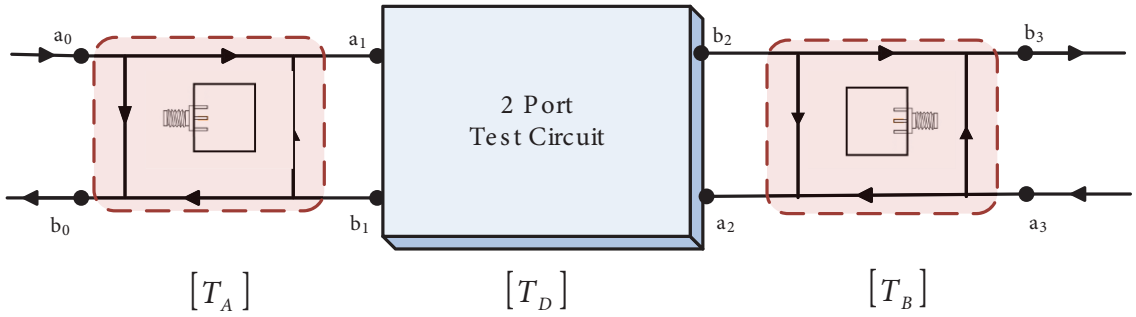


Figure 4. Model representation of the method of deembedding $[T_A]$.

4. Differential evolution algorithm

The differential evolution algorithm (DEA) is one of the powerful global optimization methods proposed by Storn and Price [17,18]. The DEA is an intelligence optimization algorithm that simulates the evolution of natural biology. It starts from a population that represents a gather of probable solutions. A population is composed of a certain quantity of individuals. These individuals are obtained by gene coding. The main program flowchart of the differential evolution algorithm is shown in Figure 5.

In [2], a genetic algorithm was used to extract the optimal RLC passive elements. In this study, the properties of the DEA, such as suitability for simple operation and converging to global optimum, are reflected to extraction of the passive RLC circuit. Each of the R, L, and C components were thought of as a chromosome in terms of DEA. The number of repetitions is determined as 200 to obtain the RLC passive elements. During the simulations, new populations representing the new gathering of new solutions were produced by crossover and mutation. The RLC circuit was obtained from the measured impedance–frequency curve, and the curve that was extracted from the model was compared to the measurements.

5. Measurement results

During the measurement, the test circuit was connected directly to the network analyzer with the SMA connector, and no voltage was applied. Figure 6 shows the measurement setup used to measure the global impedance of the PCB board, conducted path, SMA connector, and microcontroller core. The measurement results are shown in Figure 7. After measurements of S-parameters of the circuits were performed in the specified frequency range of 10 MHz to 2 GHz, Z-parameters were obtained from S-parameters. Figure 8 shows the frequency–impedance curve.

A new impedance curve was obtained after removing the effects of the unwanted portions of the test circuit that are embedded in the measured data by subtracting their contribution, as shown in Figure 9. According to the impedance–frequency curve in Figure 8, 2.4235 Ω resistance values were obtained at 39.85 MHz. The capacitance value was found as 0.959 nF at 10 MHz using Eq. (13). According to Eq. (14), the inductance value was found as 19.848 nH, taking the magnitude as 28.723 dB at 218.9 MHz. Figure 9 represents the RLC model of the power distribution network for the V_{dd} power supply pin. The root mean squared (RMS) percentage error was calculated as 0.78% between the measurement data and RLC model in the frequency range of 10 MHz to 250 MHz.

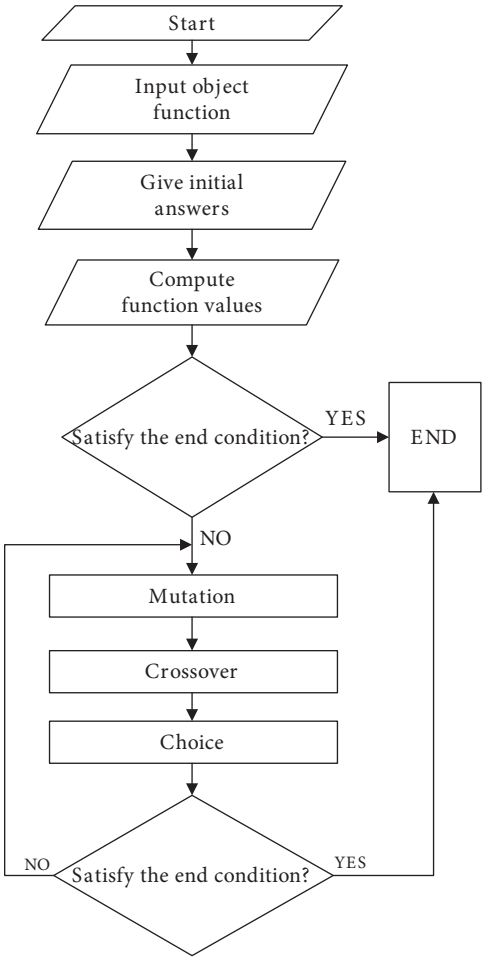


Figure 5. The main program flowchart of the differential evolution algorithm.

Figure 6. Measurement configuration of the test circuit.

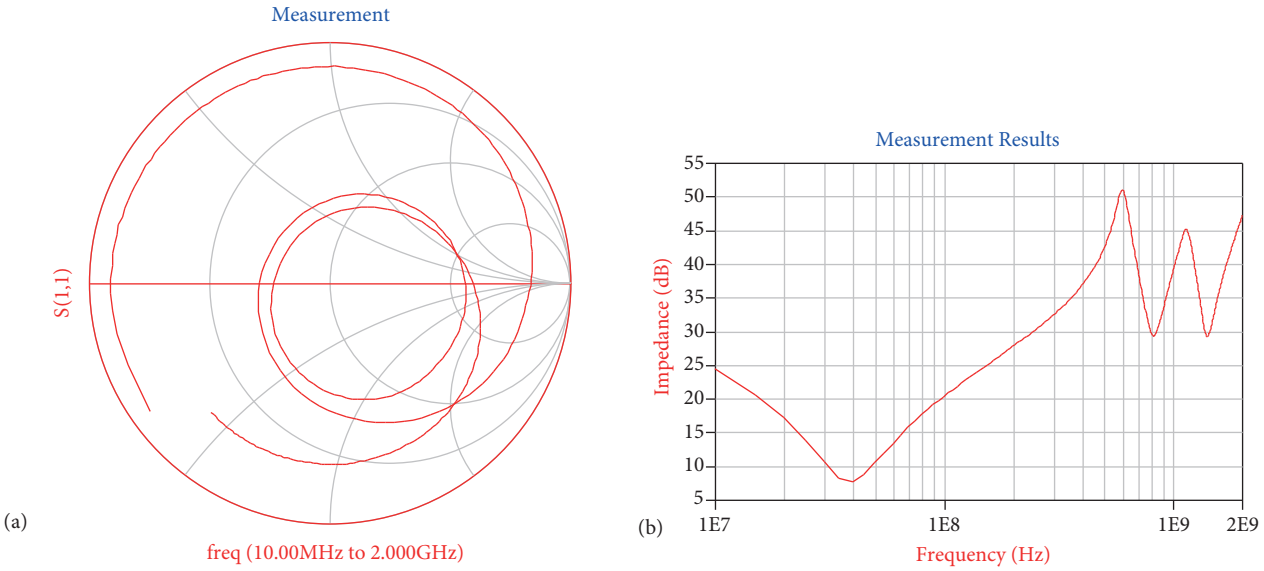


Figure 7. (a) The Smith chart of the measured S11; (b) measured impedance frequency curve.

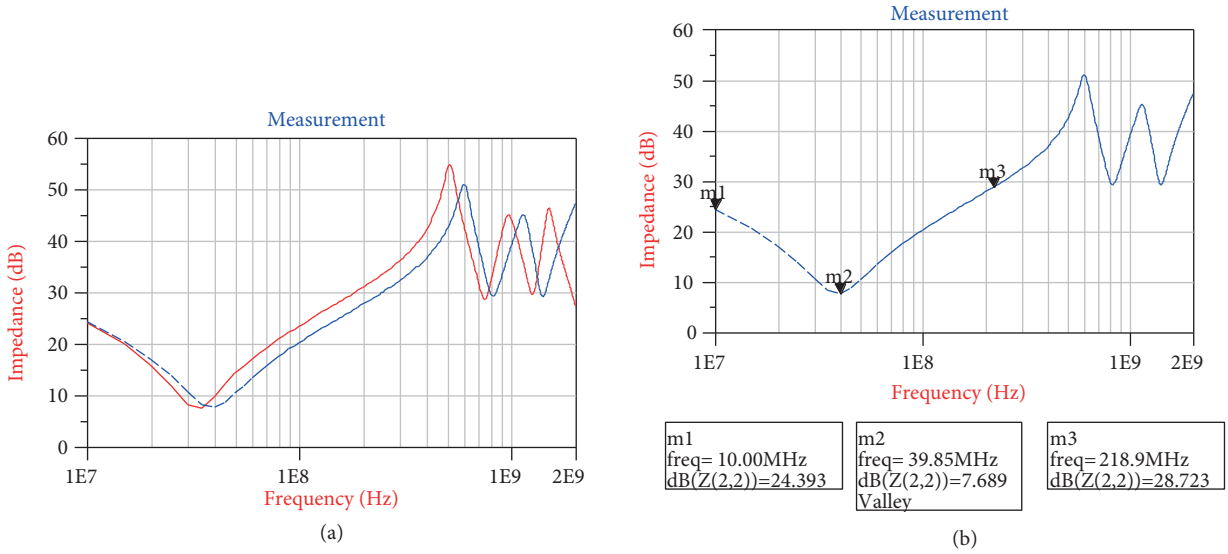


Figure 8. (a) The new impedance curve obtained by deembedding operation, the measurement (red line), after removing the effects (blue dashed line); (b) the impedance values were taken for the modeling of the RLC circuit.

$$Z_C = \frac{1}{j\omega C} \tag{13}$$

$$Z_L = j\omega L \tag{14}$$

Correlation between the measurement and RLC model is shown in Figure 10 as an impedance–frequency curve. After the deembedding process, the RLC model was extracted again by using the differential evolution algorithm. The frequency and impedance values were taken for the extraction of the RLC model as shown in Figure 11. The RLC model parameter values are found as $R_1 = 2.4\ \Omega$, $R_2 = 14\ \Omega$, $L_1 = 18.9$ nH, $L_2 = 18.6$ nH, $C_1 = 0.88$ nF, and $C_2 = 1.8$ pF using a DEA. Accordingly, the RLC circuit was extracted by using the DEA, as shown in Figure 12. The RMS percentage error between the measurement and extracted RLC model was calculated as 0.1% for the frequency range of 10 MHz to 820 MHz.

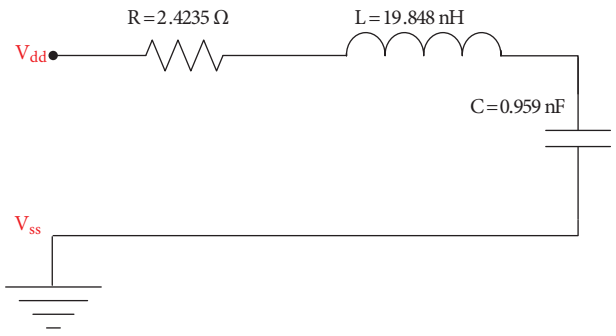


Figure 9. Passive circuit model of the power supply pin V_{dd}.

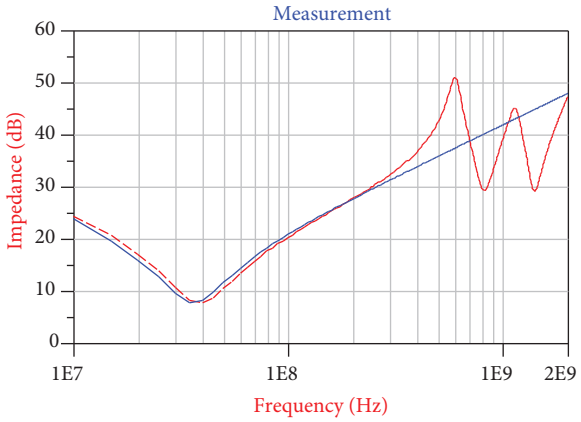
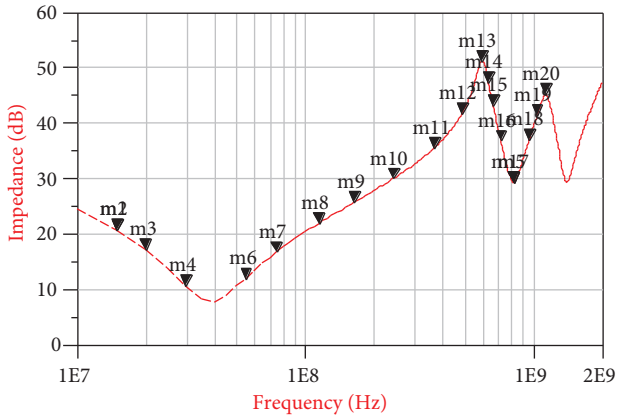


Figure 10. Correlation between measurement (red dashed line) and model (blue line).



m1 freq= 14.98MHz dB(Z(2,2))=20.602	m2 freq= 14.98MHz dB(Z(2,2))=20.602	m3 freq= 19.95MHz dB(Z(2,2))=17.148	m4 freq= 29.90MHz dB(Z(2,2))=10.660
m5 freq= 820.9MHz dB(Z(2,2))=29.270 Valley	m6 freq= 54.77MHz dB(Z(2,2))=11.800	m7 freq= 74.67MHz dB(Z(2,2))=16.674	m8 freq= 114.5MHz dB(Z(2,2))=21.842
m9 freq= 164.2MHz dB(Z(2,2))=25.683	m10 freq= 243.8MHz dB(Z(2,2))=29.929	m11 freq= 368.2MHz dB(Z(2,2))=35.370	m12 freq= 487.6MHz dB(Z(2,2))=41.572
m13 freq= 597.0MHz dB(Z(2,2))=51.044 Peak	m14 freq= 636.9MHz dB(Z(2,2))=47.243	m15 freq= 666.7MHz dB(Z(2,2))=43.113	m16 freq= 721.4MHz dB(Z(2,2))=36.704
m17 freq= 820.9MHz dB(Z(2,2))=29.270 Valley	m18 freq= 960.2MHz dB(Z(2,2))=36.887	m19 freq= 1.040GHz dB(Z(2,2))=41.320	m20 freq= 1.134GHz dB(Z(2,2))=45.134

Figure 11. The impedance values were taken for extraction of RLC circuit using DEA.

Figure 13 shows that there is a good agreement between the results of the RLC model obtained by DEA and the measurement results. The impedance of measurement, the first extracted RLC model, and the second extracted RLC model are shown by the black, blue, and red lines in Figure 13, respectively.

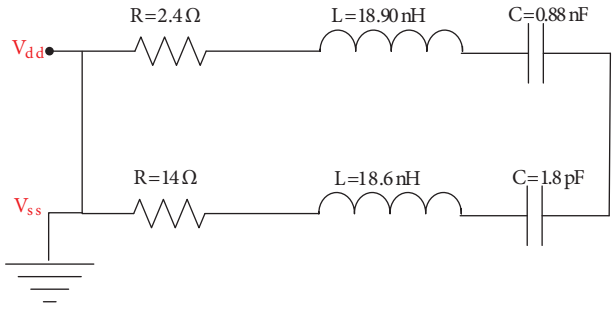


Figure 12. Passive circuit model extracted by DEA.

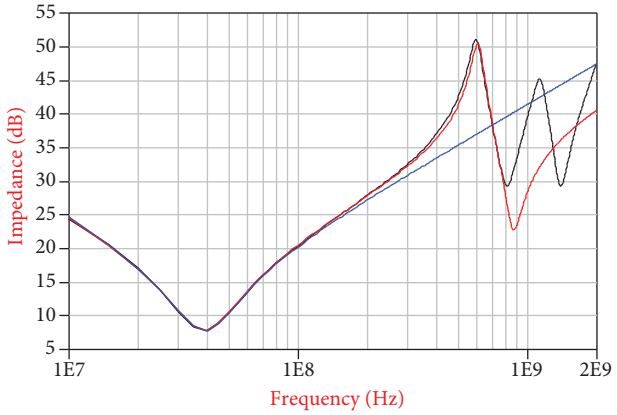


Figure 13. Measurement (black line), model (blue line), and model extracted by using DEA (red line).

The natural frequency (ω_0) and quality factor (Q) of the RLC circuit is given for sensitivity analyses in Eqs. (15)–(19).

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{15}$$

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{16}$$

$$S_L^{\omega_0} = S_C^{\omega_0} = -\frac{1}{2} \tag{17}$$

$$S_L^{Q} = -S_C^{Q} = \frac{1}{2} \tag{18}$$

$$S_R^{Q} = -1 \tag{19}$$

As can be seen from Eqs. (17) and (18), the sensitivities of the natural frequency and quality factor of C and L variables are less than or equal to a magnitude of 0.5. Since R determines the resonant frequency that causes the peak (maximum or minimum value) at the impedance–frequency curve, the sensitivity of the quality factor of the R variable is obtained as –1 in magnitude.

6. Conclusion

In this study, EMC of ICs was investigated with the use of the IC emission model, where the power distribution network is characterized by impedances. Good agreement between measured and simulated impedances was found. The RMS percentage error between the measurement and RLC model extracted by the DEA was calculated as 0.1% for a frequency range of 10 MHz to 820 MHz. Sensitivity analyses were performed to ensure the accuracy and suitability of the modeled circuit. The results show that an accurate modeling of the circuit is possible without too many complications. In the future, models will be studied based on transmission lines for higher frequencies.

Acknowledgment

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