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Highly efficient three-phase three-level multilevel inverter employing different commutation strategies

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Abstract: This paper introduces a new three-phase three-level voltage source inverter. The proposed topology constitutes the conventional three-phase two-level inverter with three bidirectional switches. For purpose of generating the appropriate switching gate signals, two different commutation strategies are suggested and analyzed. A comparison between both strategies in terms of power losses and efficiency are presented. To ensure the feasibility of the proposed configuration with its suggested commutation strategies, the prototype of the proposed inverter was manufactured and the experimental results are given.

Key words: Multilevel inverter, bidirectional switch, commutation, switching loss, efficiency

1. Introduction

There is an increasing interest towards power conversion as many industrial applications such as motor drives and power systems are requiring power converters. Therefore, multilevel inverters are being increasingly adopted for such applications. Multilevel inverters consist of a group of switching devices and DC voltage supplies or capacitors, the output of which produces voltages with stepped waveforms. Multilevel technology started with the three-level converter, followed by numerous multilevel converter topologies. Basically, there are three main topologies of such inverters, known as neutral point clamped (NPC), flying capacitor (FC), or capacitor clamped and cascaded H-bridge (CHB). The NPC multilevel inverter is an attractive high-voltage multilevel inverter due to its robustness. The neutral point voltage deviation always remains an undesired feature in NPC inverters. For this reason, DC link capacitor voltage balancing is a crucial task in such configurations. The FC multilevel converter makes use of flying capacitors for voltage clamping. For this topology, the voltage synthesis is more flexible than NPC topology due to the transformer-less operation and redundant phase leg states that make the semiconductor switches share the same distributed stress. However, the use of an excessive number of storage capacitors for higher voltage steps is considered the main drawback in such converters. The cascaded H-bridge CHB multilevel inverter is the combination of multiple units of single-phase H-bridge power cells. Because it has simple and modular control, it is more used for high-voltage applications. However, the large number of utilized DC supplies is considered the main disadvantage of the CHB structure [1–5]. Apart from these three main topologies, other topologies are introduced, including hybrid, generalized, and combined topologies [6–13]. For some applications such as adjustable speed drive, where the current is flowing in both directions, bidirectional switches are needed. Compared to the unidirectional one, a bidirectional switch is able to conduct

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the current and withstanding voltage in both directions [14]. On other hand, for the purpose of improving the performance of the conventional single-phase H-bridge inverter, different topologies employing different types of bidirectional switches were suggested in [15,16]. In these topologies the output voltage waveform tends to be more sinusoidal as more voltage steps can be obtained. However, they are designed for single-phase applications only. Three-phase N-level voltage and current source inverters with different topologies based on bidirectional switches were presented in [17–20]. Bidirectional switches with appropriate control techniques can improve the performance of multilevel inverters in terms of reducing semiconductor components, reducing total power loss, minimizing the withstanding voltage, and achieving the desired output voltage with higher levels [21–24]. This paper begins by introducing the power circuit of the proposed three-phase three-level multilevel inverter. The operation principle with the first suggested commutation is analyzed. Furthermore, for the purpose of switching loss reduction in the proposed inverter, a new commutation strategy is presented in detail. A comparison between both commutation strategies in terms of total power losses and efficiency is explained. Finally, the obtained experimental results are provided.

2. System configuration

Three different bridge-leg structures are proposed as shown in Figures 1a–1c. Each one makes use one bidirectional switch (two IGBTs, two diodes) type. The function of such a switch is to control the flow of current (i) to and from the DC-link mid-point (o) in both directions. Operating states and conducting devices for suggested structures are illustrated in Table 1.

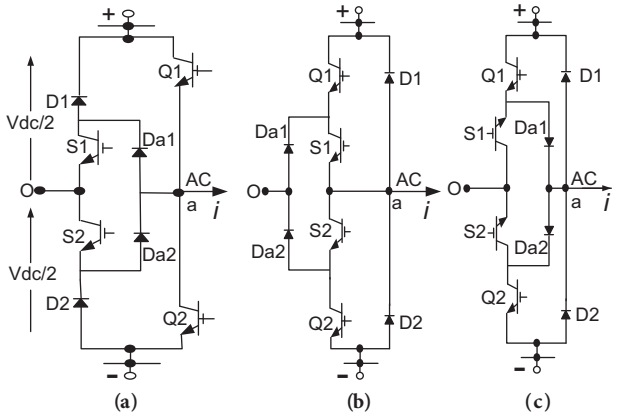

Figure 1. Bridge-leg with three different structures.

Table 1. Operating states of the proposed bridge-legs devices.

Bridge-leg (a)			Bridge-leg (b)			Bridge-leg (c)		
Current	Devices conducting	Vao	Current	Devices conducting	Vao	Current	Devices conducting	Vao
$i > 0$	$Q1$	$+Vdc/2$	$i > 0$	$Q1$ $S1$	$+Vdc/2$	$i > 0$	$Q1$ $Da1$	$+Vdc/2$
	$D2$ $Da2$	$-Vdc/2$		$D2$	$-Vdc/2$		$D2$	$-Vdc/2$
	$S2$ $Da2$			$S1$ $Da1$			$S1$ $Da1$	
$i < 0$	$D1$ $Da1$	$+Vdc/2$	$i < 0$	$D1$	$+Vdc/2$	$i < 0$	$D1$	$+Vdc/2$
	$Q2$	$-Vdc/2$		$Q2$ $S2$	$-Vdc/2$		$Q2$ $Da2$	$-Vdc/2$
	$S1$ $Da1$			$S2$ $Da2$			$S2$ $Da2$	

The basic topology of the proposed inverter is depicted in Figure 2. Three bridge-legs shown in Figure 1a connected in parallel to two series DC supplies are forming the power circuit of the proposed three-phase three-level multilevel inverter. The full bridge consists of six switches, Q1, Q2, Q3, Q4, Q5,and Q6. Each and every bidirectional switch used in the suggested configuration is the combination of two IGBTs and two diodes (for instance: S1, S2, Da1, and Da2 in leg a). Bidirectional switches ease the flow of current in both directions.

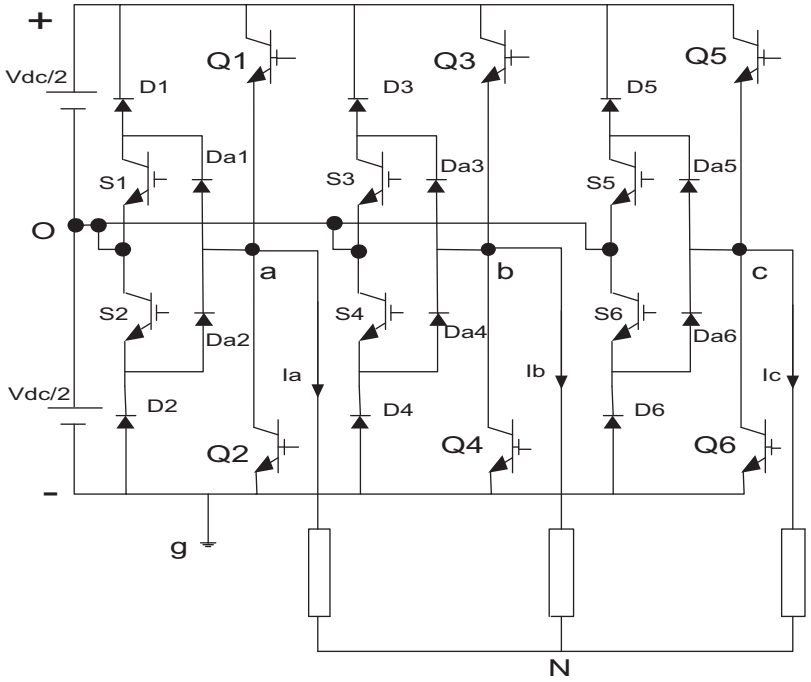

Figure 2. Circuit diagram of the proposed three-phase three-level inverter.

The voltage rating of the conventional full bridge switches Q1, Q2, Q3, Q4, Q5,and Q6 is (Vdc), whereas the middle bidirectional switches S1, S2, S3, S4, S5,and S6 and diodes D1, D2, D3, D4, D5, D6, Da1, Da2, Da3, Da4, Da5, and Da6 have a voltage rating of ($Vdc/2$), which is half of the DC bus voltage. The suggested inverter is designed to achieve five voltage levels at the output Vab ($+Vdc$, $+Vdc/2$, 0, $-Vdc/2$, $-Vdc$). According to switching states Sa, Sb, and Sc,the inverter line to ground voltages (Vag, Vbg, Vcg) can be calculated as follows:

$$\begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix} = \frac{Vdc}{N-1} \times \begin{bmatrix} Sa \\ Sb \\ Sc \end{bmatrix}, \tag{1}$$

where $N = 3$ is the number of voltage levels. By considering leg a, the operating status of the switches in the proposed inverter is represented by switching the Sa state as illustrated in Table 2.

Table 2. The definition of switch states.

Sa	Vag	$Q1$	$S2$	$S1$	$Q2$
2	$+Vdc$	on	off	off	off
1	$+Vdc/2$	off	on	on	off
0	0	off	off	off	on

Line to line voltages are related to line to ground voltage by:

$$\begin{bmatrix} Vab \\ Vbc \\ Vca \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} Vag \\ Vbg \\ Vcg \end{bmatrix}. \quad (2)$$

With the staircase modulation technique, the balanced load voltage can be achieved if the inverter operates on the modes depicted in Table 3. The inverter may have 12 different switching states within a cycle of the output waveform.

Table 3. Modes of operation of the proposed three-phase multilevel inverter during one cycle.

Sa Sb Sc	$Q1$	$S1$ $S2$	$Q2$	$Q3$	$S3$ $S4$	$Q4$	$Q5$	$S5$ $S6$	$Q6$	Vab	Vbc	Vca
200	on	off	off	off	off	on	off	off	on	$+Vdc$	0	$-Vdc$
210	on	off	off	off	on	off	off	off	on	$+Vdc/2$	$+Vdc/2$	$-Vdc$
220	on	off	off	on	off	of	off	off	on	0	$+Vdc$	$-Vdc$
120	off	on	off	on	off	off	off	off	on	$-Vdc/2$	$+Vdc$	$-Vdc/2$
020	off	off	on	on	off	off	off	off	on	$-Vdc$	$+Vdc$	0
021	off	off	on	on	off	off	off	on	off	$-Vdc$	$+Vdc/2$	$+Vdc/2$
022	off	off	on	on	off	off	on	off	off	$-Vdc$	0	$+Vdc$
012	off	off	on	off	on	off	on	off	off	$-Vdc/2$	$-Vdc/2$	$+Vdc$
002	off	off	on	off	off	on	on	off	off	0	$-Vdc$	$+Vdc$
102	off	on	off	off	off	on	on	off	off	$+Vdc/2$	$-Vdc$	$+Vdc/2$
202	on	off	off	off	off	on	on	off	off	$+Vdc$	$-Vdc$	0
201	on	off	off	off	off	on	off	on	off	$+Vdc$	$-Vdc/2$	$-Vdc/2$

Regarding Table 3, it is observed that two IGBTs per leg are receiving the same pulse in the same time. Based on the load current direction, one of these two IGBTs conducts the current.

3. Improved commutation

As mentioned earlier, each phase can be connected in three different switching states, 2, 1, and 0. *Vag = + Vdc*, for instance, could be obtained when Q1 is on. For both current directions *Vag = + Vdc/2* is obtained when S1 and S2 are turned on simultaneously, whereas *Vag* = 0 if only Q2 is on. In order to improve the performance of the proposed inverter in terms of reducing the semiconductors components' switching loss and increasing the inverter's efficiency, a new commutation strategy is suggested. The proposed commutation suggests a modification in pulse distribution by which a lower switching loss and higher efficiency can be attained.

For each output line to ground voltage level, two switches will turn on simultaneously, as illustrated in Table 4.

Table 4. The definition of the switching state (second commutation).

Sa	Vag	$Q1$	$S2$	$S1$	$Q2$
2	$+Vdc$	on	on	off	off
1	$+Vdc/2$	off	on	on	off
0	0	off	off	on	on

According to *Vag* level and current direction, the operation of each leg can be divided into eight states. For the state shown in Figure 3a, it is assumed that:

1- $Vag = + Vdc$ (Q1 and S2 are on) and Ia is positive.

In order to achieve switching transition from (+) to (o), Q1 is turned off and S1 is turned on with short delay time to avoid the short circuit. Once Q1 is turned off, the current naturally flows through S2 and Da2 connecting phase (a) to the mid-point (o).

However, if the current Ia is negative, the current commutates over S1 and Da1 after turning off Q1, as depicted in Figure 3b.

If switching transition from (o) to (+) is required, two states need to be considered.

1- Ia is positive (Figure 3c).

First $S1$ is turned off, and after the turn-on delay, Q1 is turned on. The positive current keeps on flowing through S2 and Da2 until Q1 is turned on. Once Q1 is turned on, the current naturally commutates over Q1, achieving $Vag = + Vdc$.

2- Ia is negative (Figure 3d).

Once S1 turns off, the current naturally flows through Da1 and D1. After turn-on delay time, Q1 is turned on. Following the same commutation strategy, the switching transitions from (-) to (o) and (o) to (-) in both current directions are as shown in Figures 3e–3h, respectively.

Following the new commutation strategy, the output line to line voltages produced by the proposed inverter are illustrated in Table 5.

Table 5. Mode of operation of the proposed three-phase multilevel inverter during one cycle (second commutation).

Sa Sb Sc	Q1	S1	S2	Q2	Q3	S3	S4	Q4	Q5	S5	S6	Q6	Vab	Vbc	Vca
200	on	off	on	off	off	on	off	on	off	on	off	on	+Vdc	0	–Vdc
210	on	off	on	off	off	on	on	off	off	on	off	on	+Vdc/2	+Vdc/2	–Vdc
220	on	off	on	off	on	off	on	off	off	on	off	on	0	+Vdc	–Vdc
120	off	on	on	off	on	off	on	off	off	on	off	on	–Vdc/2	+Vdc	–Vdc/2
020	off	on	off	on	on	off	on	off	off	on	off	on	–Vdc	+Vdc	0
021	off	on	off	on	on	off	on	off	off	on	on	off	–Vdc	+Vdc/2	+Vdc/2
022	off	on	off	on	on	off	on	off	on	off	on	off	–Vdc	0	+Vdc
012	off	on	off	on	off	on	on	off	on	off	on	off	–Vdc/2	–Vdc/2	+Vdc
002	off	on	off	on	off	on	off	on	on	off	on	off	0	–Vdc	+Vdc
102	off	on	on	off	off	on	off	on	on	off	on	off	+Vdc/2	–Vdc	+Vdc/2
202	on	off	on	off	off	on	off	on	on	off	on	off	+Vdc	–Vdc	0
201	on	off	on	off	off	on	off	on	off	on	on	off	+Vdc	–Vdc/2	–Vdc/2

4. Switching loss and efficiency study

In order to compare between both commutation strategies in terms of switching loss and efficiency, it is necessary to determine in which semiconductor components switching loss occurs, as well as the values of such loss. Basically, the main losses in semiconductor components such as IGBTs and diodes are categorized into two groups: conduction loss ($Pcon$) and switching loss (Psw). In general;

$$Psw\_IGBT = \frac{1}{T}\int_0^T Eon(t).dt + \frac{1}{T}\int_0^T Eoff(t).d(t), \tag{3}$$

$$Psw\_diode = \frac{1}{T}\int_0^T Err(t).dt, \tag{4}$$

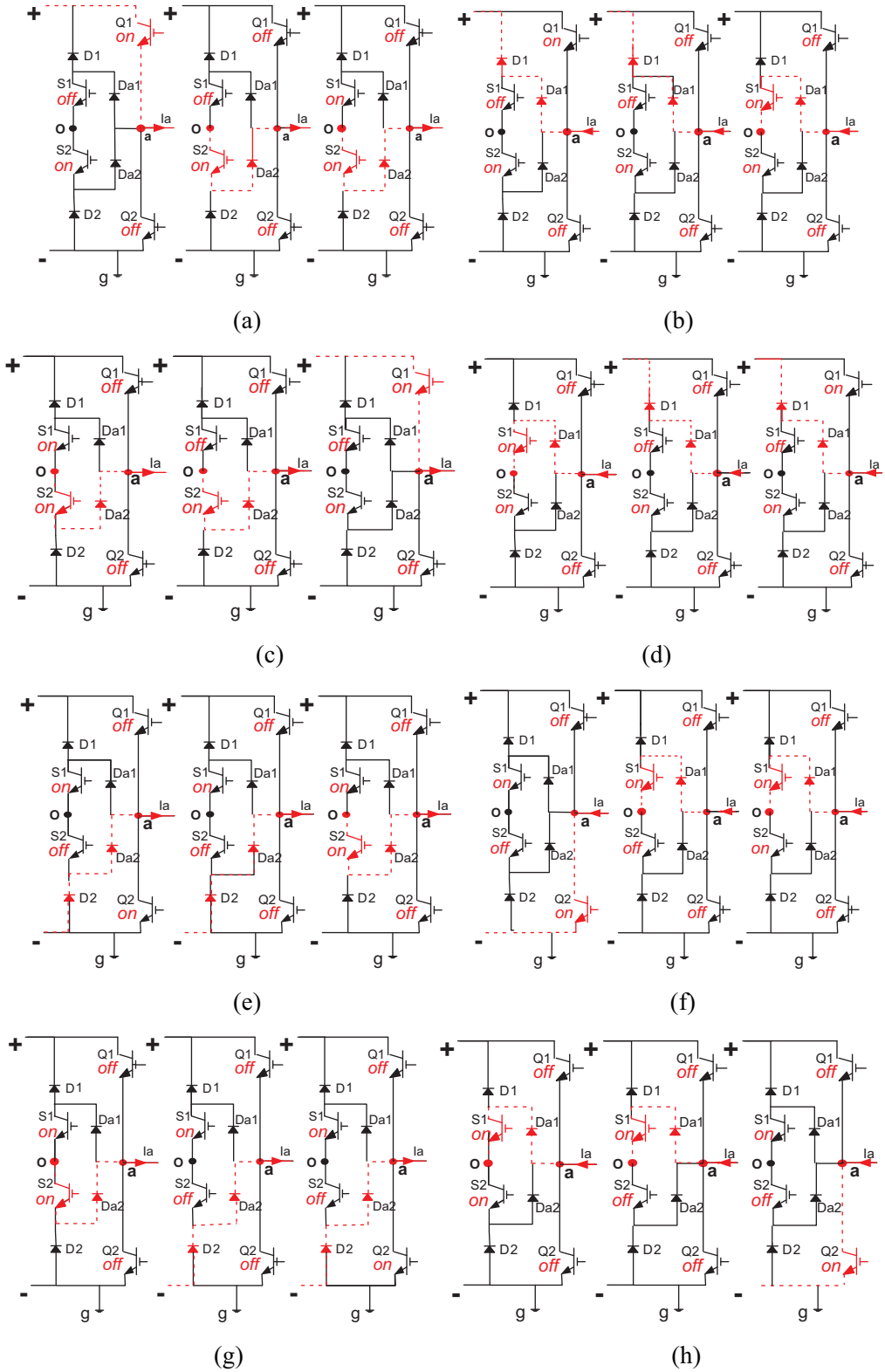

Figure 3. Current directions and commutation sequence during switching transitions.

where *Eon(t)* is a turn-on loss and *Eoff(t)* is a turn-off loss. Switching losses *Eon(t)* and *Eoff(t)* are experienced during the on and off states, respectively. *Err(t)* is the reverse recovery loss of the diode, the majority of the switching loss, which is experienced when the diode is turned off (off-state).

$$Pcon\_IGBT = \frac{1}{T}\int_0^T Von\_IGBT \times i(t).dt \tag{5}$$

$$Pcon\_Diode = \frac{1}{T}\int_0^T Von\_diode \times i(t).dt \tag{6}$$

Conduction losses of the IGBT and diode are approximated based on their forward voltage drops *Von_IGBT, Von_diode* and the instantaneous current i(t) flowing through the IGBT or diode.

The total losses, *Pt*, are expressed as:

$$P_t = P_{con} + P_{sw}\,. \tag{7}$$

Once the total semiconductor losses *Pt* in the introduced inverter are defined, the relative inverter efficiency is determined based on the following formula:

$$\eta\% = \frac{Pout}{Pt + Pout} \times 100. \tag{8}$$

Table 6 provides different current directions with the corresponding switching transitions in leg a. Therefore, and based on these two parameters, the switching loss can be simply tracked. In the first commutation, switching loss is experienced in two or three semiconductor components. However, the second commutation strategy manages to make the loss occur in two semiconductor components (diode and IGBT). For this reason, the second commutation is more efficient.

Table 6. Switching transitions with related switching losses.

Load current	Switching transition	Switching loss energies	
		First commutation	Second commutation
$Ia > 0$	$(+) \rightarrow (O)$	$EQ1_{off}$, $ES2_{on}, EDa2_{on}$	$EQ1_{off}, EDa2_{on}$
	$(O) \rightarrow (+)$	$EQ1_{on}$, $ES2_{off}, EDa2_{off}$	$EQ1_{on}, EDa2_{off}$
	$(O) \rightarrow (-)$	$ES2_{off}, ED2_{on}$	$ES2_{off}, ED2_{on}$
	$(-) \rightarrow (O)$	$ES2_{on}, ED2_{off}$	$ES2_{on}, ED2_{off}$
$Ia < 0$	$(+) \rightarrow (O)$	$ES1_{on}$, $ED1_{off}$	$ES1_{on}, ED1_{off}$
	$(O) \rightarrow (+)$	$ES1_{off}, ED1_{on}$	$ES1_{off}, ED1_{on}$
	$(O) \rightarrow (-)$	$EQ2_{on}$, $ES1_{off}, EDa1_{off}$	$EQ2_{on}, EDa1_{off}$
	$(-) \rightarrow (O)$	$EQ2_{off}$, $ES1_{on}, EDa1_{on}$	$EQ2_{off}, EDa1_{on}$

A MATLAB/Simulink model of the proposed inverter was developed to study the conduction and switching power losses at different operating conditions. The inverter delivers variable power to a distribution power system. The inverter output is connected to the 15 kV, 20 MVA, 50 Hz system through a 1000 V/15 kV transformer. A 1500 V DC supply is used to feed the proposed inverter. The multilevel inverter is controlled through two regulators to produce the desired powers at different power factors (PF = 0.85, 0.75, 0.65, and 0.55), respectively.

It is well known that the sinusoidal pulse-width modulation PWM strategies employed to control multilevel inverters strongly rely upon switching frequency. The operating switching frequencies used in these techniques can be classified into three groups: low ($fc < 2$ kHz), medium ($2 > fc < 24$ kHz), and high ($fc > 24$ kHz). Since the proposed inverter is designed to operate as a part of a distribution power system, where the typical operating switching frequencies used are normally set in a low or medium range, the sinusoidal PWM modulator is managed to use a carrier frequency fc with different values (1, 2, 4, 6, and 8 kHz).

The type of semiconductors selected for power loss estimation in this case is (5SNE 0800M170100) 1700 V/800 A. For 4 kHz carrier frequency with 150 kW output power at power factor PF = 0.75, Figures 4a and 4b respectively depict power loss distributions among the semiconductor devices (leg a) using the suggested commutations COM1 and COM2. It is clear that both commutations lead to a similar conduction loss, *Pcon*. However, as expected, the lower switching loss *Psw* occurs in COM2. In Figure 4c the inverter's efficiencies are calculated for four different power factors. The efficiency is varying proportionally with power factor and the proposed inverter with COM2 has a higher efficiency comparing to COM1. Finally, for *Pout* = 150 kW and by considering a typical operating power factor of transmission line, PF = 0.75, the inverter's efficiencies at the corresponding five switching frequencies are shown in Figure 4d. The efficiency varies inversely with the switching frequency. As the switching frequency increases, the efficiency of the inverter decreases as a result of switching loss being considerably increased in the semiconductor components. The higher switching frequency that is used, the more switching power loss will be, as experienced by the proposed inverter with COM1 resulting in lower efficiency comparing to COM2.

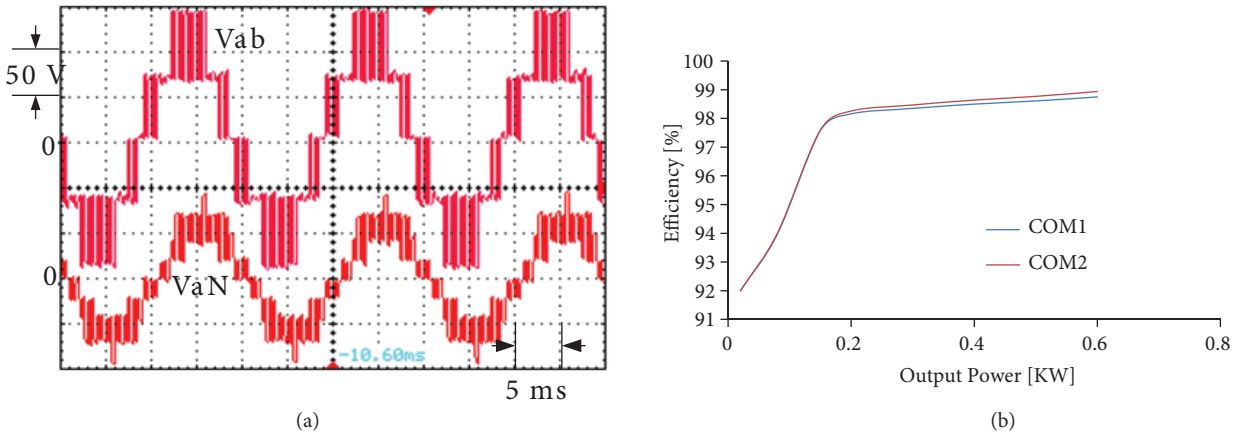

Figure 4. a) *Pcon* and *Psw* distribution with COM1, b) *Pcon* and *Psw* distribution with COM2, c) efficiency vs. PF and d) efficiency vs. *fc*.

5. Experimental results

In order to verify the feasibility of the proposed topology, its prototype was manufactured. The TMS320F335 Digital Signal Processor DSP is used to generate the switching gate signals for the proposed inverter switches. The DC link is made of two series DC supplies and the three-phase resistive-inductive load in star connection is connected to the inverter output terminals. The fundamental frequency and PWM are two modulation techniques employed to operate the proposed inverter at fundamental and medium switching frequencies. The input parameters of the suggested inverter power circuit are illustrated in Table 7 and the control block diagram of the introduced inverter is depicted in Figure 5.

Table 7. Input parameters of the power circuit.

Parameters	Value
Nominal out power ($Pout$)	0.7 kW
DC bus voltage (Vdc1, Vdc2)	Vdc1 = Vdc2 = 75 V
Fundamental frequency (f)	50 Hz
Carrier frequency (fc)	4 kHz
Modulation index (Ma)	1
Three-phase resistive-inductive load (R-L) in star connection	40 ohm – 3 mH/Phase
Controller	TMS320F335

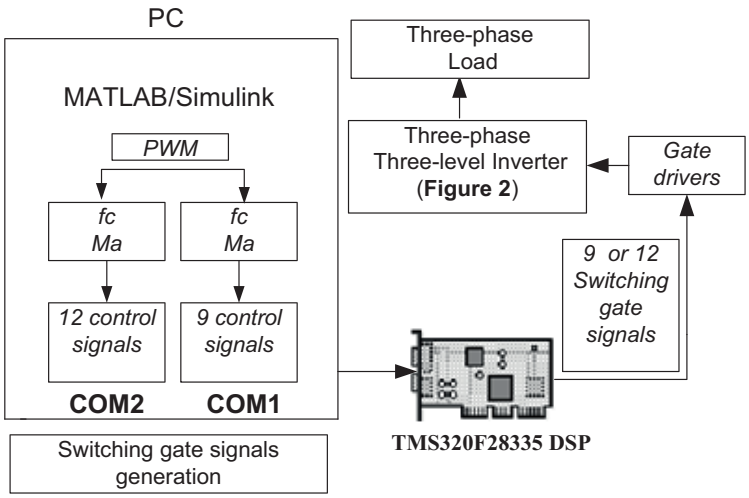

Figure 5. The control block diagram.

In order to achieve a staircase waveform with three positive voltage steps, both suggested commutation strategies are implemented. The controller manages to generate the appropriate switching gate signals that lead the inverter to output the desired voltage. For the first commutation (COM1) pulses (leg a) shown in Figure 6a, it is observed that (S1&S2) receive the same pulse, and Q1 (S1&S2) and Q2 are always in inverted conditions. Figure 6b shows the second commutation (COM2) pulses within a cycle (20 ms) of the output waveform. In the beginning time, the two switches Q1 and S2 are receiving the same pulse. As Q1 is turned off, turn-on delay time is required before S1 comes into the on-state. Hence, S1 and S2 are on simultaneously for a certain time. While S2 is turned off, turn-on delay time is also needed before Q2 is turned on. Such a process leads Q2 and S1 to turn on simultaneously for the rest of the cycle period. The line to line output voltage Vab waveform with three positive voltage steps (0, +Vdc/2, +Vdc) is depicted in Figure 6c. Figure 6d shows the three balanced line to neutral voltages VaN, VbN, and VcN waveforms with ($\frac{2\pi}{3}$) phase shifted. Furthermore, as the proposed inverter is designed to deliver an output power of 0.7 KW to a fixed resistive-inductive load, the PWM modulation technique is employed at modulation index Ma = 1, and the operating switching frequency is set at 4 kHz. Both commutation strategies COM1 and COM2 are used to investigate the performance of the suggested inverter at medium switching frequency. The efficiency of the proposed system is measured by means of power analyzer where the output voltage is raised with small steps. Figure 7a depicts the inverter output line to line and line to neutral voltage waveforms. The output powers delivered from the proposed inverter with corresponding efficiencies measured with COM1 and COM2 are shown in Figure 7b. It can be seen that

the efficiency of the proposed inverter measured with COM2 is slightly higher than that measured with COM1. This difference is caused by the additional losses generated in COM1, where the higher switching frequency used leads to an increase in switching losses and decrease in the converter efficiency.

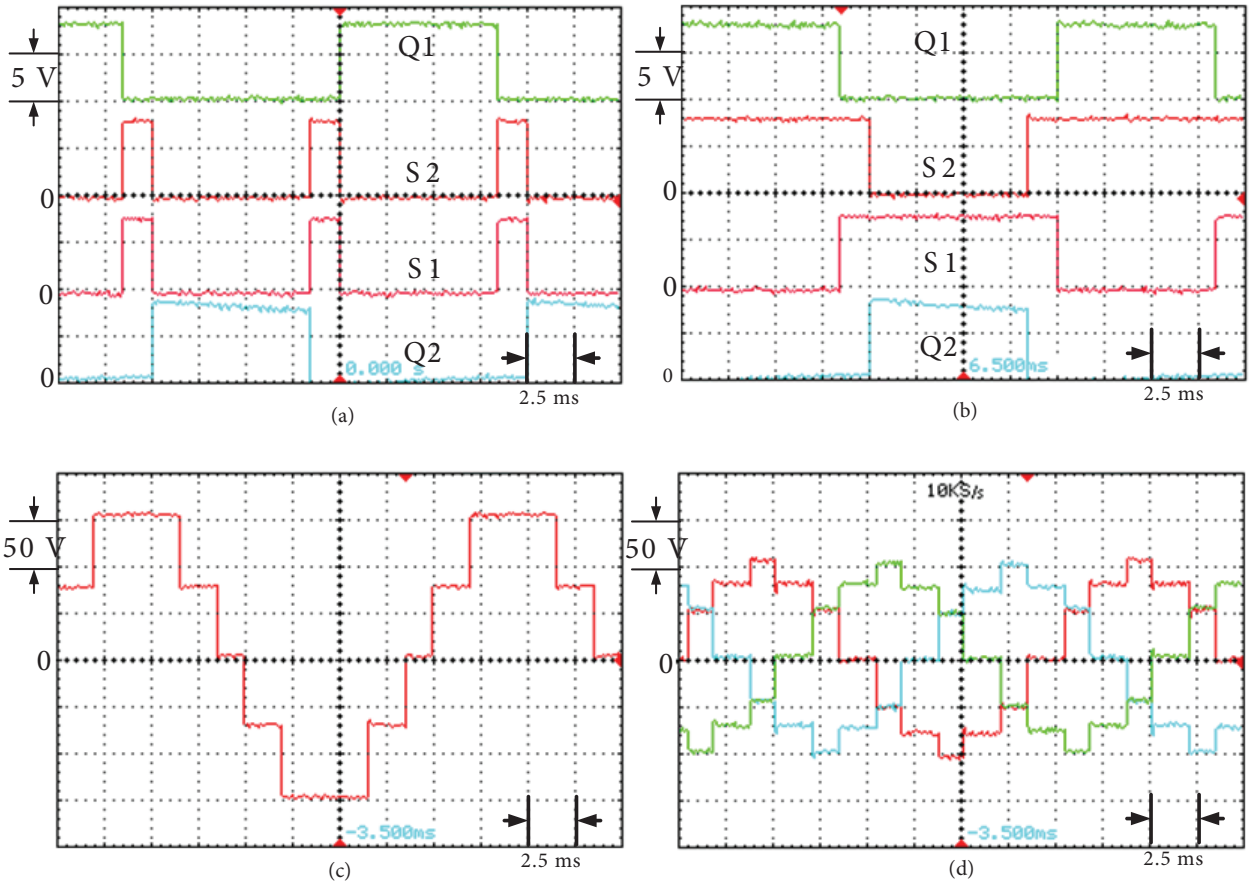

Figure 6. a) Switches' gate signals with COM1, b) switches' gate signals with COM2, c) line to line voltage *Vab*, and d) line to neutral voltages *VaN*, *VbN*, and *VcN*.

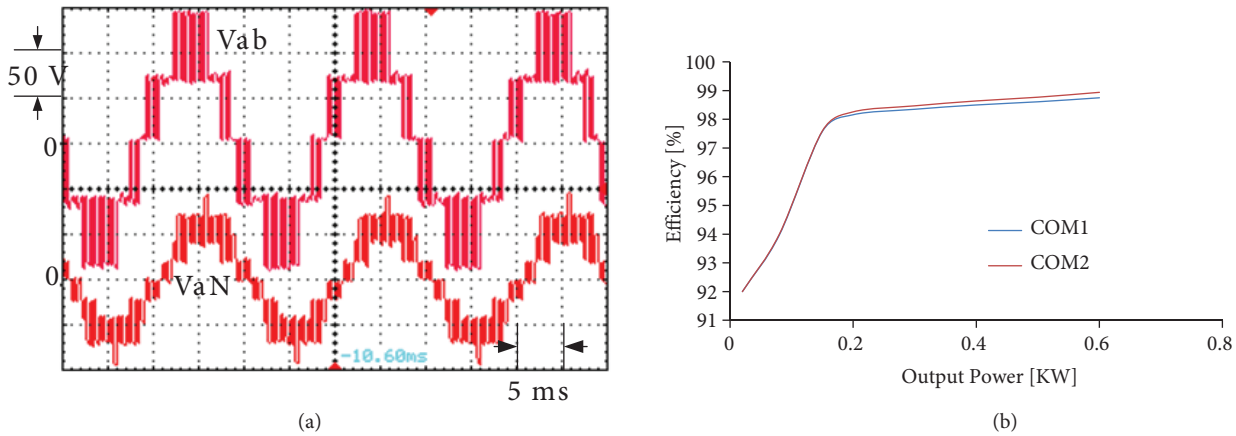

Figure 7. a) Line to line voltage *Vab* and line to neutral voltages *VaN* at (Ma = 1) and (fc = 4 kHz), b) output power vs. efficiency with COM1 and COM2.

6. Conclusion

In this paper, a new three-phase three-level multilevel inverter was introduced. The three added bidirectional switches were designed in such a way that two different commutation strategies can be implemented to achieve the desired output voltage. These two commutation strategies were illustrated, analyzed, and compared in terms of switching loss generated. The comparison has shown that the proposed inverter's efficiency is improved during its operation with one of these strategies. Furthermore, in order to verify the performance of the proposed multilevel inverter, its power circuit was manufactured and tested under low voltage. The suggested commutation strategies have showed high compatibility with the suggested topology as low and medium switching frequencies are used. The experimental results have ensured the feasibility of the proposed inverter and its capability in minimizing the total power loss and increasing the efficiency.

List of symbols:

N	number of levels
Sa, Sb, Sc	switching state variables
$Pcon$	conduction loss
Psw	switching loss
Pt	total losses
$Eon(t)$	turn-on loss
$Eoff(t)$	turn-off loss
Von_IGBT	IGBT forward voltage drop
Von_diode	diode forward voltage drop
$Pout$	output power
T	switching interval
$\eta\%$	inverter's efficiency
fc	carrier frequency
PF	power factor
COM1	first commutation strategy
COM2	second commutation strategy

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