

## A 2.4-GHz highly linear derivative superposition Gilbert cell mixer

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**Abstract:** This paper presents a new derivative superposition Gilbert cell to minimize the third-order nonlinear current term of transconductance transistors. To decrease the parasitic capacitance effect on gain, noise figure, and linearity of the circuit, extra inductors and capacitors are added between the switching and transconductance stages. The proposed mixer is simulated in 0.18- $\mu\text{m}$  RF-CMOS technology with a 1.8-V supply. The results show an improvement of about 23 dBm in IIP3 compared to conventional mixers. The power consumption of this circuit is about 3.96 mW.

**Key words:** CMOS, common source mixer, highly linear, derivative superposition technique, transconductance stage

### 1. Introduction

Nowadays, the requirement for higher speed and longer battery life for communication is a must. Most wireless communication systems work with a 2.4-GHz frequency, called the ISM band, that has many protocols for different purposes, such as Bluetooth and IEEE 802.11b standards [1,2].

One of the most important parts of wireless communication systems is the RF front-end receivers. The requirement of linearity performance for a mixer becomes more important in RF front-end receivers, which influence the linearity of the whole system. The above requirement demands a trade-off with power supply [3]. Therefore, it is a great challenge to achieve high linearity at low power.

The mixer is one of the significant blocks of these receivers. A double-banded Gilbert cell is used as an active mixer. The Gilbert mixer has three stages: the transconductance stage, switching stage, and load stage. The linearity of this cell will be controlled by the transconductance stage. The transconductance stage can be made by common-gate or common-source configurations. Most common-gate structures present wider bandwidth compared to the common-source structure that tolerates a higher gate source capacitor [4].

So far, few linearization techniques have been proposed using CMOS processes in the transconductance stage of the RF mixer. The most effective linearization method is a derivative superposition (DS) technique [5,6]. This method cancels the negative third-order derivative of the transconductance stage by combining transistors with positive and negative second-order gm derivation ( $g''_m$ ) to achieve an overall zero  $g''_m$  [5–8].

This paper deals with the design of highly linear Gilbert cell. A new modified DS scheme is introduced for the Gilbert cell in common-source structures. In this scheme, auxiliary PMOS and NMOS transistors are used in the transconductance stage of the mixer in order to decrease the nonlinear current that is generated by transistors of this stage. As a result, the new modified DS can increase the IIP3 by canceling the third-order effects.

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This paper is organized as follows. A new modified DS technique and distortion analysis are described in Section 2. The proposed mixer and simulation results are presented in Section 3, 4, and 5. Finally, the discussion and conclusion are given in Sections 6 and 7.

## 2. New derivative superposition technique

Nonlinearity of the common-source structure in the MOSFET transistor is mainly due to the transconductance ( $g_m$ ) nonlinearity. The small-signal drain currents of this structure can be expressed by using the Taylor series [9].

$$i_d = g_m v_{gs} + \frac{g'_m}{2!} v_{gs}^2 + \frac{g''_m}{3!} v_{gs}^3 + \dots \quad (1)$$

Here,  $v_{gs}$  is a small-signal gate-to-source voltage and  $g_m^n$  shows  $n$ th order transconductance with regard to  $V_{gs}$ . In determining the third-order intermodulation distortion (IMD) of an RF amplifier, the coefficient of  $V_{gs}^3$  in Eq. (1) has a significant role [10].

Figure 1a shows the new DS technique with PMOS and NMOS transistors [11]. Based on this figure, Eq. (1) can be written for these 3 transistors as follows.

$$i_n = -g_{mn} v_X + \frac{g'_{mn}}{2} v_X^2 - \frac{g''_{mn}}{6} v_X^3 + \dots \quad (2)$$

$$i_p = -g_{mp} v_1 + \frac{g'_{mp}}{2} v_1^2 - \frac{g''_{mp}}{6} v_1^3 + \dots \quad (3)$$

$$i_t = g_{mt} v_1 + \frac{g'_{mt}}{2} v_1^2 + \frac{g''_{mt}}{6} v_1^3 + \dots \quad (4)$$

Here,  $v_1 = v_{gs}$ . Based on the power series, the voltage of the drain and gate are related together:

$$v_X = C_1 v_1 + C_2 v_1^2 + C_3 v_1^3 + \dots \quad (5)$$

Here,  $C_1$ ,  $C_2$ , and  $C_3$  are frequency-dependent. Substituting Eq. (5) into Eq. (2) shows that the current of the NMOS transistor Mn will be:

$$i_n \approx -(C_1 g_{mn}) v_1 + (-C_2 g_{mn} + C_1^2 \frac{g'_{mn}}{2}) v_1^2 + (-C_3 g_{mn} + 2C_1 C_2 g'_{mn} - \frac{g''_{mn}}{6} C_1^3) v_1^3 \quad (6)$$

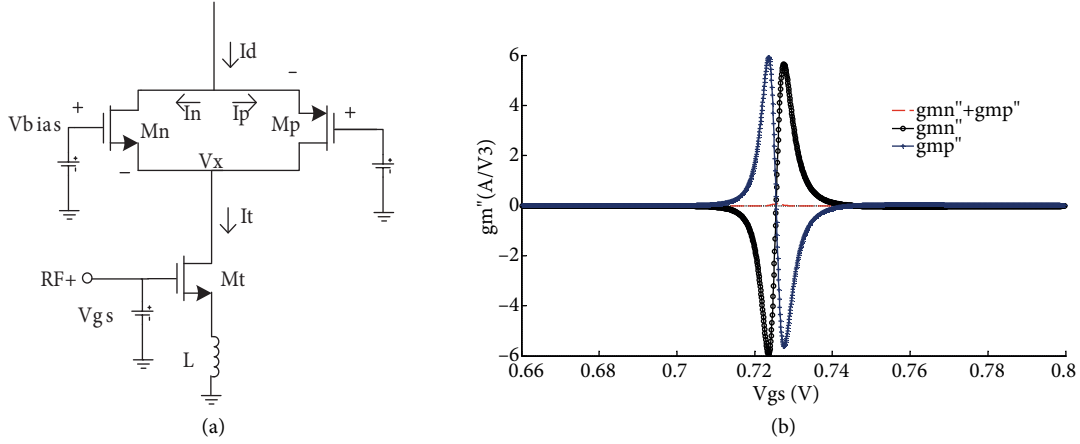
Also, KCL in the X node is:

$$i_t = i_n + i_p \quad (7)$$

Placing Eq. (3) and Eq. (6) into Eq. (7), the total current is:

$$\begin{aligned} i_t = & (-g_{mp} - C_1 g_{mn}) v_1 + (\frac{g'_{mp}}{2} + C_2 g_{mn} + C_1^2 \frac{g'_{mn}}{2}) v_1^2 \\ & + \left( -\frac{g''_{mp}}{6} - C_3 g_{mn} + 2C_1 C_2 g'_{mn} - \frac{g''_{mn}}{6} C_1^3 \right) v_1^3 \end{aligned} \quad (8)$$

Here,  $C_1$  and  $C_3$  have negative values, so  $g''_{mt}$  is approximately  $g''_{mt} \approx -\frac{g''_{mp}}{6} - \frac{g''_{mn}}{6} C_1^3$ .



**Figure 1.** a) A new derivative superposition method, b) third nonlinear currents of Mt, Mp, and Mn transistors.

Using the current relations of the MOS transistor in the saturation region:

$$I = K \frac{(V_{GS} - V_{th})^2}{1 + \theta(V_{GS} - V_{th})} (1 + \lambda V_{DS}) \quad (9)$$

Here,  $K = \frac{\mu_{eff} C_{ox}}{2} (W/L)$ ,  $\mu_{eff} = \frac{\mu_0}{1 + E/E_c}$ , and  $\theta = \frac{1}{LEC}$ .  $L$  is the device channel length,  $\lambda$  is the output impedance constant,  $\mu_0$  is the low-field mobility,  $E$  is the longitudinal electric field, and  $E_c$  is the critical electric field [12]. If  $M = V_{GS} - V_{th}$ , Eq. (9) will be:

$$I \cong K \frac{M^2}{1 + \theta M} \quad (10)$$

Calculating  $g_m$ ,  $g'_m$ ,  $g''_m$ , Eq. (8) can be changed:

$$\begin{aligned} i_t = & \left( -\frac{2M_p + \theta_p M_p^2}{(1 + \theta_p M_p)^2} - C_1 \frac{2M_n + \theta_n M_n^2}{(1 + \theta_n M_n)^2} \right) v_1 \\ & + \left( \frac{1}{(1 + \theta_p M_p)^3} + C_2 \frac{2M_n + \theta_n M_n^2}{(1 + \theta_n M_n)^2} + C_1^2 \frac{1}{(1 + \theta_n M_n)^3} \right) v_1^2 \\ & + \left( \frac{\theta_p}{(1 + \theta_p M_p)^4} - C_3 \frac{2M_n + \theta_n M_n^2}{(1 + \theta_n M_n)^2} \right. \\ & \left. + 2C_1 C_2 \frac{1}{(1 + \theta_n M_n)^3} + \frac{\theta_n}{(1 + \theta_n M_n)^4} C_1^3 \right) v_1^3 \end{aligned} \quad (11)$$

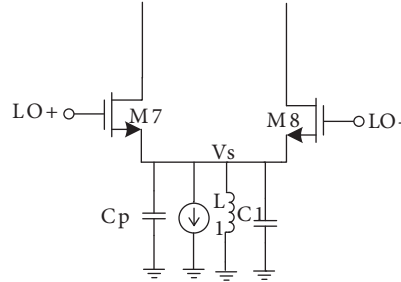
The constant factor of  $V_1^3$  term is  $g''_{mt}$ , which is:

$$\begin{aligned} g''_{mt} = & \frac{\theta_p}{(1 + \theta_p M_p)^4} - C_3 \frac{2M_n + \theta_n M_n^2}{(1 + \theta_n M_n)^2} \\ & + 2C_1 C_2 \frac{1}{(1 + \theta_n M_n)^3} + \frac{\theta_n}{(1 + \theta_n M_n)^4} C_1^3 \\ \approx & \frac{\theta_p}{(1 + \theta_p M_p)^4} + \frac{\theta_n}{(1 + \theta_n M_n)^4} C_1^3 \end{aligned} \quad (12)$$

Therefore, the coefficient of third-order transconductance can be zeroed by adjusting the size of transistors and their biasing points (Figure 1b).

Figure 1b shows the linearization of the derivative superposition scheme. Based on this circuit, one transistor is biased in a weak region to achieve positive  $g_m''$  and the other transistor is biased in a strong region to achieve negative  $g_m''$ . As a result, the  $g_m''$  values of two transistors are summed up to zero, so the third-order distortions are canceled and IIP3 is adequately improved.

Parasitic capacitances of the gate source of transistors M3 and M4 are  $C_1$  and  $C_2$ , respectively, and the total capacitance from the common-source node to ground  $C_P$  consists of the source-bulk capacitance of M3 and M4 and the drain-bulk capacitance of M1, as shown in Figure 2 [13].



**Figure 2.** Applying LC to source of LO stage.

The small signal current  $I_t(t)$  is given by [13]:

$$I_t = GV + G_v V^2 + G_{vv} V^3 + \frac{d}{dt} (Cv + C_v V^2 + C_{vv} V^3) \quad (13)$$

Here,  $I_t$  is a function of overdrive voltage of switching transistors.  $G$ ,  $G_v$ , and  $G_{vv}$  are a function of transconductance and  $C$ ,  $C_v$ , and  $C_{vv}$  are the first and second derivatives of the switching stage capacitances.

Adding  $L_1$  and  $C_1$  to this schematic, the Eq. (13) can be changed:

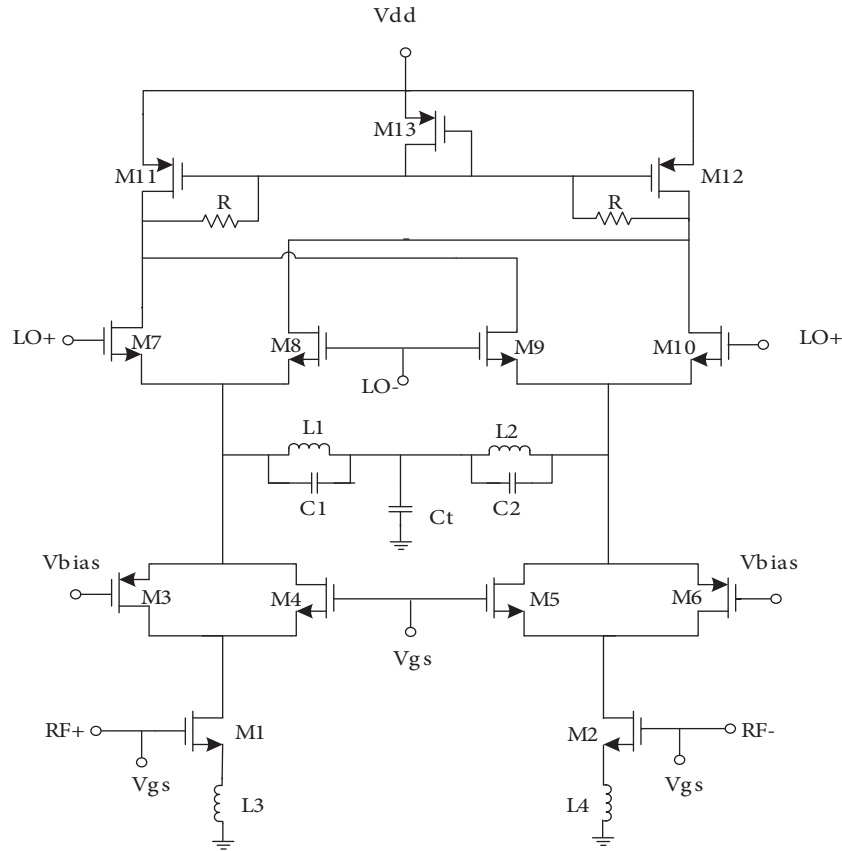
$$I_t = GV + G_v V^2 + G_{vv} V^3 + \frac{d}{dt} (CV + C_v V^2 + C_{vv} V^3) + \int \frac{(-V)}{L_1} dv + C_1 \frac{d}{dt} (-V) \quad (14)$$

According to Eq. (9), the nonlinearity effect of gate-source capacitors can be reduced by choosing proper values of  $C$  and  $L$ .

### 3. Proposed mixer

Figure 3 shows the complete proposed highly linear mixer. In this mixer, the common source configuration is a major source of IMD. The nonlinear current that was generated in the common source structure is absorbed by a common gate transistor.

M1 and M2 transistors are sized  $(7/0.18\mu m) \times 12$  for input matching. The size of the auxiliary PMOS transistors (M3 and M6) considered is  $(8/0.18\mu m) \times 11$  and they are biased with 1.8 V, and the size of the auxiliary NMOS transistors considered is  $(8/0.2\mu m) \times 22$ . The switching transistors M7–M10 are sized  $(8/0.18\mu m) \times 12$  and are driven by 14dBm local oscillator power. The size of the load transistors (M11 and M12) considered is  $(8/0.18\mu m) \times 10$ . M13 is sized  $(2/0.18\mu m) \times 1$  as the current bias of load transistors. The value of auxiliary  $L$  and  $C$  that are used in this mixer are respectively 1.233 nH and 3.515 pF.



**Figure 3.** The proposed mixer.

#### 4. Simulation results

The proposed mixer was designed with 0.18- $\mu\text{m}$  CMOS technology with 1.8-V supply voltage. The results were simulated with the Advance Design System (ADS) simulator. For all simulation and measurement results, the RF frequency is 2.4 GHz, the local oscillator (LO) frequency is 2.3 GHz, and the output frequency is 100 MHz.

The simulation shows that by using auxiliary PMOS and NMOS transistors in the transconductance stage, the IIP3 is 26 dBm at 2.4 GHz, as shown in Figure 4a.

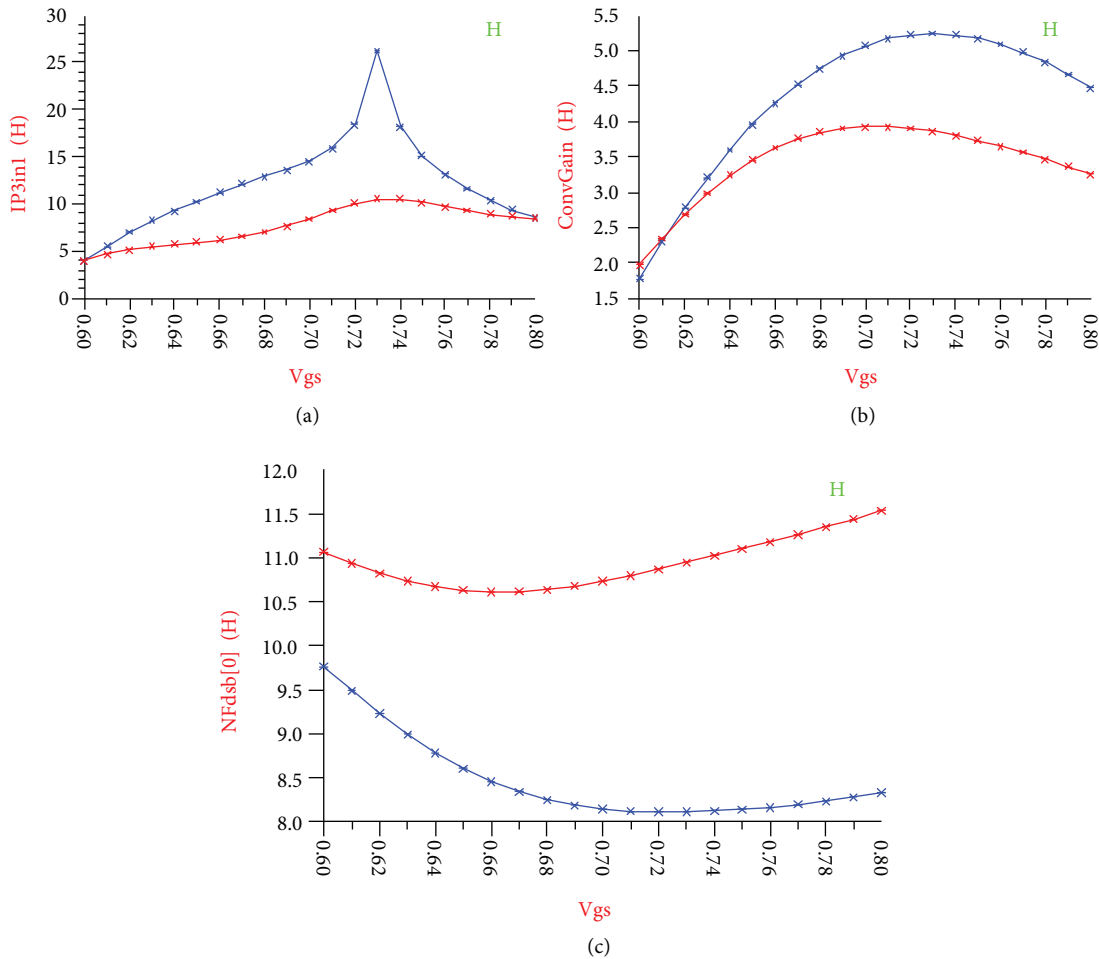
For simulating the effect of matching and threshold variation, the bias point of M1 is considered to be equal to M4. In Figure 4a the IIP3 vs.  $V_{gs}$  of M1, M3, and M4 is shown. Referring to Figure 4b, the conversion gain at  $V_{gs} = 0.73$  V is equal to 5.3 dB using 2.2 mA from the 1.8-V supply. Impedance matching of the RF and LO ports is  $50\ \Omega$ .

Utilizing the LC stage, the conversion gain and noise figure (SSB) are improved by 2 dB and 5 dB, respectively (Figures 4b and 4c).

Mixer performance summary and comparisons with four proposed designs are given in the Table.

#### 5. Postlayout simulation results

The proposed mixer is simulated by Cadence SpectreRF using the TSMC 0.18- $\mu\text{m}$  1P6M RF CMOS process (Figure 5). The size of the proposed mixer is  $750\ \mu\text{m} \times 375\ \mu\text{m}$ .



**Figure 4.** a) Simulation of linearity performance of the proposed ( $\times$ ) and conventional mixer with ADS ( $\times$ ); b) simulation of conversion gain with ( $\times$ ) and without LC stage with ADS ( $\times$ ); c) simulation of noise figure with ( $\times$ ) and without LC stage with ADS ( $\times$ ).

**Table.** Comparison of mixer performance.

	This work	[9]	[14]	[15]	[16]
Process	0.18 $\mu$ CMOS	0.18 $\mu$ CMOS	0.18 $\mu$ CMOS	0.18 $\mu$ CMOS	0.18 $\mu$ CMOS
RF freq.	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz	2.4 GHz
Gain	5.3 dB	16.5 dB	6.2 dB	11.08 dB	6.3 dB
IIP3	+26 dBm	+9 dBm	-4.4 dBm	+13.6 dBm	+13.4 dBm
NF	8.1 dB	14.2 dB	12.8 dB	14 dB	—
Voltage	1.8 V	1.8 V	1.8 V	1.8 V	1.2 V
Power	3.96 mW	5.4 mW	3.3 mW	3.99 mW	4.8 mW

The LO power and RF power are 13 dBm and -25 dBm, that is used to drive the switching and transconductance stages, respectively. Figure 6a shows the measurement result of conversion gain, with different gain-to-source voltage in the transconductance stage. When the input  $V_{gs}$  is 0.73, conversion gain is 7.9 dB. There is 2.6 dB of difference in gain between simulation and postlayout results. Figure 6b depicts the double

sideband (DSB) noise figure (NF) versus  $V_{gs}$ . Noise figure, which is 7.1 dB, i.e. 1 dB lower than the simulation result with ADS.

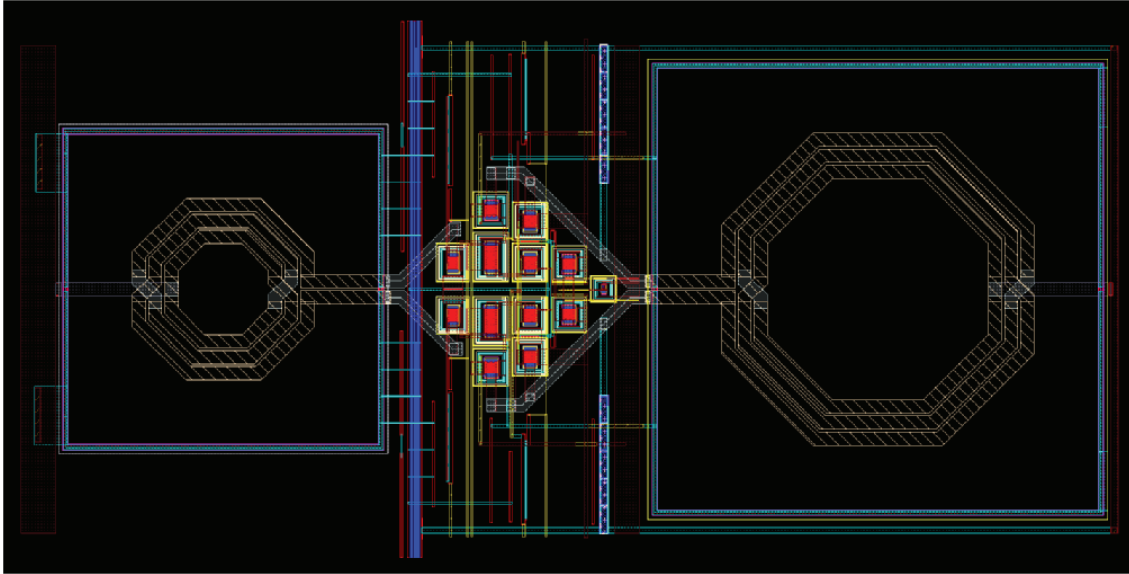


Figure 5. Postlayout view of proposed mixer.

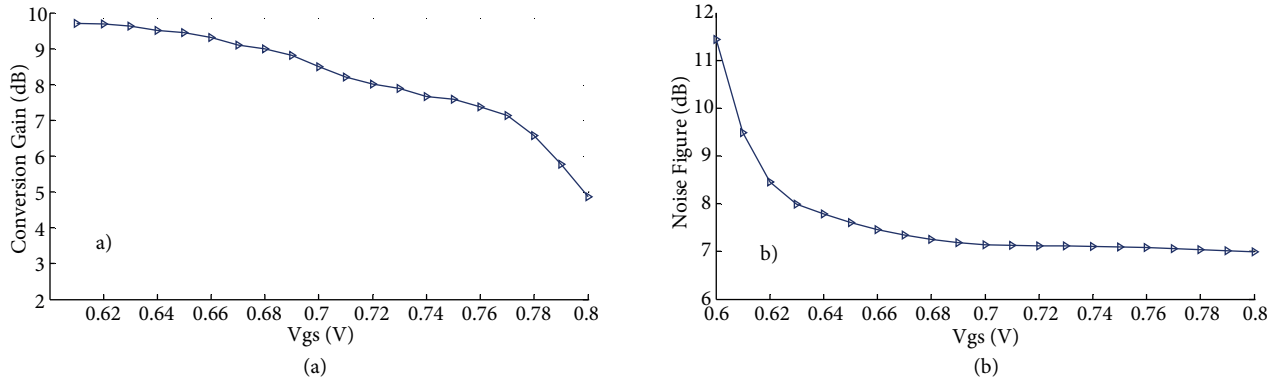


Figure 6. a) Postlayout simulation of conversion gain with cadence; b) postlayout simulation of noise figure with cadence.

The third-order intermodulation intercept point (IIP3) of the proposed mixer is 22 dBm, as shown in Figure 7. The postlayout result of IIP3 is 4 dBm lower than in the mixer simulation.

## 6. Discussion

A new derivative superposition common source mixer is designed with  $0.18\text{-}\mu\text{m}$  RF-CMOS technology in 2.4-GHz frequency. In this linearization technique, using the derivative superposition method, the  $g_m''$  of the transconductance stage of NMOS is canceled by summation of the  $g_m''$  of both the PMOS and NMOS auxiliary stages. Thus, the IIP3 can be improved significantly by using this method rather than conversion mixers.

The nonlinearity effect of gate-source capacitors in the switching stage can be decreased by adding extra inductors and capacitors in parallel between transconductance and switching stages to improve conversion gain. Therefore, it will be boosted with noise figure reduction in comparison to a non-LC stage configuration.

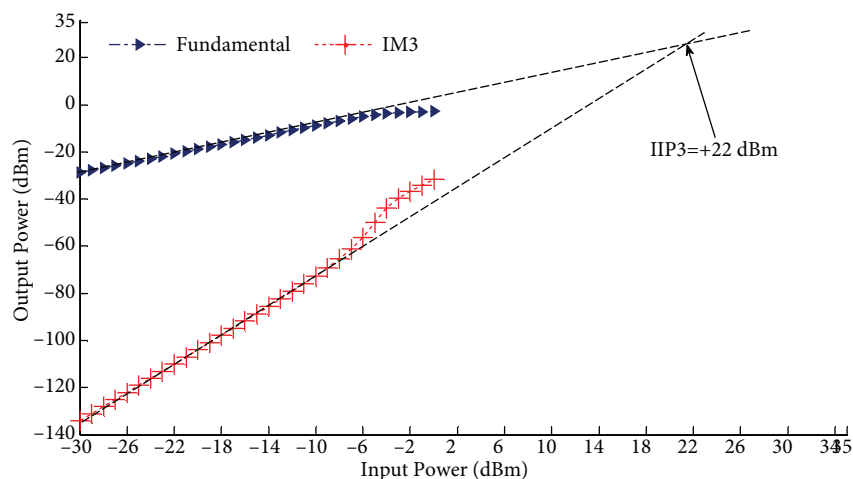


Figure 7. Input third-order intercept point @ IF frequency = 100 MHz.

## 7. Conclusion

In this paper, we have tried to show results with computer simulation and layout. All measurements prove that the derivative superposition method can be suitable for use in a Gilbert cell mixer, because the linearity of almost all mixers is controlled by the RF stage. Whereas the linearity of the mixer directly affects other parts of the front-ended receivers, by using the DS method, we can improve the linearity of them.

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