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A new single stage single phase power factor corrected and isolated AC-DC converter based on resonance and soft switching

Hacı BODUR, Erdem AKBOY*, İsmail AKSOY
Department of Electrical Engineering, Faculty of Electrical and Electronics Engineering,
Yıldız Technical University, İstanbul, Turkey

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Abstract: In this paper, a new single stage single phase power factor corrected and isolated AC-DC converter based on resonance and soft switching (SS) is presented. In fact, a new concept for power factor corrected converter is proposed in this study. This converter provides power factor correction (PFC) by using a switch and a fully resonant circuit. It also provides regulated and isolated output voltage with direct power transfer by using a second switch and forward and flyback topologies based on resonance. Both switches in the converter are controlled with the same closed loop and the time multiplexing, and are switched with soft switching dominantly because of resonance. The input or PFC switch is turned on and off under zero current switching (ZCS) due to the resonant circuit. The output switch is turned on with ZCS due to resonance, and unfortunately is turned off with hard switching. The operation principle, detailed steady state analysis, and design procedure of the new PFC converter are presented. The theoretical analysis is verified by a prototype of the new converter using 125 W and 100 kHz.

Key words: Power factor correction, soft switching, direct power transfer

1. Introduction

Use of electrical appliances and so energy consumption has been increasing with the effect of technological developments. Therefore, energy should be used more efficiently. Nonlinear loads such as uninterrupted and switching mode power supplies and electronic ballasts draw harmonic currents, and so cause deteriorations in the grid. Electronic devices such as personal computers and microprocessors that are fed from the same grid could be affected negatively by reason of these harmonics. Thus, energy should be used in a quality manner too. There are international mandatory standards about power factor and harmonics in terms of the use of energy with high quality and efficiency. Therefore, to cope with these standards power factor correction (PFC) circuits have been increasing in importance in both academic and industrial studies [1–20].

PFC techniques such as passive and active filters have been studied for many years. Due to the complicated structure and high price of active ones and the bulky structure of passive ones [1], the attention on high frequency AC-DC converters has been increasing. These converters can be realized by a two stage approach or a single stage approach. Two stage PFC circuits, which consist of input current shaper and output voltage regulation stages, are commonly used in high power applications. Although they have superior performance in terms of PFC and output voltage regulation due to their separate control structure, they have a complex structure and low efficiency owing to the fact that both stages process total input power [2,3].

*Correspondence: eakboy@yildiz.edu.tr

To overcome these drawbacks of two stage schemes, various single stage PFC converters have been presented [4–20]. The PFC and output voltage regulation stages are combined into one stage generally using only one switch. Thus the attention on single stage PFC circuits has been increasing for low power applications due to their simpler control structure and circuitry scheme. Although they have the aforementioned advantages, total power is processed through output twice as two stage ones in some single stage PFC circuits. Therefore, efficiency is dramatically low in such kinds of single stage PFC circuits [12].

The direct power transfer (DPT) technique, in which most of the input energy is processed through output at once, provides high efficiency. In this sense, several single stage PFC circuits have been presented [4–9,11–13,16–20]. An ideal DPT scheme is presented in Figure 1 for single phase PFC converters. It is explained in [4] that 68% of the total input power is transferred to output directly and the remaining power is transferred to the output twice to achieve output voltage regulation. In [4] and [5] PFC and DPT are achieved by different combinations of flyback and boost topologies. These circuits suffer from excessive magnetic components and semiconductors, and complex control scheme and circuit structure. Also there are hard switching and switching losses because of operating in continuous current mode (CCM). A new DPT approach in which the features of flyback and boost converters were merged in only one transformer was presented in [6]. PFC is achieved by operating in discrete current mode (DCM) in both boost and flyback modes. Although a single switch is used, two bulky capacitors are used in some implementations.

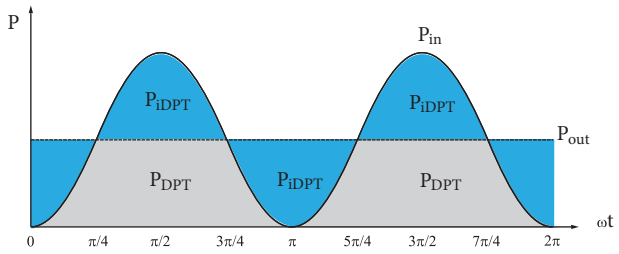

Figure 1. Power relationship in ideal DPT idea.

On the basis of the DPT concept, there are other topologies such as forward [16,17] and flyback converters [18,19]. In circuits in which a forward converter is the main converter, the DPT idea cannot be realized when the main voltage is lower than the reflected voltage on the primary side of the transformer [16,17]. In [16], PFC was dependent on the load. Although the line current waveform is similar to sinusoidal with light loads, it becomes a square wave with heavy loads. Moreover, a safety problem occurs in this circuit; hence there is no isolation between the bulky capacitor and the output. There is no dead angle due to flyback operating of the proposed circuit when the line voltage is low [17]. In spite of this advantage, there are line current deteriorations in low main voltage applications.

There is another topology in which the DPT idea is accomplished by a flyback converter [18]. In this circuit there are two operation modes in one switching period concerning line voltage value. When the line voltage is high, as the majority of input energy is processed to output by flyback topology, the remaining energy is processed to the auxiliary capacitor firstly by forward topology and then is processed to output for output voltage regulation by DC-DC flyback topology. In this mode, the line current is not proportional to the main voltage because of forward operation and so the current wave is not sinusoidal exactly. It could be solved by increasing DPT, resulting in higher auxiliary capacitor voltage. Thus, PFC is dependent on converter topology. In the other mode, in which the line voltage is low, output is supplied by input and an auxiliary capacitor,

both operating as flyback converters. Although DPT is achieved by an AC-DC flyback converter operating in DCM, the line current wave is still nonsinusoidal. Furthermore, in this circuit both switches turn off under hard switching, which causes switching losses.

The present paper proposes a new converter topology for single stage PFC based on resonance and soft switching (SS). The time multiplexing control scheme is used for both switches. Therefore, the output voltage regulation and DPT at output and PFC at input are achieved by frequency modulation while the duty cycle is constant. At the PFC stage, the waveform of the current drawn from the line is sinusoidal and its peaks are proportional to the line voltage waves, and so PFC and SS are obtained by using a fully resonant circuit. In the regulation stage, the converter construction works as a flyback or forward concerning line voltage value by way of a transformer, and so DPT, isolation, and regulation are obtained. Moreover, the voltage and current stresses on the semiconductor devices are kept at reasonable levels in the converter.

2. Operational principle and analysis

2.1. Definitions and assumptions

A new single stage single phase PFC converter with resonance and SS is presented in Figure 2. This circuit has been improved from the simulation study in [21] and an experimental circuit is achieved. In this circuit, V_{AC} and i_{AC} are main voltage and current, V_i and i_i are rectified voltage and current, and V_o and i_o are output voltage and current. This circuit consists of rectifier diodes D_1–D_4, the other diodes D_5–D_{11}, PFC or input switch S_1 and output switch S_2, transformers T_1 and T_2, resonance inductor L_r, resonance capacitor C_r, forward inductor L_F, storage capacitor C_B, and output capacitor C_o. Moreover, a_{11} and a_{12} are the turns ratios between primary and secondary windings of T_1, while a_2 is the turns ratio of T_2.

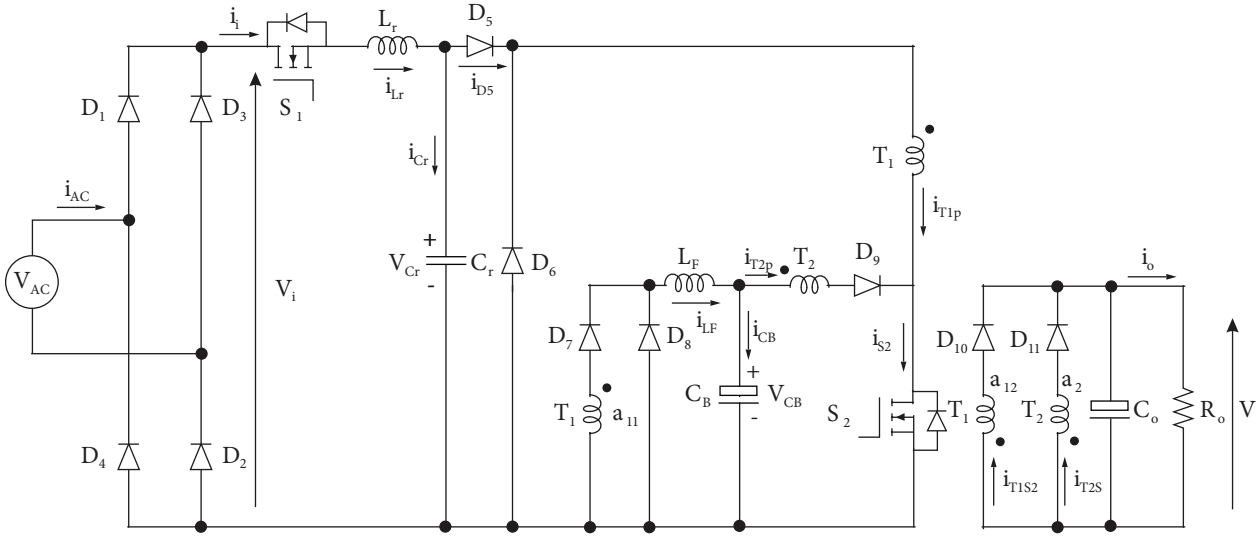

Figure 2. Proposed single stage single phase PFC converter with resonance and soft switching.

For one switching cycle, the following assumptions are made in order to simplify the steady state analysis of the proposed PFC converter. Main voltage V_{AC}, input voltage V_i, output voltage V_o, and storage capacitor voltage V_{CB} are constant and all semiconductors, inductors, capacitors, and transformers are ideal.

2.2. Operation principle

During the positive resonance period, S_1 is on and resonance occurs between L_r and C_r. In this period, C_r is charged by resonance current that is drawn from the grid and is sinusoidal. Then C_r is discharged through S_2 and primary winding of T_1 in the negative resonance period. The operation modes of transformers T_1 and T_2 are given in Figure 3.

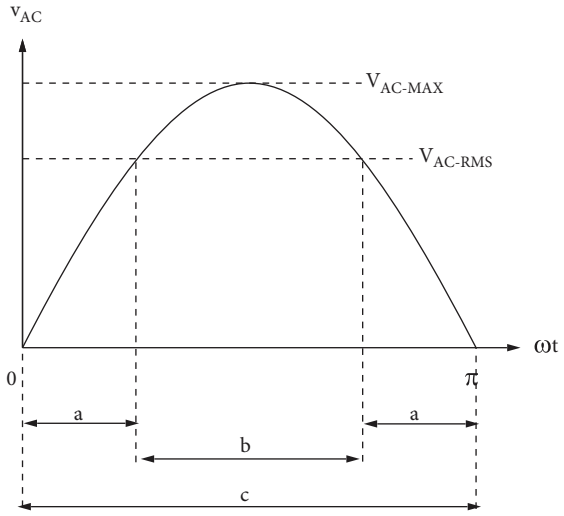

Figure 3. Operation modes of transformers depending on the main voltage: (a) T_1 operates only as a flyback transformer, (b) T_1 operates as both forward and flyback transformer, (c) T_2 always operates as a flyback transformer.

Here, T_2 provides output voltage regulation as operating flyback transformer. The energy stored in T_2 while S_2 is on is transferred to the output while S_2 is off. For the operating of T_1, two modes occur concerning the value of the main voltage. If the main voltage is higher than its rms value, Mode 1 occurs, as shown in Figure 3b. In this mode, T_1 operates as a forward transformer and most of the energy in C_r is transferred to the storage capacitor C_B. The remaining energy in C_r is transferred to the output by flyback operating of T_1. If the main voltage is lower than its rms value, Mode 2 occurs, as shown at Figure 3a. In this mode, T_1 operates as a flyback transformer and the energy stored in C_r is transferred to the output directly.

MODE 1

For this operation mode, six stages occur over one switching period. The equivalent circuit schemes of operation stages are given in Figure 4. The key waveforms concerning the operation stages are shown in Figure 5.

Stage 1 ($t_0 < t < t_2$: Figure 4a): Before this stage all switches are in the off state. At the moment $t = t_0$, $v_{Cr} = 0$, $i_{Lr} = 0$, $i_{T1p} = 0$, $i_{T2p} = 0$, $i_{LF} = 0$, $i_{T1S2} = I_{T1S20}$, and $i_{T2S} = I_{T2S0}$ are valid. When the control signal is applied to the gate of S_1, resonance starts between L_r and C_r via V_i. For this resonance, the following equations are obtained:

$$i_{Lr} = i_{S1} = \frac{V_i}{Z_1} \sin\left(\omega_1 \left(t - t_0\right)\right) \tag{1}$$

$$v_{Cr} = V_i \left(1 - \cos\left(\omega_1 \left(t - t_0\right)\right)\right) \tag{2}$$

$$v_{Cr} = V_i \left(1 - \cos\left(\omega_1 \left(t - t_0\right)\right)\right) \tag{3}$$

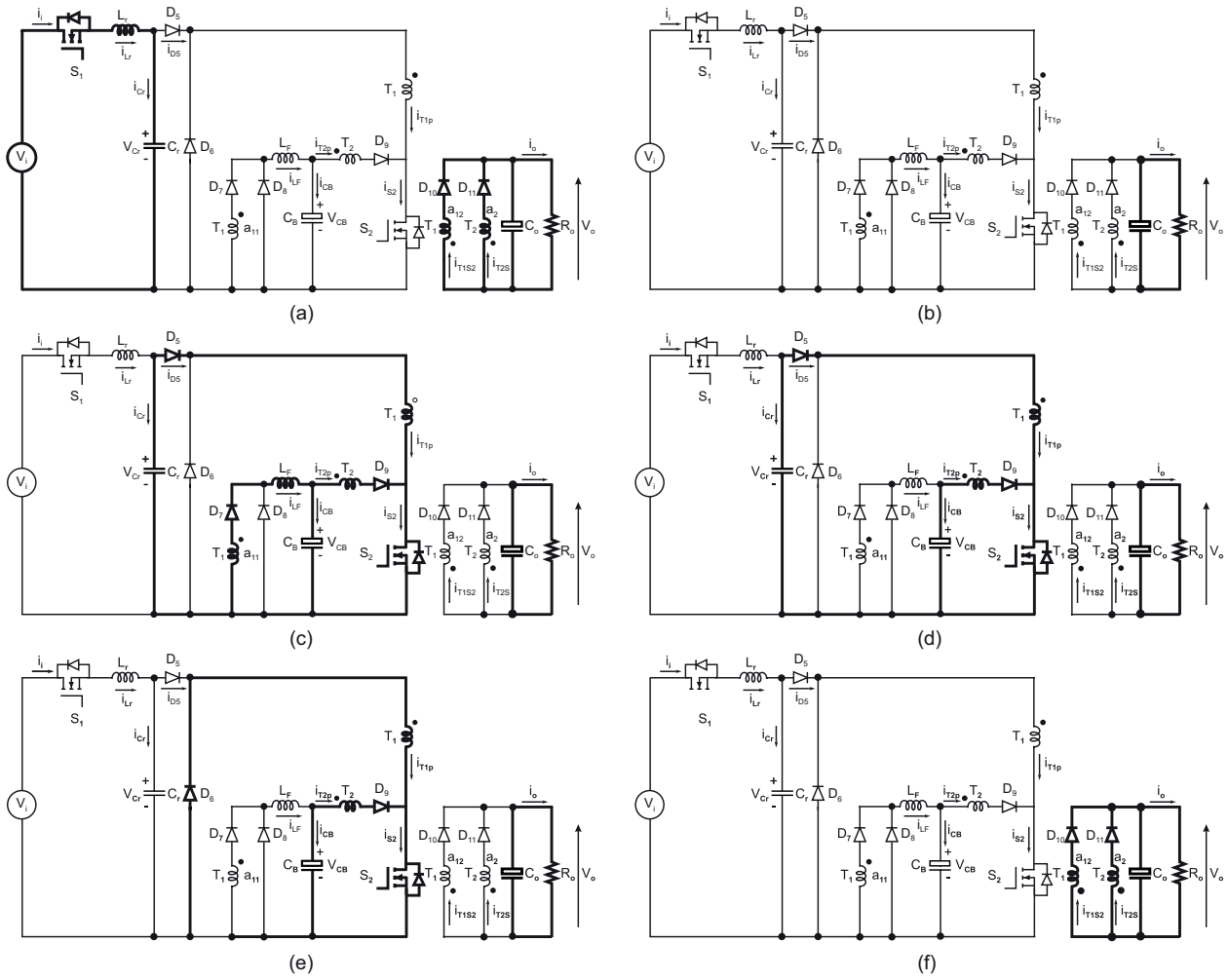

Figure 4. Equivalent circuit schemes of the operation stages of Mode 1.

$$I_{Lr\max} = \frac{V_i}{Z_1}$$

$$t_{02} = \pi\sqrt{L_r C_r} \tag{4}$$

In these equations,

$$\omega_1 = \frac{1}{\sqrt{L_r C_r}} \tag{5}$$

$$Z_1 = \omega_1 L_r = \frac{1}{\omega_1 C_r} = \sqrt{\frac{L_r}{C_r}} \tag{6}$$

are valid. In this stage, the current i_{Lr} is sinusoidal, reaches at its maximum value at t_1, and decreases to zero at t_2. C_r is charged to $2V_i$ value at the end of this stage. The maximum value of L_r current is proportional to the instantaneous value of the line voltage. In addition, the switch S_1 and the diodes D_1–D_4 are turned on and off with ZCS due to resonance at this stage.

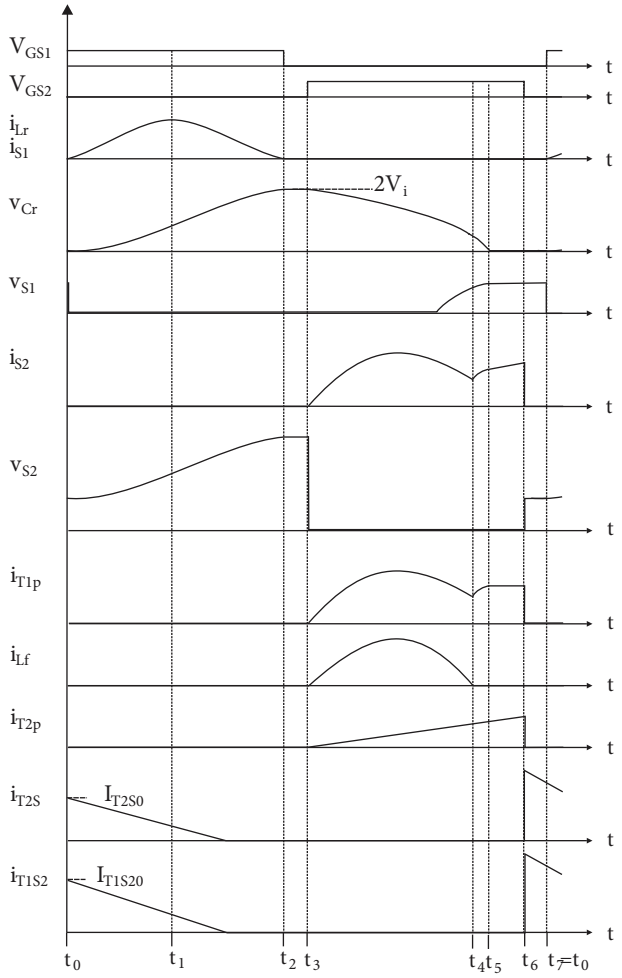

Figure 5. Key waveforms concerning the operation stages of Mode 1.

Moreover, at this stage, the magnetization energies of T_1 and T_2 transformers are transferred to the output through D_{10} and D_{11}. For this stage, the following equations can be written:

$$i_{T1S2} = i_{D10} = I_{T1S20} - \frac{V_0}{L_{1S2}}(t - t_0) \tag{7}$$

$$i_{T2S} = i_{D11} = I_{T2S0} - \frac{V_o}{L_{2S}}(t - t_0) \tag{8}$$

Before the end of this stage, the currents i_{T1S2} and i_{T2S} become zero, and so the diodes D_{10} and D_{11} are turned off with ZCS.

Stage 2 ($t_2 < t < t_3$: Figure 4b): At $t = t_2$, $v_{Cr} = 2V_i$, $i_{Lr} = 0$, $i_{T1p} = 0$, $i_{T2p} = 0$, $i_{LF} = 0$, $i_{T1S2} = 0$, and $i_{T2S} = 0$ are valid. This interval is used for output voltage regulation control. This stage ends by applying a control signal to the gate of S_2.

Stage 3 ($t_3 < t < t_4$: Figure 4c): At $t = t_3$, $v_{Cr} = 2V_i$, $i_{Lr} = 0$, $i_{T1p} = 0$, $i_{T2p} = 0$, $i_{LF} = 0$, $i_{T1S2} = 0$, and $i_{T2S} = 0$ are valid. This interval starts at $t = t_3$ when S_2 is turned on and resonance between

C_r, L_m, and L_{Fp} begins. For this resonance,

$$i_{LFp} = \left(\frac{2V_i}{\omega_2 L_{Fp}} - \frac{V_{CBp}}{\omega_2 L_{e1}}\frac{L_m}{L_{Fp}}\right)\sin(\omega_2 (t-t_3)) - \frac{V_{CBp}}{L_{e1}}(t-t_3) \tag{9}$$

$$i_{Lm}(t) = \left(\frac{2V_i}{\omega_2 L_m} - \frac{V_{CBp}}{\omega_2 L_{e1}}\right)\sin(\omega_2 (t-t_3)) + \frac{V_{CBp}}{L_{e1}}(t-t_3) \tag{10}$$

$$v_{cr}(t) = \left(2V_i - V_{CBp}\frac{L_m}{L_{e1}}\right)\cos(\omega_2 (t-t_3)) + V_{CBp}\frac{L_m}{L_{e1}} \tag{11}$$

are obtained. In these equations,

$$L_{e1} = L_m + L_{Fp} \tag{12}$$

$$L_{e2} = \frac{L_m L_{Fp}}{L_m + L_{Fp}} \tag{13}$$

$$\omega_2 = \frac{1}{\sqrt{L_{e2}C_r}} \tag{14}$$

$$Z_2 = \sqrt{\frac{L_{e2}}{C_r}} \tag{15}$$

are valid. Here, L_{Fp} and V_{CBp} are reflected values to the primary of the secondary waves L_F and V_{CB} respectively. L_m is magnetizing inductance of T_1.

In the meantime, T_2 operates as a flyback transformer and its current rises linearly. This state can be expressed as follows:

$$i_{T2p} = \frac{V_{CB}}{L_{2p}}(t-t_3). \tag{16}$$

At this stage T_1 operates as a forward transformer based on resonance and C_r is discharged and C_B is supplied. At the same time, T_2 operates as a flyback transformer and so some energy is stored in its magnetizing inductor. At the moment $t = t_4$, L_F current falls to zero; meanwhile D_7 turns off with ZCS and this interval ends.

Stage 4 ($t_4 < t < t_5$: Figure 4d): This interval starts when D_7 turns off with ZCS. At $t = t_4$, $v_{Cr} = V_{Cr4}$, $i_{Lr} = 0$, $i_{T1p} = i_{T1p4}$, $i_{T2p} = i_{T2p4}$, $i_{LF} = 0$, $i_{T1S2} = 0$, and $i_{T2S} = 0$ are valid. Resonance between C_r and L_m begins. T_1 operates as a flyback transformer at this stage. For this resonance, the following equations are obtained:

$$i_{Lm} = \frac{V_{cr4}}{Z_3}\sin(\omega_3 (t-t_4)) + I_{Lm4}\cos(\omega_3 (t-t_4)) \tag{17}$$

$$v_{cr} = V_{Cr4}\cos(\omega_3 (t-t_4)) - I_{Lm4}Z_3\sin(\omega_3 (t-t_4)) \tag{18}$$

In these equations,

$$\omega_3 = \frac{1}{\sqrt{L_{1p}C_r}} \tag{19}$$

$$Z_3 = \sqrt{\frac{L_{1p}}{C_r}} \tag{20}$$

are valid. Here, L_{1p} is the primary inductance of T_1 and Z_3 is the impedance of the resonance circuit. At $t = t_5$, C_r voltage falls to zero and D_5 is turned off and D_6 is turned on with ZVS, and so this interval ends.

Stage 5 ($t_5 < t < t_6$: Figure 4e): D_6 is turned on with ZVS and at $t = t_5$, $v_{Cr} = 0$, $i_{Lr} = 0$, $i_{T1p} = I_{T1pmax}$, $i_{T2p} = I_{T2p5}$, $i_{LF} = 0$, $i_{T1S2} = 0$ and $i_{T2S} = 0$ are valid. At this stage, T_2 continues operating as a flyback transformer. Primary inductance of T_1 operates as a current source. At $t = t_6$, the gate signal of S_2 is stopped. Therefore, the switch S_2 is turned off with hard switching.

Stage 6 ($t_6 < t < t_7$: Figure 4f): This interval starts at $t = t_6$ when S_2 is turned off. At the beginning of this stage $v_{Cr} = 0$, $i_{Lr} = 0$, $i_{T1p} = 0$, $i_{T2p} = 0$, $i_{LF} = 0$, $i_{T1S2} = I_{T1S2max}$, and $i_{T2S} = I_{T2Smax}$ are valid. At this stage, a part of the energies in magnetizing inductances of T_1 and T_2 are transferred to the output.

For this stage, the following equations can be written:

$$i_{T1S2} = I_{T1S2\max} - \frac{V_o}{L_{1S2}}(t - t_6) \tag{21}$$

$$i_{T2S} = I_{T2S\max} - \frac{V_o}{L_{2S}}(t - t_6) \tag{22}$$

Finally, at $t = t_7 = t_0$, the switch S_1 is turned on again and so one switching period is completed and a new switching period starts.

MODE 2

When the line voltage is lower than the value $(a_{11}/2)V_{CB}$, Mode 2 occurs, and at this mode five stages occur. Both T_1 and T_2 operate as a flyback transformer in principle over one switching period. Only stage 3 is different from stage 3 at Mode 1, and the other stages are similar at both modes.

Before the different stage 3 at Mode 2, at $t = t_3$, $v_{Cr} = 2V_i$, $i_{Lr} = 0$, $i_{T1p} = 0$, $i_{T2p} = 0$, $i_{LF} = 0$, $i_{T1S2} = 0$, and $i_{T2S} = 0$ are valid. At $t = t_3$, a control signal is applied to the gate of S_2 and this stage begins. In this stage, resonance between C_r and L_{1p}, the primary inductance of T_1, occurs. For this resonance, the following equations are obtained:

$$i_{Lm} = \frac{2V_i}{Z_3}\sin(\omega_3(t - t_3)) \tag{23}$$

$$v_{Cr} = 2V_i\cos(\omega_3(t - t_3)) \tag{24}$$

$$I_{Lm\max} = 2V_i\sqrt{\frac{C_r}{L_{1p}}} \tag{25}$$

$$t_{43} = \frac{\pi}{2}\sqrt{L_{1p}C_r} \tag{26}$$

This interval ends when C_r voltage falls to zero and D_6 turns on with ZVS.

In the meantime, T2 operates as a flyback transformer and its current rises linearly. This state can be expressed as below:

$$i_{T2p} = \frac{V_{CB}}{L_{2p}}(t - t_3) \tag{27}$$

3. Design procedure

The proposed new converter, based on resonance and soft switching, provides a good PFC and tight output voltage regulation with exceptional PFC and an ideal DPT. For this converter, the following design procedure can be implemented by considering the theoretical analysis given above.

1) At first, the signal and the blocking times of the switching period are determined depending on the maximum switching frequency. There are two signal and two blocking times in one switching period as shown in Figure 5. If the blocking time is chosen to be 10% of the switching period for maximum frequency, the following equations can be written:

$$T_{P\min} = \frac{1}{f_{p\max}} \tag{28}$$

$$T_{GS1} = T_{GS2} = T_{GS} = 0.9\frac{T_{P\min}}{2} \tag{29}$$

$$T_{BL1} = T_{BL2} = T_{BL} = 0.1\frac{T_{P\min}}{2} \tag{30}$$

2) The maximum input power can be written as below by using the energy of the resonance capacitor and the maximum switching frequency:

$$P_{in\max} = \frac{1}{2}C_r\left(V_{AC-RMS}\right)^2 f_{p\max} \tag{31}$$

The resonance capacitor value can be calculated from this equation.

3) The positive half period of the PFC resonance, which occurs when the switch S_1 is on, should be completed at a time period of signal time at most. For this stage,

$$t_{02} = \pi\sqrt{L_rC_r} \le T_{GS} \tag{32}$$

can be written. The resonance inductor can be calculated from this equation.

4) Based on the ideal DPT idea as shown in Figure 1, when the instantaneous value of the line voltage is higher than its rms value, T_1 must operate as both forward and flyback transformer; otherwise it must operate only as a flyback transformer as shown in Figure 3. When T_1 operates only as a flyback transformer, the resonance capacitor C_r should be discharged through the primary inductance of T_1 and the switch S_2 at a time period of at most a signal time. In this case, the following equation can be written from (26):

$$t_{43} = \frac{\pi}{2}\sqrt{L_{1p}C_r} \le T_{GS} \tag{33}$$

The primary inductance of T_1 can be obtained from this equation.

5) The following equation can be written by considering that the voltage value of C_r is twice the instantaneous line voltage for operating of T_1 at the boundary of forward and flyback.

$$\frac{2V_{AC-RMS}}{a_{11}} = V_{CB} \tag{34}$$

The turns ratio a_{11} and then L_{1S} of T_1 can be calculated by using this equation. For example, for $V_{CB} = V_{AC-RMS}$, $a_{11} = 2$ and $L_{1S} = L_{1p}/4$ are obtained.

6) Considering T_1 operating at boundary, the maximum current of L_{1p} in (25) can be written as below:

$$I_{T1p\max\_b} = 2V_{AC-RMS}\sqrt{\frac{C_r}{L_{1p}}} \tag{35}$$

W operating as a flyback converter, this current should be reduced to zero through secondary winding within a signal time. This situation can be explained with the following equation:

$$a_{12}I_{T1p\max\_b} - a_{12}^2\frac{V_o}{L_{1p}}T_{GS} = 0 \tag{36}$$

The turns ratio a_{12} and then L_{1S2} of T_1 can be calculated by using this equation.

7) It is known that 68% of total input power should be transferred to the output directly for an ideal DPT and in the converter energy stored in the primary inductance should be transferred to the output as a control signal is applied to the gate of S_2. Thus, the maximum primary current of T_2 and the power transferred to the output through T_2 can be explained with the following equations, respectively:

$$I_{T2p\max} = \frac{V_{CB}}{L_{2p}}T_{GS} \tag{37}$$

$$P_{IDPT} = \frac{0.81}{8}\frac{V_{CB}^2}{f_{p\max}L_{2p}} = 0.32P_{in\max} \tag{38}$$

The primary inductance of T_2 can be calculated by using these equations. Moreover, the current in (37) should be reduced to zero through secondary winding within a signal time similarly in (36). For this state, the following equation can be written:

$$a_2I_{T2p\max} - a_2^2\frac{V_o}{L_{2p}}T_{GS} = 0 \tag{39}$$

The turns ratio a_2 and then L_{2S} of T_2 can be calculated by using this equation.

8) When the instantaneous value of the main voltage is higher than its rms value, the transformer T_1 operates as a forward transformer at first and transfers the excess energy of C_r from the value at the boundary operating to C_B through L_F. Then T_1 operates as a flyback transformer and it transfers the remaining energy of C_r to the output through L_m. For an ideal DPT, the values of the energy transferred to the output must be constant.

The state explained above can be provided by determining a suitable L_F value. For this purpose, the value of L_F is calculated to provide maximum L_m current to be equal to the value given in (35) for different line voltage values between V_{AC-RMS} and V_{AC-MAX}. Then the average of L_F values is used and so a good DPT is achieved. For example, the calculated values of L_F for the prototype in this study are given in Figure 6. The average L_F value is 46 μH.

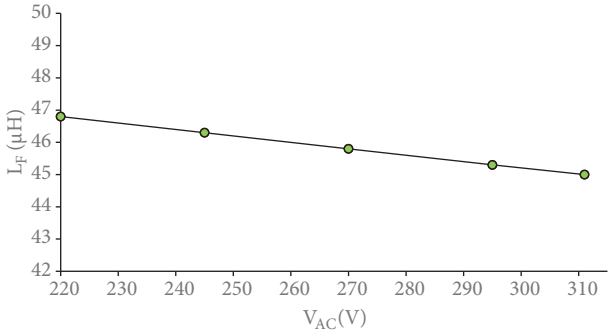

Figure 6. Required L_F values for different line voltage values.

4. Experimental results

The proposed new single stage single phase PFC converter with resonance and soft switching given in Figure 2 was implemented for 125 W and 100 kHz. The key parameters of the components used in the experimental circuit are given in the Table. Component parameters were determined with respect to the design procedure.

Table. Some values of the components used in experimental circuit.

Component	Parameter	Value
PFC Resonant Circuit	L_r	81 μH
	C_r	20 nF
T_1 Transformer	L_{1p}	325 μH
	L_{1S1}	81 μH
	L_{1S2}	88 μH
T_2 Transformer	L_{2p}	1020 μH
	L_{2S}	210 μH
Capacitors	C_B	220 μF
	C_o	2200 μF
Inductors	L_F	46 μH
Semiconductors	S_1	IXFH15N100Q (1000 V-15 A-0.7 Ω)
	S_2	IXTQ460P2 (500 V-24 A-270 mΩ)
	D_1-D_{11}	DSEI12-12 (1200 V-11 A)

The oscillogram of the main voltage and the current waveforms is given in Figure 7. As shown in this figure, the power factor is 0.998 and it can be seen that PFC is achieved perfectly by using a purely resonant circuit in the proposed converter. On the other hand, the quality of PFC is not affected by the variations in the input line voltage and the output load and it is 0.996 at the worse condition that is rated load and minimum line. Moreover, a very light L-C filter is used for the line input.

In Figure 8, Figure 9, Figure 10, and Figure 11 are taken for Mode 1. The voltage and the current waveforms of the switch S_1 are given. In this figure, it is clearly seen that the switch S_1 operates fully SS and it is not subjected to an additional voltage stress. Moreover, the current flowing through S_1, which is drawn from the main at the same time, is purely sinusoidal.

The current and voltage waveforms of the switch S_2 are given in Figure 9. Here, S_2 current is the sum of the currents of the magnetizing inductances of the transformers T_1 and T_2. The switch S_2 is turned on with ZCS due to operating with DCM and so starting from zero of the magnetizing currents of T_1 and T_2, although it is turned off with hard switching.

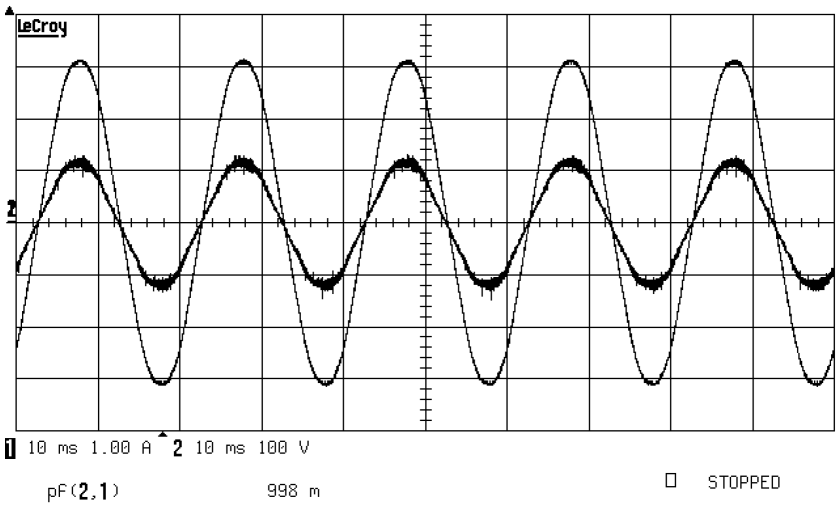

Figure 7. Main voltage and current waveforms.

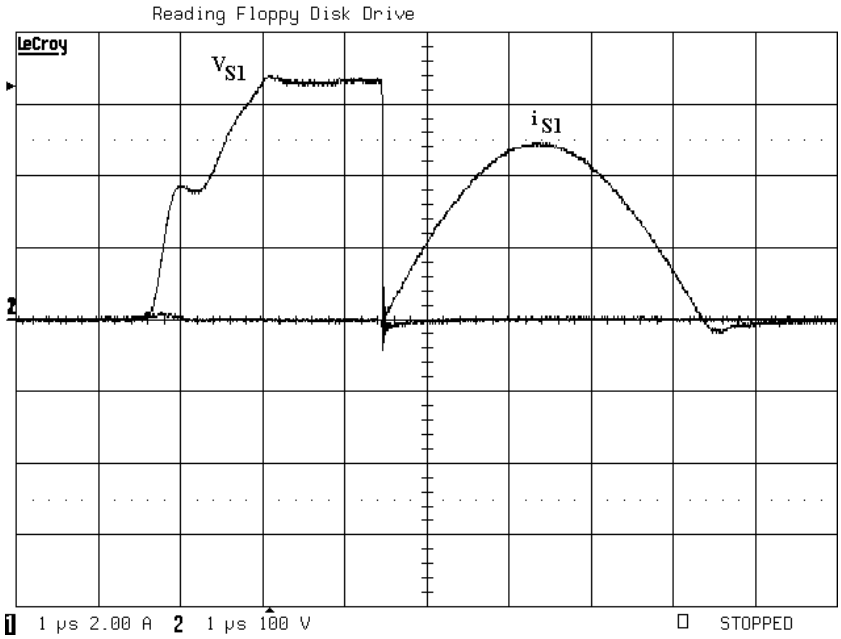

Figure 8. Voltage and current waveforms of S_1.

In Figure 10, current waveforms of the primary inductance of T_1 and forward inductance are given for Mode 1. Here, because of the resonances mentioned in stage 3 and stage 4 for Mode 1, the variations in the currents are near sinusoidal.

The currents that are transferred to the output through secondary windings of the transformers T_1 and T_2 are given in Figure 11. Those currents fall to zero linearly in signal time. Thus, SS is provided for the diodes D_{10} and D_{11}. At the same time, the areas of i_{L1S2} and i_{L2S} currents show the transferred energies to the output for DPT and for regulation, respectively.

The oscillogram of the efficiency curve versus output power is shown in Figure 12. From this state, it can be seen that maximum efficiency is about 75% and is provided at full load.

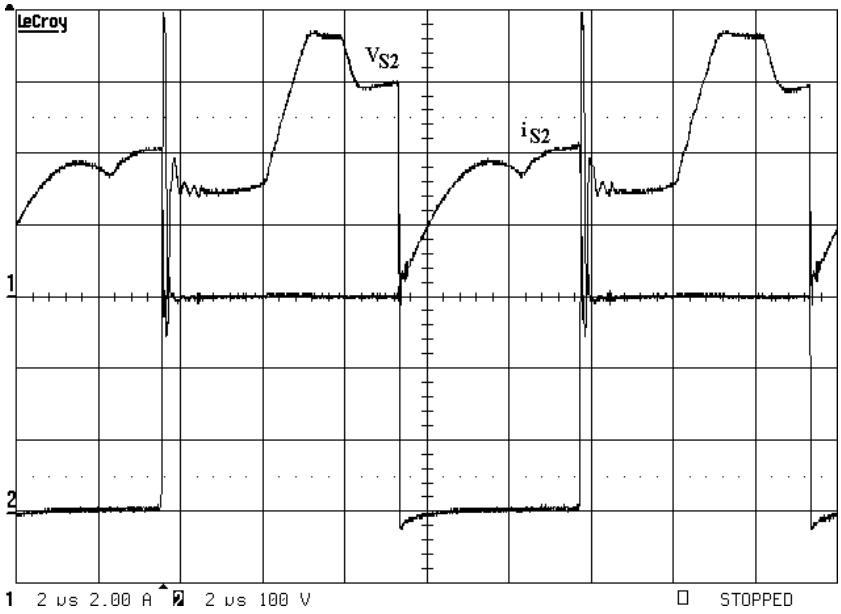

Figure 9. Voltage and current waveforms of S_2.

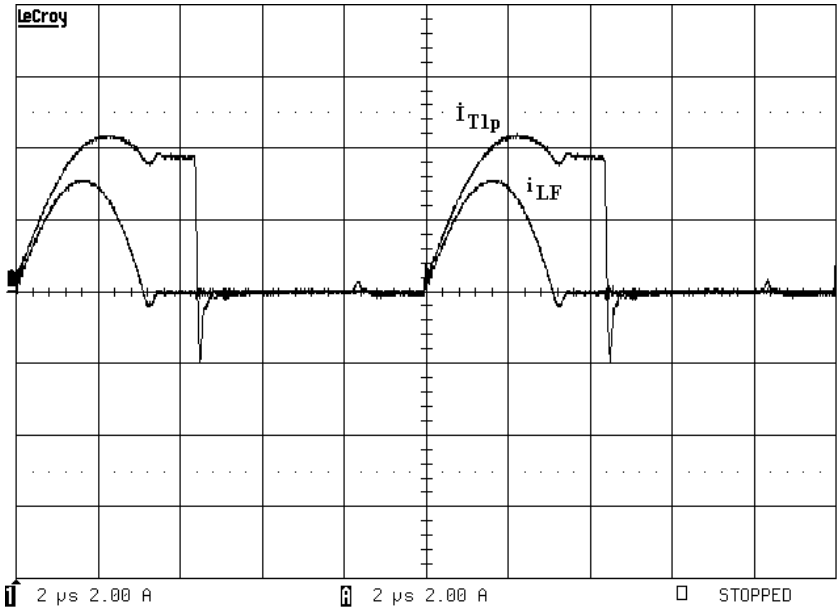

Figure 10. The current waveforms of primary inductance of T_1 and L_F.

5. Conclusion

This paper presents a new single stage single phase PFC converter with resonance and SS. In this converter, PFC is achieved by using a fully resonant circuit and one switch. The resonance current that is drawn from the grid is purely sinusoidal and its peak value is proportional to the instantaneous value of the main voltage. Therefore, a very light L-C filter is used for the line input. Moreover, PFC is not affected by the variations in the line voltage or the load. In addition, PFC switch S_1 is turned on and off with ZCS because of the resonance.

With the proposed topology, the isolation and the regulation of output voltage are achieved by using a second switch and flyback and forward topologies based on resonance and DPT. On the basis of the DPT idea,

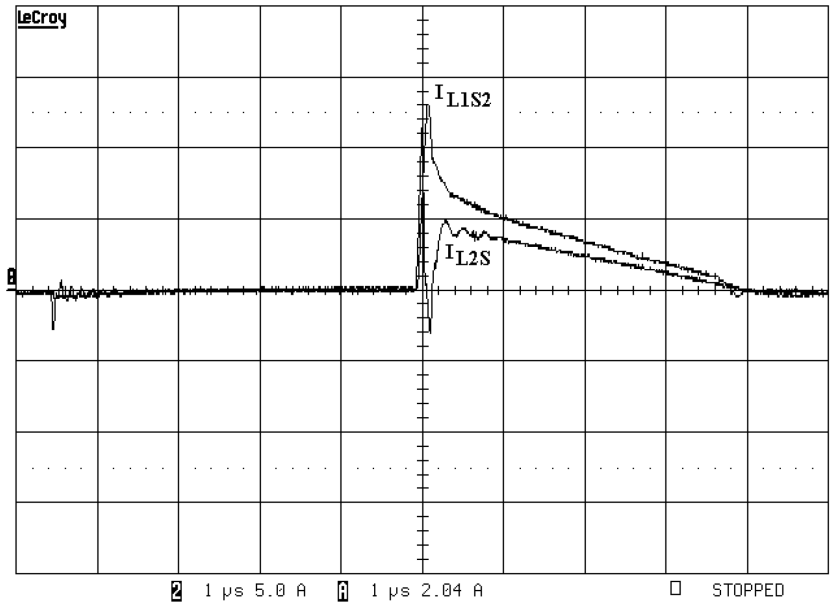

Figure 11. The current waveforms of secondary windings of T_1 and T_2.

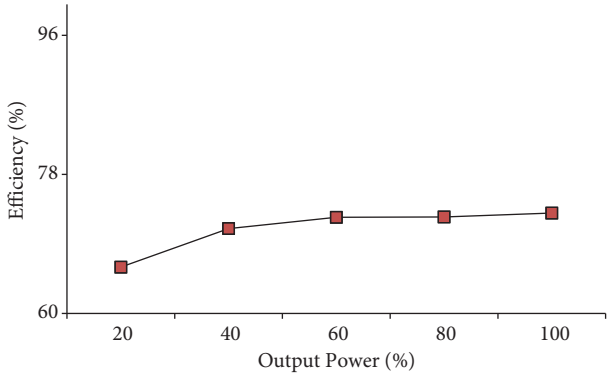

Figure 12. The efficiency curve versus output power.

the majority of the input energy is transferred to the output directly and the remaining energy is transferred to C_B by a resonance circuit. Then the energy is transferred to the output by flyback converter operating in DCM for output voltage regulation. The second or output switch S_2 is turned on with ZCS due to operating in DCM yet it is turned off with hard switching. Therefore, both switches are controlled with the same closed loop and the time multiplexing, and are switched with soft switching.

The proposed new single stage single phase PFC isolated converter with resonance and soft switching was analyzed in detail. The operation principle and the theoretical analysis of the new converter were exactly verified by a prototype at 125 W and 100 kHz. It has been observed that a good PFC and a tight output voltage regulation with DPT and SS have been achieved perfectly in the proposed converter.

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