

High dynamic performance of a BLDC motor with a front end converter using an FPGA based controller for electric vehicle application

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Abstract: This paper focus on a novel operation of a brushless dc (BLDC) motor fed by a proportional integral (PI) controlled buck–boost converter supplemented with a battery to provide the required power to drive the BLDC motor. The operational characteristics of the proposed BLDC motor drive system for constant as well as step changes in dc link voltage of a front end converter controlled by a Xilinx System Generator (XSG) based PI controller for two quadrant operations are derived. Thus a field programmable gate array (FPGA) based PI controller manages the energy flow through the battery and the front end converter. Moreover, speed to voltage conversion logic, made to control the BLDC motor through the PI controller, improves the performance and gives optimum control under the unstable driving situation or varying load condition when the complete system becomes a subject of application to electric vehicles (EVs) and hybrid electric vehicles (HEVs). The dual closed loop control implemented for end to end speed control of the proposed drive system facilitates the system with high accuracy integrated with excellent dynamic and steady state performance. In this paper, the proposed controller was designed for a 5 kW/480 V BLDC motor drive system. The feasibility of the proposed dual loop control topology for the BLDC motor drive system is validated and verified with extensive dynamic simulation in MATLAB/SIMULINK and XSG environment.

Key words: BLDC motor drive, EVs, FPGA, front end converter, HEVs, PI controller, Xilinx system generator (XSG)

1. Introduction

Over the last two decades, issues like sustainable development and environmental pollution due to vehicular emissions are accelerating modern science and technology and have given thrust to the research on electric vehicles (EVs) and hybrid electric vehicles (HEVs). Brushless dc (BLDC) motor drives have been found more suitable for EVs, HEVs, and other low power applications [1–3]. The BLDC motor has many advantages over the conventional induction and dc motors, such as better speed and torque characteristics, high efficiency and reliability, low electromagnetic interference (EMI), high power to weight and torque to current ratio, and long operation life [4,5]. Compared to induction machines the BLDC motor has lower inertia, allowing for faster dynamic response to reference commands. Moreover, advancements in power electronic devices and DSP/FPGA based processors have added more features to these motor drives to make them more prevalent in industrial installations [6–8]. Hysteresis current control and pulse width modulation (PWM) control coupled with continuous control theory produced the most widely used BLDC motor control techniques. The control

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of a BLDC motor in medium as well as high speed applications is much easier compared to induction motors. Hysteresis current control is essential in achieving adequate control of instantaneous torque and hence yielding faster speed response. Digital PWM control techniques implemented for speed control of BLDC motors have maximum speed error below 5% [9,10]. Therefore, they are not suitable for applications that require high precision. Conduction angle control and current mode control of BLDC motors also have significant errors in speed control, though less than those of digital PWM control [11]. Conventional BLDC motors with a six switch inverter, excited through bipolar based soft switching currents, are suitable for low/medium power and medium speed applications as well. In order to use these motors effectively at their optimal efficiency and in the safe operating zone they must be driven at their nominal power requirement [12]. Power electronic converters provide the featured solution to meet the demand for regulated electrical power for efficient and dynamic operation of BLDC motor drives. Most of the controllers designed for speed control of BLDC motors consider the unidirectional power flow converter as it facilitates the easy control and reduced cost of the drives [13]. Moreover, the use of the battery to feed to the front end converter of the BLDC motor drive not only removes the lack of specific power, but also enables excellent performance of the drive system in both acceleration and regenerative braking in EV applications [14]. The converter also adjusts the dc input voltage to the front end converter of the BLDC motor versus the motor speed in order to reduce the ripple of the motor current waveform [15]. This fact is of particular importance in the case of slotless axial-flux PMDC motor drives, which have been proposed recently for medium-speed and high torque motor drive applications such as the direct driving of EV wheels [16]. Conventional proportional integral (PI) control technology does not meet the requirement of a very fast dynamic response of EVs under rapid changes in operating modes of the drive system. The evolution of a high speed and high density FPGA based processor is now providing the best alternative to the ASIC and microprocessor based implementation of complex control algorithms. The improved and appreciable dynamic and steady state performance of BLDC motors supplemented with FPGA based controllers will make them suitable for position control in machine tools, robotics and high precision servos, aerospace, healthcare/biomedical equipment, speed control, and torque control in various industrial drives and process control applications.

In this paper, a novel FPGA based dual speed control technique is proposed targeting very precise speed control applications. The complete paper is structured as follows. The overall work is briefly introduced in section 2. Section 3 deals with the mathematical modeling of a buck–boost converter, the induction profile of the BLDC motor, and the front end converter. The proposed dual loop speed control, designed to meet the transient and steady state constraint with an objective of excellent speed control of BLDC motor drive systems, is discussed in detail in section 4. Section 5 deals with simulation analysis of the proposed control strategy in MATLAB/SIMULINK and Xilinx system generator environment and performance evaluation of the entire drive system under steady state and dynamic conditions. Finally, conclusions are given with a discussion of the results and merits of the proposed control scheme in section 6.

2. Structure of the proposed controlled dc-dc converter fed BLDC motor drive

Figure 1 shows front end converter fed BLDC motor drives with a dual control loop designed on an FPGA processor to control the variable dc link voltage and hence to achieve the desired speed control. The battery used to feed the buck–boost converter circuit acts as source and sink during acceleration and regeneration mode of EVs, respectively. The validation of the proposed model for EV application governs the choice of buck–boost converter for this application. Additionally, the selection of buck–boost converter reduces the switching losses

of VSI operated at low frequency for electronic commutation of the BLDC motor drive [17]. The discrete rotor position, sensed through a Hall sensor, is fed back to the FPGA processor

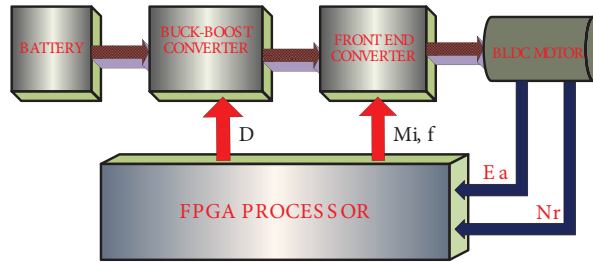


Figure 1. Block diagram of the proposed drive system.

- (i) wherein speed to voltage conversion is carried out. Voltage error equivalence, $V_e(k)$, of speed error, $N_e(k)$, is given to the PI controller, which generates the control signal, D , for the operation of the buck–boost converter.
- (ii) to generate switching signal M_i at a frequency, f , for the operation of the front end converter.

3. Mathematical modeling

3.1. Buck–boost converter

Eq. (1) governs the relation between input (V_{in}) and output voltage (V_{dc}) during continuous conduction mode of the buck–boost converter [18].

$$V_{dc} = \frac{V_{in} * D}{1 - D} \tag{1}$$

The value of the inductance L_0 is given by (2)

$$L_0 = \frac{(1 - D) * V_{in}}{\Delta i_{L_0} f_s} \tag{2}$$

The value of the capacitance C_0 is given by (3)

$$C_0 = \frac{D}{(R f_s) \left(\frac{\Delta V_{c0}}{V_0} \right)} \tag{3}$$

3.2. The induction profile of the BLDC motor drive system

The motor under investigation is a permanent magnet synchronous machine (PMSM) with the permanent magnet mounted on the rotor and concentrated stator windings resulting in trapezoidal induced back EMFs with maximum possible width of the flat top portion [19]. To ensure smooth torque production a constant current is forced through each phase winding during the interval when the back EMF is at its maxima as shown in Figure 2. For unipolar excitation with soft switching current, positive current flows through the phase windings for positive back EMFs with each conduction period lasting for 120° . However, no current flows through phase windings when back EMFs vary with time. This results in two phases conducting at a time and producing the torque. Therefore, for trapezoidal variation of induced back EMFs and with an assumption that phase inductances are constant, the equations governing the above described induction profile of the BLDC motor in abc reference frame [20] are given by

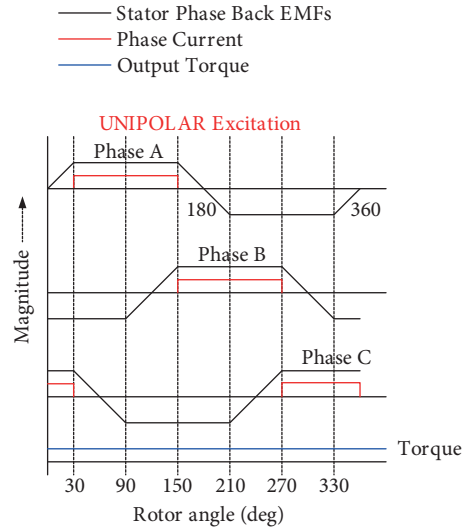


Figure 2. Induction profile of the BLDC drive system showing back EMFs, phase current, and output torque waveform with unipolar excitation.

$$\frac{di_a}{dt} = \frac{1}{3L_s} [2V_{ab} + V_{bc} - 3R_s i_a + \psi p \omega_r (-2E_a + E_b + E_c)] \quad (4)$$

$$\frac{di_b}{dt} = \frac{1}{L_q} [-V_{ab} + V_{bc} - 3R_s i_b + \psi p \omega_r (E_a - 2E_b + E_c)] \quad (5)$$

$$\frac{di_c}{dt} = - \left[\frac{di_a}{dt} + \frac{di_b}{dt} \right] \quad (6)$$

$$T_e = \left[\frac{E_a i_a + E_b i_b + E_c i_c}{\omega} \right] \quad (7)$$

3.3. Front end converter

Figure 3 shows a three phase front end converter for speed control of the BLDC motor drive system through electronic commutation. Each leg has two IGBT switches, accompanied by antiparallel flywheel diodes, which are complementary in their switching action. For understanding the underlying principles involved in working of this front end converter circuit, phase A is taken under consideration.

From Figure 3, the voltage V_{aN} across phase A with respect to the neutral point (N) of the dc link capacitor [21] is expressed by Eq. (8):

$$V_{aN} = \frac{4}{\pi} \left[\frac{V_{dc}}{2} \right] \left[\cos \omega_o t - \frac{1}{3} \cos 3\omega_o t + \frac{1}{5} \cos 5\omega_o t - \frac{1}{7} \cos 7\omega_o t + \frac{1}{9} \cos 9\omega_o t - \dots \right] \quad (8)$$

The voltage, V_{nN} , between the neutral of stator winding and neutral point (N) of the dc link capacitor is given by (9):

$$V_{nN} = \frac{4}{\pi} \left[\frac{V_{dc}}{2} \right] \left[-\frac{1}{3} \cos 3\omega_o t - \frac{1}{9} \cos 9\omega_o t - \dots \right]. \quad (9)$$

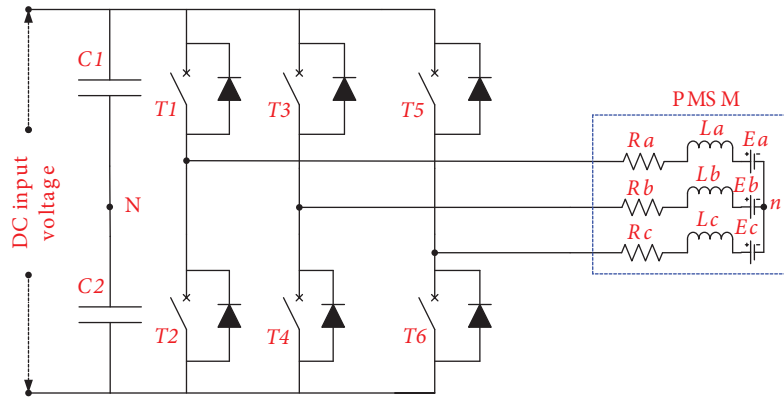


Figure 3. Circuit topology of a voltage control three phase inverter.

Therefore, the voltage V_{an} that appears across phase A with respect to winding’s neutral n is given by (10):

$$V_{an} = V_{aN} - V_{nN} \tag{10}$$

$$V_{aN} = \frac{4}{\pi} \left[\frac{V_{dc}}{2} \right] \left[\cos \omega_o t + \frac{1}{5} \cos 5\omega_o t - \frac{1}{7} \cos 7\omega_o t + \dots \right]. \tag{11}$$

It can be inferred from Eq. (11) that the most dominant 3rd order harmonics are eliminated.

4. Proposed dual loop speed control

When precise speed control becomes the prime concern, multiple pathways become an essential ingredient to achieve the stated objective. Here in the proposed BLDC drive system the speed is being controlled

1. by controlling the input voltage to the front end converter with the help of the proposed PI controller and
2. by triggering the switching pulse of the front end converter proportional to EMF detection.

The design of efficient controllers is needed for the optimal operation of power converters to improve the close loop dynamic and steady state performance of the BLDC drive system. The conventional way of implementing a digital controller based on FPGA and developing a control algorithm using a high level language like Verilog hardware description language (VHDL) is cumbersome and tedious. The newly evolved FPGA based Xilinx system generator provides a very realistic solution for the aforesaid problem. Automatic code generation, dedicated hardware intellectual properties of the Xilinx block sets for FPGA core, and simulation of a real time physical system in a safer environmental zone make it an appropriate platform for our research. Thus, designing the controller based on FPGA (Xilinx system generator, a type of real time digital simulator) ensures very rapid prototyping of our proposed methodology [22].

The subject of application of the proposed BLDC drive system to EVs and HEVs, where predominantly step changes in speed occur, governs the selection of PI controller for excellent dynamic response of the system with zero steady state error. Here the discrete time FPGA based PI controller is controlling the dc link voltage to the front end converter and thus the speed of the BLDC drive system. Therefore, the dynamics of the entire drive system is completely governed by the controller.

4.1. Modelling of XSG based digital PI controller

In Figure 4, if $N_r(k)$, $N_r^*(k)$, and $N_e(k)$ denote the actual rotor speed, reference speed, and speed error, respectively, input to the speed to the voltage converter is given by (12)

$$N_e(k) = N_r^*(k) - N_r(k) \tag{12}$$

Voltage error, $V_e(k)$, equivalent to speed error is given by (13)

$$V_e(k) = \left[\frac{V_n}{N} \right] * N_e(k) \tag{13}$$

The output, switching command $U(k)$, of the PI controller at the k th instant is expressed as

$$U_k = [U_{k-1} + K_p \{V_e(k) - V_e(k-1)\} + K_i \{V_e(k) + V_e(k-1)\} * \Delta k], \tag{14}$$

where PI controller constant $K_p = 0.6$ and $K_i = 5$ and Δk is the sampling interval.

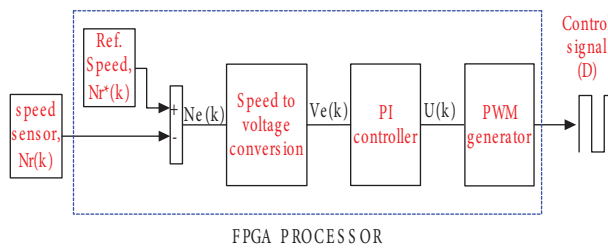


Figure 4. Block diagram of the proposed speed control algorithm.

Control signals, D , for the operation of the buck–boost converter, are generated by comparison of $U(k)$ with a 20-kHz triangular wave.

4.2. Delay control of switching sequences in the front end converter

The second way to control the speed of the motor is to vary the triggering rate of switches. The speed of the motor can be changed here by manipulating the time interval between switching of different phases. To control speed via this method, the circuitry required is shown in Figure 5.

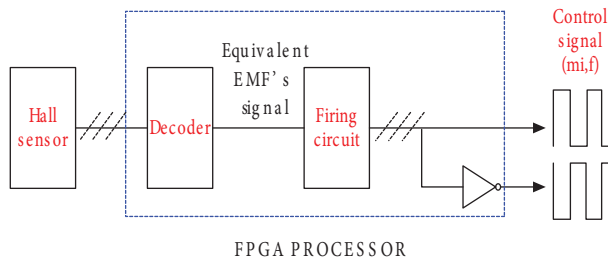


Figure 5. Switching signal generator for VSI.

To achieve a variable rate of switching between the different phases switching pulses are generated in synchronism with the discrete rotor position sensed by the Hall sensor. As shown in Figure 6, the Hall sensor will detect the discrete rotor position after every 60 degree rotation and will produce pulses that are converted into equivalent back EMF signals by the decoder. A firing circuit with back EMF signal produces the switching pulses, shown in Table 1, for the front end converter.

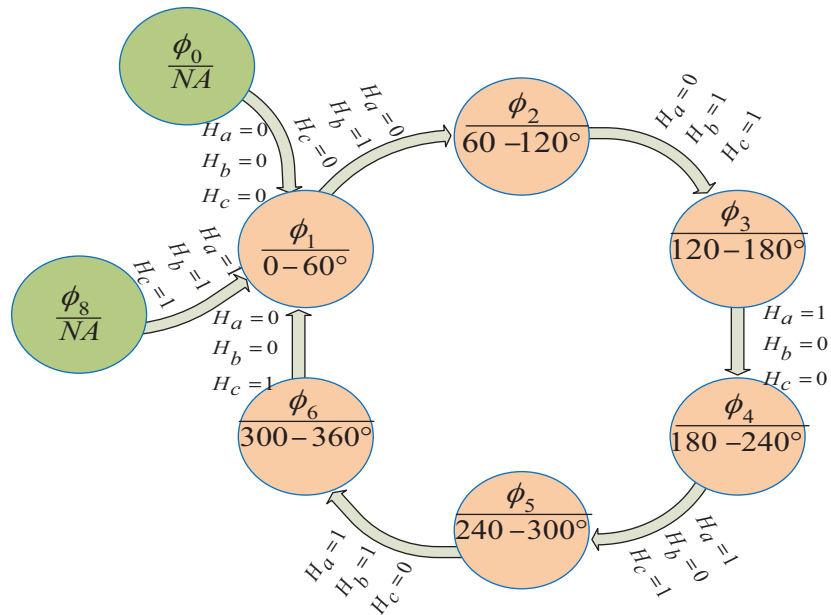


Figure 6. State representation of Hall sensor functionality.

Table 1. Switching states of the VSI feeding a BLDC motor drive based on the Hall-effect position signals.

ϕ°	State of switches					
	T ₁	T ₂	T ₃	T ₄	T ₅	T ₆
NA	0	0	0	0	0	0
0-60	0	0	0	1	1	0
60-120	0	1	1	0	0	0
120-180	0	1	0	0	1	0
180-240	1	0	0	0	0	1
240-300	1	0	0	1	0	0
300-360	0	0	1	0	0	1
NA	0	0	0	0	0	0

Therefore, the change in speed is accompanied by electronic commutation where the inductance energy of any one phase reaches the maximum value during each 30 electrical degrees, inductance holds this energy for next 120 electrical degrees, and which finally is released in the next 30 electrical degrees through an antiparallel fly wheel diode. This commutation process for phase A is shown in Figure 7.

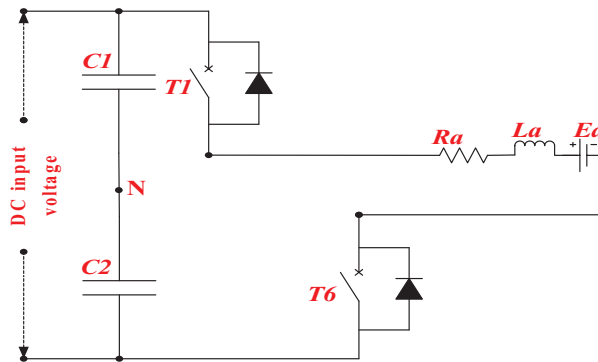


Figure 7. Equivalent circuit of phase A of the BLDC drive system.

5. Description of simulation setup and performance evaluation of the proposed control scheme

To validate the proposed methodology, extensive dynamic simulations are carried out in

1. MATLAB/SIMULINK environment using the power system toolbox for power circuitry in floating point representation.
2. XSG environment using Xilinx block set tools for a control circuit in fixed point representation.

The overall block diagram with closed loop control using the proposed FPGA based PI controller is shown in Figure 8, which outlines the communication between the FPGA based PI controller and the rest of the electric drive system. The control circuit consists of three parts:

1. Speed to voltage conversion
2. PI controller and saturation
3. Delay control of switching in front end converter.

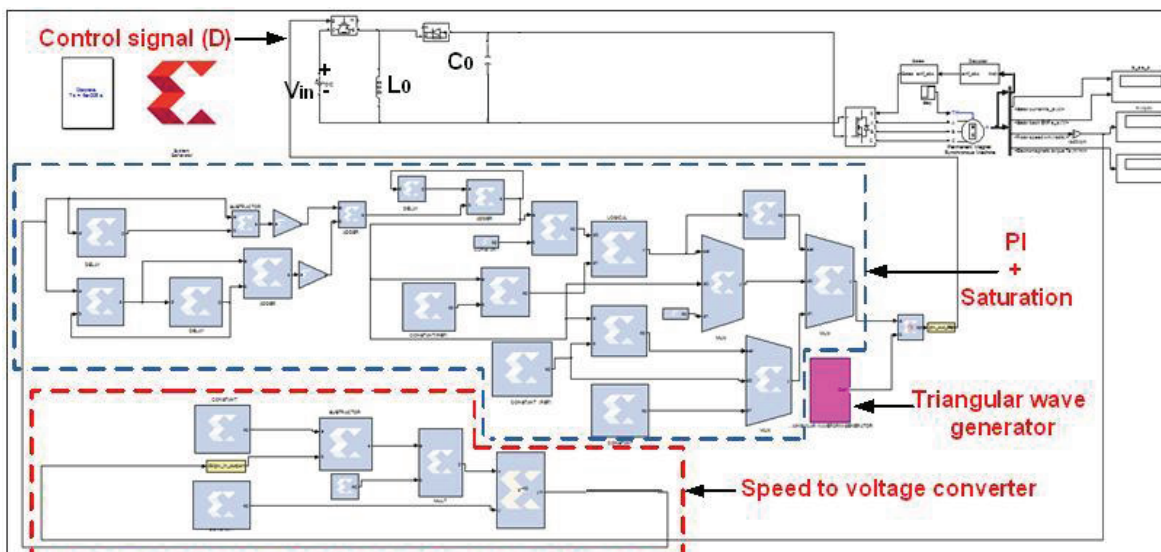


Figure 8. Simulation circuit diagram in MATLAB/SIMULINK and Xilinx system generator environment.

The power circuit consists of

1. Buck–boost converter
2. VSI fed BLDC drive system.

Reference speed is digitally set and actual rotor speed is sensed and a speed to voltage conversion logic loop, shown in Figure 8, is used to convert speed error into voltage equivalence error, which is further utilized by the proposed PI controller to generate a gate signal for discrete IGBT switch used in the buck–boost converter. The IGBT switch is rated for 60 A, 700 V, and 20 kHz frequency. In this way voltage is drawn from the power converter for the desired speed response of the BLDC drive system. Simulation results and performance of proposed system are discussed below.

The detailed data of power circuit considered for simulation are given in Table 2. The performance of the BLDC motor drive system is categorized into steady state and dynamic performance. The performance indices:

Table 2. Parameters of power circuit considered for simulation.

S. no.	Parameter	Numerical value
BLDC motor drive		
1	No. of pole pairs	2
2	Rated power (P_{rated})	5 KW
3	Rated torque (T_{rated})	10 N.m
4	Rated dc link voltage (V_{rated})	480 V
5	Torque constant (K_t)	1.4 N.m/A
6	Voltage constant	160 V/k rpm
7	Stator phase resistance (R_s)	2.85 ohm
8	Stator phase inductance (L_s)	8.5 mH
Buck-boost converter		
9	Buck boost inductor (L_0)	20 mH
10	Buck boost capacitor (C_0)	800 μ F
11	Input voltage (V_{in})	12 V
12	Switching frequency(f_s)	20 kHz

Primary-(a) Percentage average speed error, (b) Maximum speed ripples, (c) Percentage maximum speed error and

Secondary-(a) stator back EMFs E (V), (b) stator current I (A), (c) electromagnetic torque T_e (N-m), (d) dc link voltage V_{dc} (V) from the buck-boost converter are selected to study the effectiveness of the proposed control scheme.

5.1. Steady state analysis

This analysis is aimed to determine if the actual motor speed reaches the commanded speed at steady state. Based on the speed error and its voltage equivalence being correct the proposed controller executes the steps required to decide the duty cycle required for the IGBT switch of the buck-boost converter in the next cycle.

5.1.1. Speed ripple and percentage speed error calculation

The average speed error and maximum speed error are the function of speed ripples. It is therefore essential to find out the speed ripples at steady state for both the dynamic and steady state performance evaluation.

$$\% \text{Average speed error} = \frac{\text{Average speed ripple}}{\text{Average speed}} \times 100$$

$$\% \text{Maximum speed error} = \frac{\text{Maximum speed ripple}}{\text{Reference speed}} \times 100$$

The results, shown in Figures 9 (a)–(c), illustrate that the ability of the proposed controller in tracking the commanded speed is reasonably good under different sets of operating conditions. The results, in reference to Figures 9(a)–(c) and Table 3, are summarized below:

1. It is very clear that average speed lies very close to commanded speed and maximum speed ripple is well below 6 rpm.
2. The percentage average speed error and percentage maximum speed error are always less than 1%.
3. It is also notable that average error and maximum error are decreasing reasonably fast with increase in commanded speed.

4. For lower speed range (900–1100 rpm), ripples are almost constant, during steady state, in their magnitude. Due to this reason average error and maximum error are almost equal to each other, which can be seen from Table 3.

Table 3. Summary of simulated results.

Proposed control technique	Performance indices	N_r^* (rpm)	N_{avg} (rpm)	%Average error	Maximum speed ripple	%Maximum error
	Steady state performance	900	898.35	0.623	5.62	0.624
1000		999.80	0.40	4.0	0.40	
1100		1101.35	0.42	4.62	0.42	
Dynamic performance	1500	1500.1	0.23	3.9	0.26	
	3000	3001.7	0.11	4.5	0.15	

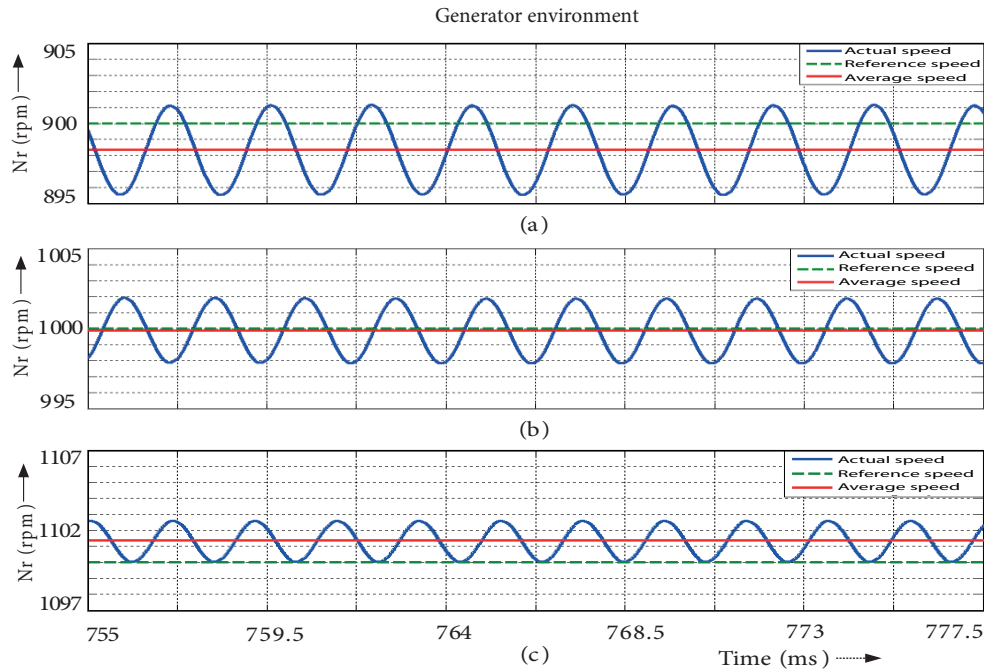


Figure 9. (a)–(c) Simulated speed response of the considered BLDC drive for reference speed of (a) 900 rpm, (b) 1000 rpm, (c) 1100 rpm, at 30% of rated load condition.

From Table 3 a chart is shown in Figure 10, in order to give a clear insight about the effectiveness of the proposed control scheme. The chart is drawn for

1. Percentage average error vs. average speed and
2. Percentage maximum speed error vs. reference speed

From the chart it can clearly be seen that average as well as maximum speed error keeps on decreasing with increase in reference speed.

Further, the steady state performance of the proposed control scheme for the BLDC drive against constant load of 3 N-m at two different commanded speeds is also shown in Figures 11 and 12.

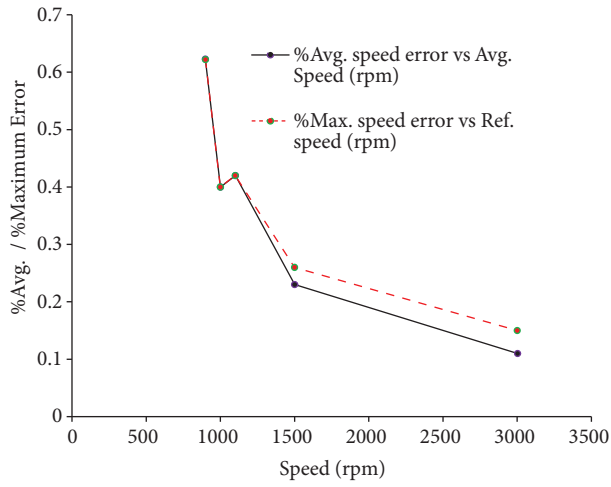


Figure 10. Performance evaluation of the proposed control scheme in terms of average and maximum error at different commanded speed.

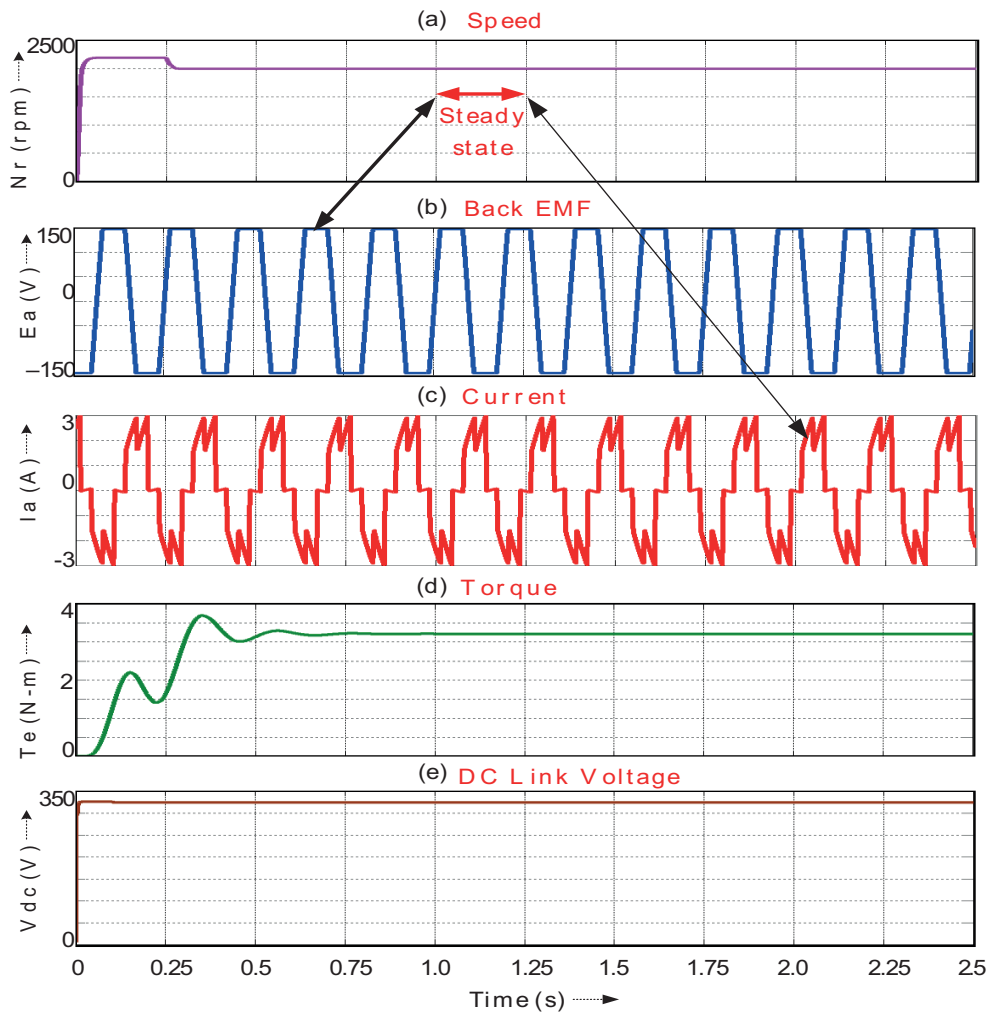


Figure 11. Steady state performance of the proposed BLDC motor drive at 2000 rpm and at 30% of full load condition.

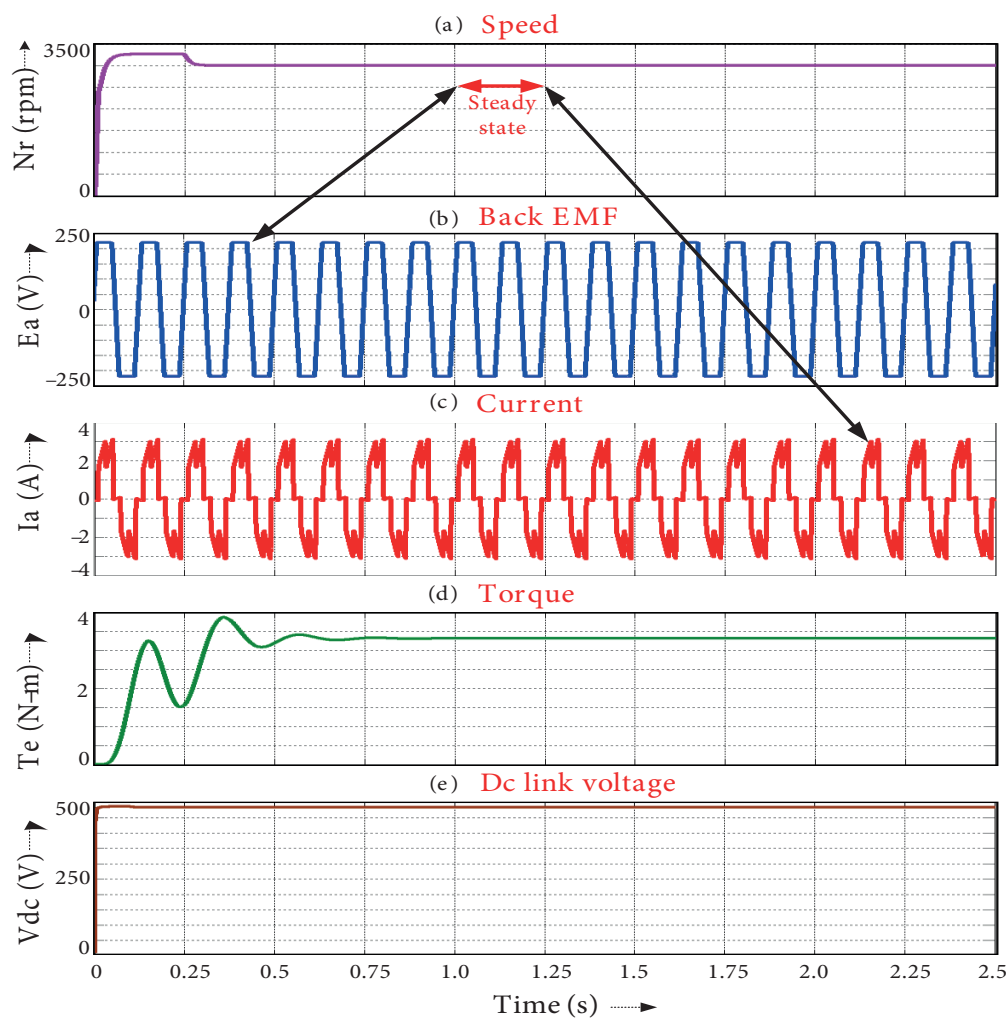


Figure 12. Steady state performance of the proposed BLDC motor drive at 3000 rpm and at 30% of full load condition.

It can be seen from Figures 11(a) and 12(a) that the controller is sufficiently fast in tracking reference speed in approximately 0.25 s. The enlarged views of back EMFs and phase current are shown in Figures 11(b) and 11(c) and 12(b) and 12(c), which are constant for preset load of 3 N-m. Since the load is assumed to be constant, as shown in Figures 11(d) and 12(d), the phase current is also constant. The dc link voltage follows the changes made in commanded speed as can be observed from Figures 11(e) and 12(e).

5.2. Dynamic performance

In order to test the dynamic performance of the proposed control scheme, the desired response of the BLDC drive system is investigated under sudden change in reference speed, issued at $t = 1.5$ s. The response of the system is shown in Figure 13(a) and an enlarged view of speed response, after step change in commanded speed, is shown in Figure 13(b).

The results depicted in Figure 13(b) show that the actual speed attains a steady state value very close to commanded speed, in less than 40 ms, after a step change in reference or commanded speed (3000 to 1500 rpm) is enforced.

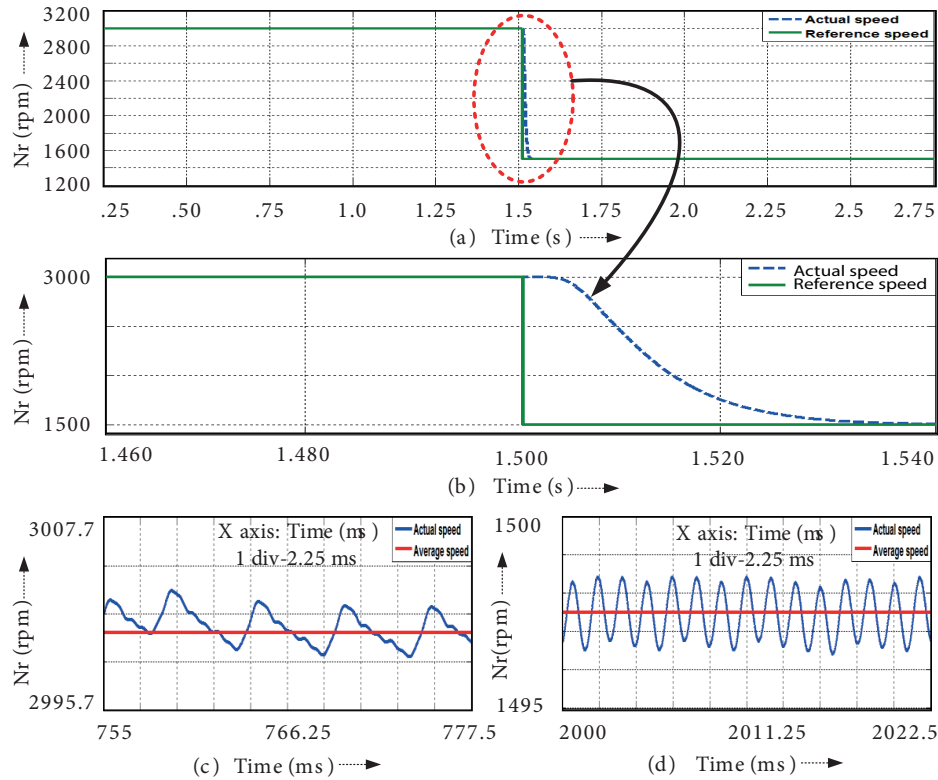


Figure 13. Simulated result, at 30% of full load condition (a) for a step change in reference speed from 3000 to 1500 rpm, (b) enlarged view for step change showing response time and tracking, (c)-(d) zoomed view of actual speed to account for ripples.

The enlarged view of the actual speed spectrum is also shown in Figures 13(c) and 13(d) to assess the average and maximum speed ripple at steady state under the issued change in commanded speed. The effectiveness and efficiency of the proposed control scheme in terms of chosen performance indices such as average and maximum speed error, and maximum speed ripple are presented in Table 3. It can clearly be observed from Figures 13(c) and 13(d) and Table 3 that maximum speed ripple stays well within 5 rpm and percentage average error and percentage maximum error stay less than or equal to 0.23 and 0.26, respectively. Thus the simulation results validate the utility and effectiveness of the proposed control scheme in terms of precise tracking of reference speed. Furthermore, the time taken by the controller to track the commanded speed, after the system has been subjected to a step change in speed, is less than 40 ms, which is an appreciably fast response of the controller.

Moreover, for a step change in commanded speed issued at $t = 1.5$ s and $t = 1.6$ s, the dynamic behavior of the proposed BLDC drive system is investigated against secondary performance indices, which are shown in Figure 14(i) (a). It can be observed from Figure 14(i) (c) that, under the issued changes, the electromagnetic torque regains its steady state value with acceptable values of overshoot in less than 0.5 s after the commanded speed has been changed. As the load torque has been assumed to be constant this makes stator phase current also constant, which can be easily seen from Figure 14(i) (b). It can also be seen from Figure 14(i) (d) that the dc link voltage exactly follows the corresponding changes made in commanded speed. Any change in reference speed is followed by actual speed and the corresponding change in stator phase back EMF is shown in Figure 14(ii).

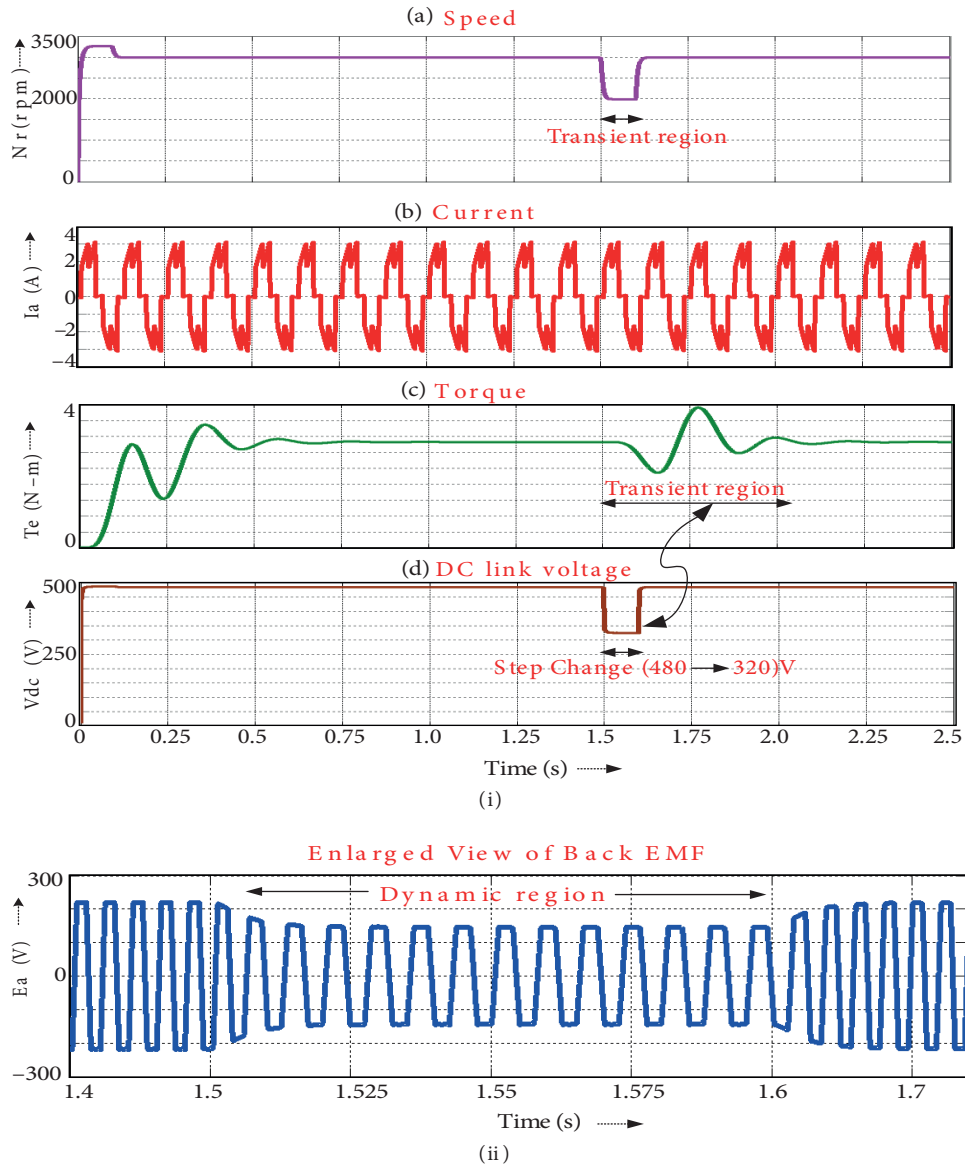


Figure 14. (i) Dynamic performance of the proposed BLDC motor drive during step change in speed, (ii) Enlarged view of back EMF for phase A, at step change in commanded speed issued at $t = 1.5$ and $t = 1.6$, at 30% of rated load.

6. Conclusions

The dual loop control scheme, based on an FPGA, for speed control of a BLDC motor, targeting precise speed control and medium power application such as EVs and HEVs, has been presented in this paper. The proposed control scheme has the following advantages:

1. Simulation results discussed so far illustrate the effectiveness of the control scheme in tracking the commanded speed in a very shorter time and with quite less speed ripple as well.
2. The main attractive feature of the proposed work is the easy and quick realization in real time applications when this control logic is implemented on the XSG platform.

3. The proposed FPGA based PI controller is sufficiently fast in its action of generating the desired dc link voltage from the buck–boost converter and hence the desired speed control.
4. Moreover, the average speed error and maximum speed error are evaluated in order to determine certain further applications of the proposed system. Therefore, the observed dynamic performance of the BLDC drive system has demonstrated the ability of the proposed control scheme to be selectively used for applications that require very high speed accuracy along with fast dynamic response such as biomedical/health care equipment, printing technology, and aerospace applications.

This controller provides far superior performance when the proposed drive system is used for high speed application over the classical zero crossing sensorless approach, which is applicable only in low speed applications. Indeed, the availability of discrete rotor position through a Hall effect sensor and disturbance torque information greatly improves the efficiency and robustness of the system, while decreasing the acoustic noise. This paper, thus, illustrates the feasibility of an accurate speed controller along with the estimator portion of the controller. The implementation of a dual control loop to control speed either via changing dc link voltage with a PI controller or by changing the time interval for conduction state of phases facilitates end to end speed control. Hence the proposed model realized the speed controller for a BLDC motor, which is demanded increasingly, using the FPGA based control scheme. Finally the performance of the system is evaluated in MATLAB/SIMULINK software integrated with the Xilinx system generator.

Nomenclature:

V_{dc}	output voltage of buck–boost converter	R_s	resistance of the stator windings
V_{in}	dc input voltage to buck–boost converter	ψ	amplitude of the flux induced by the permanent magnets of the rotor in the stator phase
D	duty cycle	P	number of pole pairs
f_s	switching frequency	ω_r	angular velocity of rotor
R	load resistance	E_a, E_b, E_c	a, b, and c phase electromotive forces
Δi_{Lo}	range of variation of inductor current	T_e	electromagnetic torque
ΔV_{co}	range of variation of dc link voltage	V_n	maximum voltage from buck–boost converter
i_a, i_b, i_c	a, b, and c phase currents	k	kth sample
L_s	inductance of the stator windings		
V_{ab}, V_{bc}	ab and bc phase to phase voltage		

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