Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2016) 24: 820 – 832

doi:10.3906/elk-1307-159

Design of a high-linear, high-precision analog multiplier, free from body effect

Ali NADERI SAATLO*, İsmail Serdar ÖZOĞUZ
Faculty of Electrical and Electronics Engineering, İstanbul Technical University, Maslak, İstanbul, Turkey

Received: 20.07.2013 • **Accepted/Published Online:** 30.10.2013 • **Final Version:** 23.03.2016

Abstract: In this paper, a new CMOS four-quadrant analog multiplier circuit is proposed, based on a pair of dual-translinear loops. The significant features of the circuit are its high accuracy and high linearity as well as its body effect-free operation, owing to the fact that the circuit relies on a new dual-translinear topology. In addition, harmonic distortions are precisely discussed due to their conceivable mismatches, including transconductance and threshold voltage of the transistors. HSPICE postlayout simulation results are presented to verify the validity of the theoretical analysis, where under a supply voltage of 2.8 V, the bandwidth of the proposed multiplier is 137 MHz, and the corresponding maximum linearity error remains as low as 1.12%. Moreover, the power dissipation of the proposed circuit is found to be 521 μW. The presented multiplier is expected to be useful in the design of various analog signal processing applications such as modulators and frequency doublers, as illustrated in this paper.

Key words: Analog multipliers, current-mode circuits, translinear circuits, body effect

1. Introduction

The four-quadrant multiplier is a very important building block of analog signal processing systems. It has many applications in automatic gain controlling, modulation, frequency translation, square rooting of signals, phase-locked loop, neural network, and fuzzy integrated systems. Many CMOS circuits pertaining to these basic blocks have already been discussed in the literature [1–4]. Ideally, an analog multiplier produces a linear product of 2 input signals, such as x and y, yielding $z = K \times x \times y$, where K is a constant of suitable dimension. Similar to other analog circuits, multiplier circuits can be categorized into 2 main groups: voltage-mode and current-mode. The current-mode multipliers have attracted significant interest and have been extensively investigated in recent years [4–22], thanks to the potential advantages of high-speed operation that are due to low parasitic capacitor nodes, low power consumption, and simple circuitry [5].

The translinear principle is one of the most utilized methods in the design of current-mode circuits, employing loop transistors operating either in the subthreshold region [7–9] or the saturation region [6,10–14]. Although the technique leads to circuits offering low-power consumption in the subthreshold region, the dynamic range and the operation speed of the designed circuits have turned out to be limited. In the saturation region, the conventional translinear circuits are of so-called "stacked" and "up-down" topologies, which are realized using only NMOS or PMOS transistors [6,12,13]. On the other hand, design experiences in the past years indicate that circuits based on the "dual-translinear loops", which consist of both NMOS and PMOS transistors, may offer significant advantages in comparison to the conventional "stacked" or "up-down" topologies in terms of bandwidth, dynamic range, and speed [5,10,11,14], which consist of either NMOS or PMOS transistors.

*Correspondence: naderi@itu.edu.tr

Nonetheless, the body effect is an important problem in circuits based on dual-translinear loops in such a way that this effect causes mismatches in the threshold voltages, which, in turn, influence the linearity and accuracy of the circuit. In some existing analog multipliers, the effect of the transistor mismatches was properly studied and a few techniques were proposed in order to reduce the body effect [15,16]. However, none of these are of dual-translinear configurations, and they suffer from low accuracy and/or low bandwidth.

In addition, the multipliers reported in [3,10,17,21] require dual supply voltage, which is not suitable for integrated circuit design. Another salient feature of multiplier circuits is the four-quadrant operation capability, an important asset that is very useful in various applications [18,19]. Some of the well-known multiplier circuits operate only in one [13,20] or two [17,21,22] quadrants.

In this paper, a new four-quadrant analog multiplier circuit based on the dual-translinear loop is proposed. The key feature of the circuit is being free from body effect, which directly refers to the variation of the transistors' threshold voltage. High linearity, high precision, and a wide dynamic range originating from the dual-translinear loop configuration are further advantages of the circuit. The performance of the proposed multiplier is characterized using Cadence and HSPICE with TSMC level 49 (BSIM3v3) parameters for 0.35-μm CMOS technology.

2. Circuit description

The principle of the proposed multiplier is based on the square-difference algebraic identity, which is $(x+y)^2-(x-y)^2 = 4 \times x \times y$. Thus, the multiplier needs summing, subtraction, and squaring operations. In the current-mode approach, the summation and the subtraction of 2 signals are simply realized by interconnecting the corresponding current output terminals, as a result of Kirchhoff's current law. The design of the squarer and subsequently the multiplier circuit are described below.

Figures 1 and 2 show the proposed squarer and the four-quadrant multiplier circuits, respectively. The squarer circuit is designed based on the translinear principle, and the multiplier circuit consists of 2 dual-translinear loops, where the first loop, consisting of M5, M8, M10, and M12, realizes the $(x+y)^2$ function, while the second loop (M25, M26, M29, M33) provides the $(x-y)^2$ function.

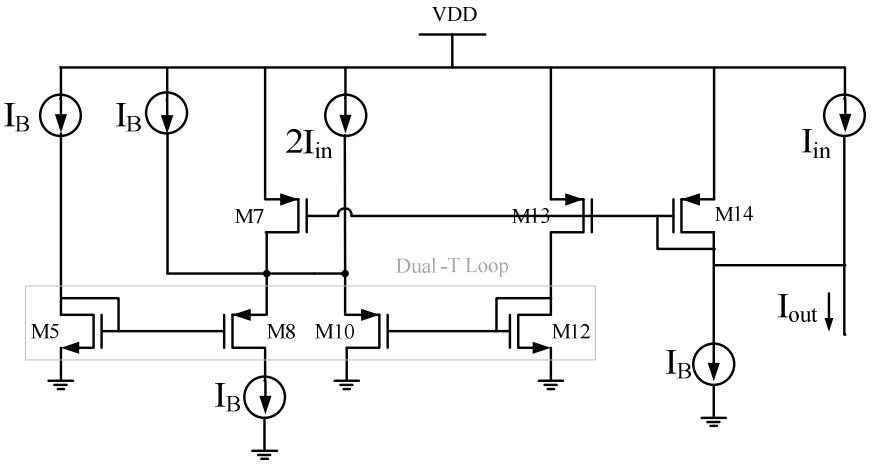

Figure 1. Basic schematic of the proposed squarer circuit.

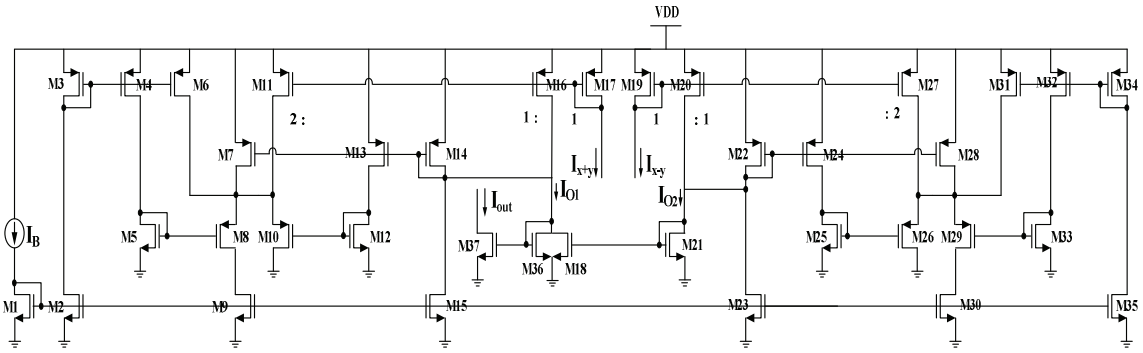

Figure 2. Proposed analog multiplier circuit based on 2 dual-translinear loops.

Let us consider the dual-translinear loop composed of transistors M5, M8, M10, and M12 in Figure 2, which yields:

$$V_{GS5} + V_{GS8} = V_{GS10} + V_{GS12}. \tag{1}$$

Assuming that these transistors are biased in the saturation region and perfectly matched, from the translinear loop principle one can obtain:

$$\sqrt{I_{DS5}} + \sqrt{I_{DS8}} = \sqrt{I_{DS10}} + \sqrt{I_{DS12}}. \tag{2}$$

Since the drain currents I_{DS5} and I_{DS8} are equal to a constant current source, i.e. I_B, one can easily express the drain currents of M10 and M12 as follows:

$$I_{DS10} = I_{O1} + I_{x+y} + I_B, \tag{3}$$

$$I_{DS12} = I_{O1} - I_{x+y} + I_B. \tag{4}$$

Substituting Eqs. (3) and (4) into Eq. (2) and taking the square of both sides, we have:

$$2\sqrt{I_B} = \sqrt{I_B + I_{O1} - I_{x+y}} + \sqrt{I_B + I_{O1} + I_{x+y}}, \tag{5}$$

$$4I_B = 2I_B + 2I_{O1} + 2\sqrt{I_B^2 + I_{O1}^2 + 2I_B I_{O1} - I_{x+y}^2}. \tag{6}$$

By squaring both sides again, the output current can be written as:

$$I_{O1} = \frac{I_{x+y}^2}{4I_B}. \tag{7}$$

It can be seen from Eq. (7) that the current I_{O1} is the square of the input current; hence, this subcircuit is the basic building block of the CMOS analog multiplier. The same procedure can be followed for the second translinear loop to obtain I_{O2}.

To design the four-quadrant multiplier, the output of the squarer circuit that resulted from the positive input current should remain the same while the input becomes negative. Considering Figure 2 and the first translinear loop, by changing the polarity of the input current (positive into negative or vice versa), the currents of M10 and M12 can be rewritten as:

$$I_{DS10} = I_{O1} - I_{x+y} + I_B, \tag{8}$$

$$I_{DS12} = I_{O1} + I_{x+y} + I_B. \tag{9}$$

The only difference is that the corresponding terms in Eqs. (3) and (4) are interchanged, although the output current is still the same.

M18, M21, M31, and M37 form a current subtraction of two squarer circuits as:

$$I_{out} = I_{O1} - I_{O2} = \frac{(I_x + I_y)^2}{4I_B} - \frac{(I_x - I_y)^2}{4I_B} = \frac{I_x I_y}{I_B}. \tag{10}$$

Thus, Eq. (10) yields the multiplication of I_x and I_y divided by the constant current of I_B, which is normalized to one. The signals I_{x+y} and I_{x-y} are realized using an additional input stage composed of simple current mirrors (see Figure 3).

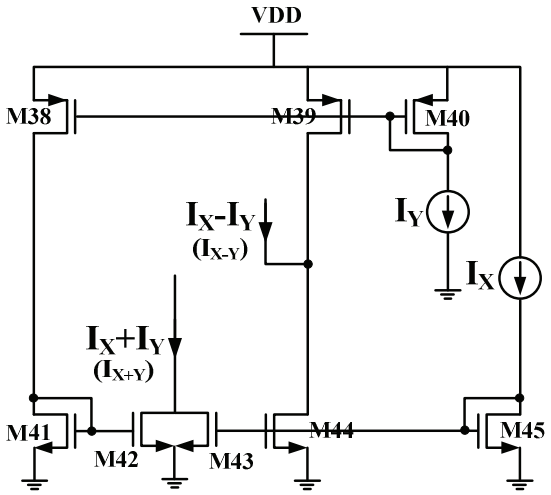

Figure 3. Additional circuit to provide required currents to the multiplier circuit.

The next section provides a performance analysis of the circuit and deviations from ideal assumptions, followed by supporting simulation results.

3. Performance analysis

In this section, the harmonic distortion caused by a mismatch in the input stage transistors, which leads to errors in currents I_{x+y} and I_{x-y}, is studied in detail. Afterwards, the effects of the mismatches in the transconductance parameters of the transistors in the dual-translinear loops, as well as the mismatch in the threshold voltages due to transistor body effects, are thoroughly analyzed. Finally, the input/output ranges and impedances of the proposed multiplier are derived.

3.1. Input current mismatch

The proposed multiplier requires 2 well-matched input signals (I_x and I_y). It is worthwhile to mention that the mismatch in the input signals leads to second harmonic distortion terms at the output of the multiplier circuit.

Each input current can be defined as follows in terms of possible mismatches:

$$I_{xi} = \hat{I}_x + \Delta x_i \hat{I}_x, \tag{11}$$

$$I_{yi} = \hat{I}_y + \Delta y_i \hat{I}_y, \quad \text{for} \quad I = 1, 2, \tag{12}$$

where $\hat{I}_x$ and $\hat{I}_y$ are mean values, and Δx_i and Δy_i are mismatch percentages of $\hat{I}_{xi}$ and $\hat{I}_{yi}$, respectively. By applying $\hat{I}_x + \hat{I}_y$ and $\hat{I}_x - \hat{I}_y$ to the multiplier circuit, and considering Δx_i^2, Δy_i^2, and $\Delta x_i \Delta y_i << 1$, the output current is given by:

$$I'_{out} \approx \frac{\hat{I}_x \hat{I}_y}{I_B} + \frac{\delta_x \hat{I}_x^2 + \hat{I}_x \hat{I}_y (\delta_x + \delta_y) + \delta_y \hat{I}_y^2}{2I_B}, \tag{13}$$

where:

$$\delta_x = \Delta x_1 - \Delta x_2, \tag{14}$$

$$\delta_y = \Delta y_1 - \Delta y_2. \tag{15}$$

If one of the inputs ($\hat{I}_x$) is kept constant and the other is sinusoidal in the form of $\hat{I}_y = \hat{i}_m \sin \omega t$, the second harmonic distortion with respect to the input signal mismatches can be derived as follows:

$$HD_2 = \frac{\delta_x}{\hat{I}_x (\delta_x + \delta_y) + 2\hat{I}_x} \hat{i}_m. \tag{16}$$

It should be pointed out that when the mismatch percentage of $\hat{I}_x$ increases (see Eq. (16)), the second harmonic distortion also increases (decrease in dB). Nonetheless, it remains nearly steady and does not significantly affect the third harmonic distortion, as it did not appear in the hand calculations.

3.2. Transconductance parameter mismatch

In this section, a detailed analysis of the mismatch between the transconductance parameters of the NMOS and PMOS transistors is provided, and the errors affecting the ideal performance of the proposed circuit are studied.

The mismatch of the transconductance parameter can be modeled as follows:

$$K_P = K + \Delta k K, \tag{17}$$

$$K_N = K - \Delta k K, \tag{18}$$

where K is a mean value and Δk is a mismatch percentage of the transconductance parameter. Assuming this, Eq. (2) becomes:

$$\sqrt{\frac{I_B}{K + \Delta k K}} + \sqrt{\frac{I_B}{K - \Delta k K}} = \sqrt{\frac{I''_{O1} + I_{x+y} + I_B}{K + \Delta k K}} + \sqrt{\frac{I''_{O1} - I_{x+y} + I_B}{K - \Delta k K}}. \tag{19}$$

Simplifying Eq. (19) and ignoring the terms containing Δk^2 (because $\Delta k << 1$), the output current of the squarer circuit can be written as:

$$I''_{O1} \approx \frac{I_{x+y}^2 + 2\Delta k I_B I_{x+y}}{4I_B + 2\Delta k I_{x+y}}. \tag{20}$$

Eq. (20) implies that the transconductance mismatch leads to the slope and offset at the output of the squarer circuit. By applying summation and subtraction of the signals to the proposed multiplier circuit, one can express the output current as:

$$I''_{out} = I''_{O1} - I''_{O2} \approx \frac{4I_B^2 I_y \Delta k + 4I_x I_y I_B + I_x^2 I_y \Delta k - I_y^3 \Delta k}{4I_B^2 + 4I_B I_x \Delta k}. \tag{21}$$

Applying $\hat{I}_x$ as a constant current and $\hat{I}_y = \hat{i}_m \sin\omega t$, the third harmonic distortion caused by the transconductance parameter mismatch is given by:

$$HD_3 = \frac{\Delta k}{16I_B^2 \Delta k + 4I_x^2 \Delta k + 16I_B I_x + 3\Delta k} \hat{i}_m^2. \tag{22}$$

In short, when the transconductance mismatch of loop transistors increases, the third harmonic distortion increases simultaneously (decrease in dB), whereas the second harmonic distortion is hardly affected.

3.3. Error due to body effect and threshold voltage mismatch

In Section 2, the body effect that influences the threshold voltages of the loop transistors was ignored to simplify the basic circuit calculations. This section investigates the effect of this nonideality on the circuit performance.

In an MOS transistor, body effect refers to the change in the transistor threshold voltage (V_{TH}) resulting from a voltage difference between the transistor source and substrate, which can be characterized by:

$$V_{TH} = V_{t0} + \gamma[\sqrt{(VSB + |2\varphi_F|)} - \sqrt{|2\varphi_F|}], \tag{23}$$

where V_{t0} is the zero-bias threshold voltage, γ is the body effect coefficient, and φ_F is the Fermi potential.

Considering a nonideal case for equality of threshold voltages for NMOS and PMOS transistors in one of the dual-translinear loops, and subsequently rewriting Eq. (2), we have:

$$V_{TH5} + \sqrt{\frac{I_{DS5}}{K_5}} + V_{TH8} + \sqrt{\frac{I_{DS8}}{K_8}} = V_{TH10} + \sqrt{\frac{I_{DS10}}{K_{10}}} + V_{TH12} + \sqrt{\frac{I_{DS12}}{K_{12}}}. \tag{24}$$

Since the sources of M8 and M10 are tied to the same node, V_{SB8} and V_{SB10} are equal; as a result, V_{TH8} and V_{TH10} are modified equally by body effect. Therefore, there is no requirement for separate wells to obtain the $V_{TH8} = V_{TH10}$ equality, although it is possible. Similarly, since V_{SB5} and V_{SB12} are zero, V_{TH5} and V_{TH12} are not affected by body effect, and this results in their equality (equal to V_{t0}). This causes V_{TH5} and V_{TH8} to cancel out V_{TH10} and V_{TH12}, respectively, and Eq. (2) can be written accordingly.

3.4. Input/output ranges and impedances

The input dynamic range of the multiplier is restricted by the dual-translinear loop transistors, which should operate in the saturation region.

To determine this range in terms of bias current, we assume that $I_{in} = \beta I_B$, and we rewrite Eq. (2) as follows:

$$2\sqrt{I_B} \geq \sqrt{(1-\beta)I_B + \frac{\beta^2 I_B}{4}} + \sqrt{(1+\beta)I_B + \frac{\beta^2 I_B}{4}}. \tag{25}$$

Solving this inequality gives $-2I_B \leq I_{in(SQ)} \leq 2I_B$ as an input range of the squarer circuit, and $-I_B \leq I_{in(MUL)} \leq I_B$ for the multiplier circuit. In addition, one can find the output ranges as $0 \leq I_{out(SQ)} \leq I_B$ and $-I_B \leq I_{out(MUL)} \leq I_B$ for the squarer and multiplier circuits, respectively.

It should be noted that high output impedance is an important characteristic of the current-mode circuits. The proposed circuit enjoys this feature by providing an output impedance equal to the intrinsic drain-source resistance of M37. Although the typical value of this impedance is sufficiently high for many applications, higher output impedance can be further achieved by using cascade-connected transistors instead of M18, M21, M36, and M37, where the bias current is chosen as 10 μA. On the other hand, small input impedance is an equally important asset of current-mode circuits. Considering Figure 3 as the input stage of the circuit and I_X and I_Y as the input currents, it is easy to verify that the input impedances are equal to $1/g_{m45}$ and $1/g_{m40}$, respectively.

4. Postlayout simulation results

In this section, postlayout simulations are presented using Cadence and HSPICE, with TSMC level 49 (BSIM3v3) parameters for 0.35-μm CMOS technology so as to verify the performance of the proposed circuit.

Figure 4 shows the layout of the multiplier circuit drawn by a single poly and 2 metals (Metal 1 and Metal 2), whose area is 39.95 $\times$ 40.15 μm.

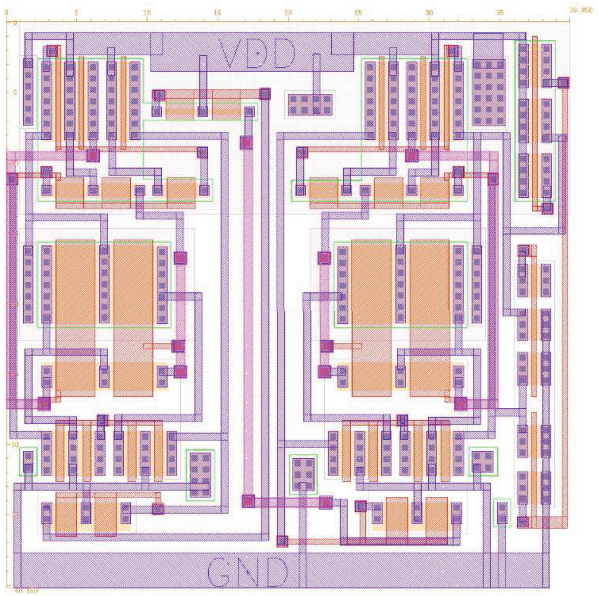

Figure 4. Layout of proposed analog multiplier.

The aspect ratio of the transistors is given in Table 1. The supply voltage is 2.8 V, and I_B is set to 10 μA.

Figure 5 shows the DC transfer characteristics of the proposed analog multiplier, which illustrates high linearity in the mentioned range of the inputs, where the output current shifts between –10 μA and +10 μA. Within this range, the measured nonlinearity error is 1.12%.

Table 1. Transistor aspect ratios.

Transistor name	W/L (μm/μm)
M1, M2, M9, M15, M23, M30, M35	3.2/0.6
M7, M13, M14, M22, M24, M28	5.6/0.35
M3, M4, M6, M31, M32, M34	1/2
M16, M17, M19, M20	4/0.35
M5, M12, M25, M33	2/2.8
M8, M10, M26, M29	5.6/2.8
M11, M27	8/0.35
M18, M21, M36, M37	2/ 0.6
M38–M40	3/0.5
M41–M45	2/0.5

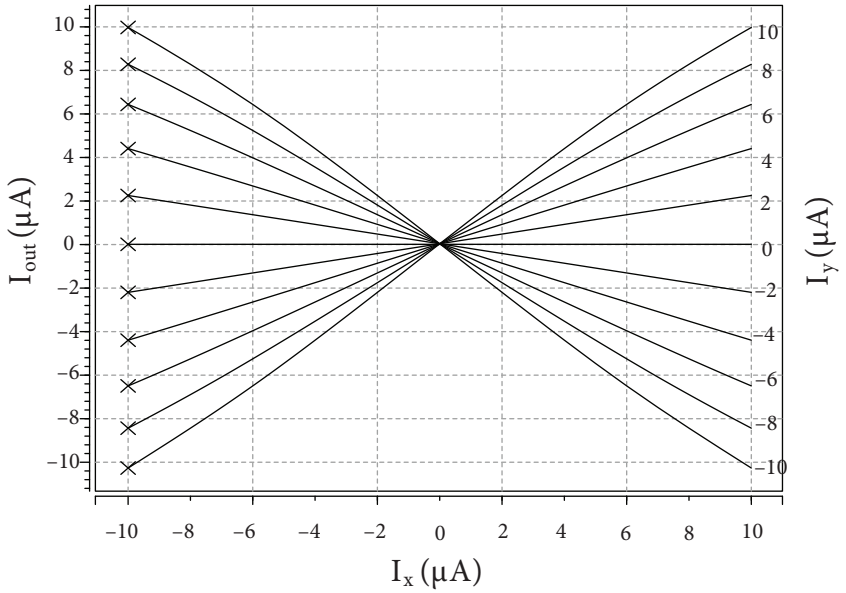

Figure 5. Postlayout simulation result for DC transfer characteristics.

Figure 6 shows the multiplier being used as a balance modulator. I_x and I_y are 1 MHz and 100 kHz, respectively; 20 μA_{P-P} sinusoidal carrier and modulation signals are fed to the inputs of the proposed multiplier, while I_B is constant. Figure 7 shows how the multiplier circuit can be employed as a frequency doubler. If both frequencies of the input currents are 1 MHz, the figure shows the corresponding output waveform with double frequency as well as the error quantity.

The total harmonic distortion versus input signal at 100 kHz and 1 MHz is shown in Figure 8. In the worst case, an input signal of 20 μA_{P-P} at a frequency of 1 MHz resulted in a total harmonic distortion of less than 1.45%. The simulation results in Figures 9 and 10 verify the hand calculations of the harmonic distortions in the previous section, where second and third harmonic distortions versus mismatch percentage of input signals and transconductance were achieved.

Figure 11 shows the threshold voltage difference of NMOS and PMOS transistors in the dual-translinear loop versus different inputs, where I_x shifts from –10 μA to +10 μA while I_y is constant (10 μA).

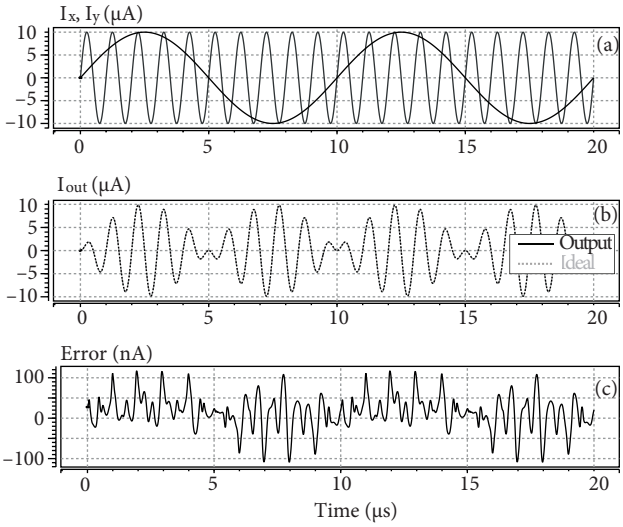

Figure 6. The proposed multiplier as an amplitude modulator: a) 100 kHz modulating signal and 1 MHz carrier signal; b) modulated output; c) error measurement.

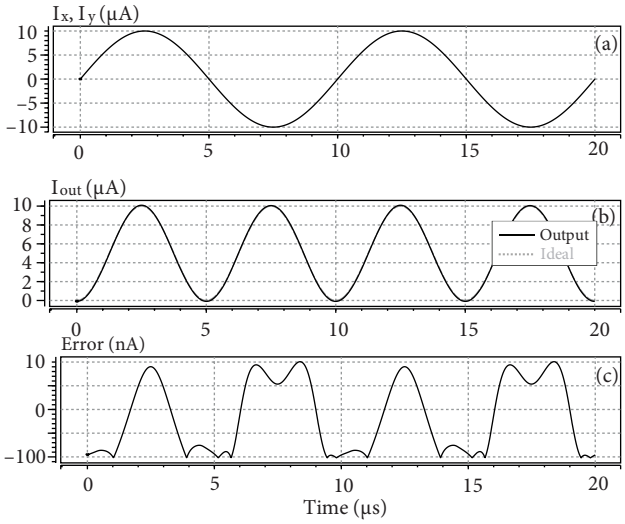

Figure 7. The proposed multiplier as a frequency doubler: a) input waveform; b) output waveform; c) error measurement.

The Monte Carlo analysis of the proposed circuit with 15 iterations was carried out by applying 5% of mismatch in the transistors' aspect ratio and threshold voltage with Gaussian distribution. This was done to ensure the robustness of the circuit performance against the fabrication process (Figure 12).

Frequency response of the circuit shows that –3 dB bandwidth is 137 MHz when the input signal is applied to I_x, and $I_y = 10\ \mu$A. Maximum power consumption obtained is 0.521 mW.

Table 2 summarizes some relevant results of the proposed multiplier and allows a more detailed comparison. Please note that in comparison to [11] (in 0.25 μm), speed was sacrificed in the design at the expense of accuracy, as shown in Figures 6 and 7. In addition, to improve the linearity of the multiplier circuit, fairly large gate-length transistors were used, which affected the bandwidth of the circuit. Owing to the design of a specific

topology of the dual-translinear loop, power consumption is slightly higher than in prior works. Nevertheless, this work is free from body effect and insensitive to threshold voltage variation.

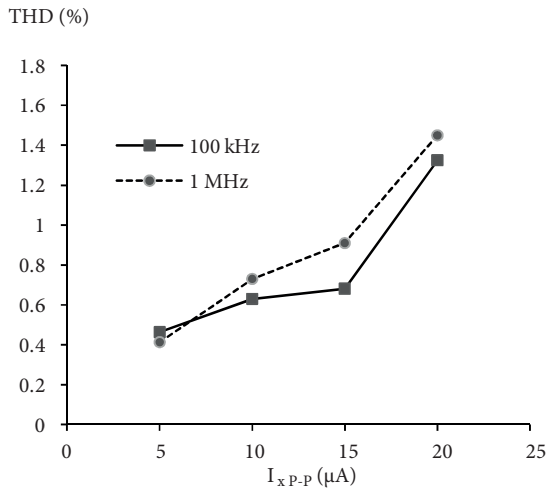

Figure 8. Relation between total harmonic distortion and I_x.

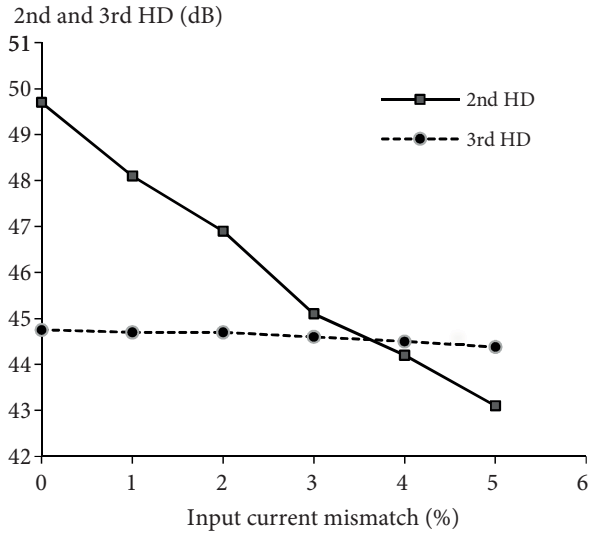

Figure 9. Input current mismatch as a factor of second harmonic distortion.

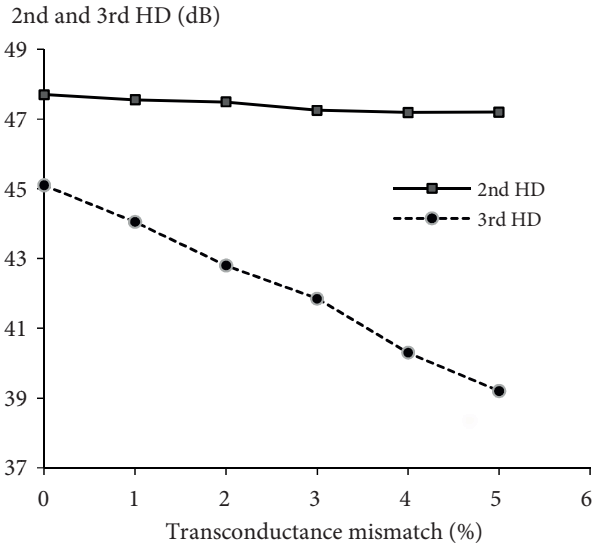

Figure 10. Transconductance mismatch as a factor of third harmonic distortion.

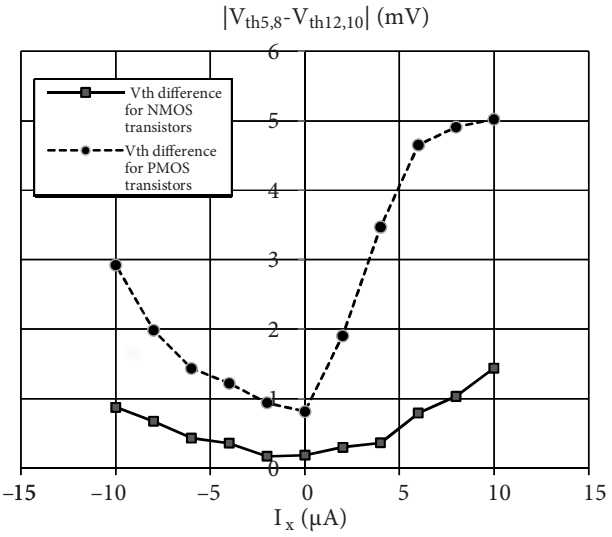

Figure 11. Threshold voltage difference of NMOS and PMOS transistors in the dual-translinear loop versus different inputs.

5. Conclusion

A new all-MOS analog multiplier was presented, having the capability of operation in four-quadrant. The circuit relies on the specific topology of the dual-translinear loop to omit the body effect of the multiplier circuit. High linearity and high accuracy were significant characteristics of the circuit. To study the performance of the proposed circuit, input and output range were thoroughly discussed and harmonic distortion analysis

Table 2. Comparative parameters of the proposed multiplier and other recent works.

	[22]	[12]	[11]	[10]	[5]	[4]	[3]	This work
Translinear type/method	Triode	Up-down	Dual	Dual	Dual	Subthreshold	CCCII+	Dual
Sensitivity to body effect	Dependent	Free	Dependent	Dependent	Dependent	Dependent	-	Free
Power consumption (mW)	2	0.6	0.17	0.46	0.34	0.067	3.82	0.521
Power supply (V)	3.3	3.3	2.5	±1.5	3.3	1.5	±2.5	2.8
Total harmonic distortion (%) (1 MHz to 20 μA)	0.2 (100 kHz)	1.5 (10 kHz)	0.91	3.7	0.97	4.2 (10 kHz)	0.5 (100 kHz)	1.45
Nonlinearity (%)	2.5	1.9	2.5	1.20	1.1	3.2	-	1.12
–3 dB bandwidth (MHz)	3	3	278	19	41.8	0.268	44.5	137
Technique (μm)	0.5	2.4	0.25	0.5	0.35	0.35	CBICR model	0.35
Area ($mm^{2)}$	0.083	0.24	0.033	-	0.009	-	-	0.016
Simulation (Sim.) or measurement (Meas.)	Meas.	Meas.	Postlayout	Sim.	Sim.	Sim.	Sim.	Postlayout

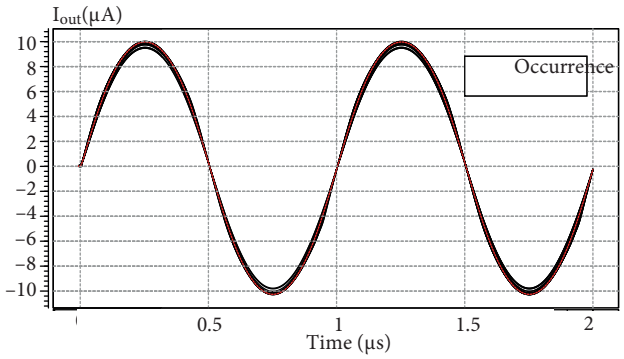

Figure 12. Monte Carlo analysis of the multiplier circuit for 5% mismatch in transistors' aspect ratio and threshold voltage.

was performed. In addition, the effects of mismatch in the transconductance parameters of the transistors in the dual-translinear loops as well as mismatch in the threshold voltages were analyzed. In order to simulate the proposed circuit, the Cadence design tool and HSPICE simulator were utilized to verify the validity of the theoretical analysis. To illustrate the efficiency of the presented multiplier, it was employed as a balance modulator and frequency doubler, and the simulation results were compared with an ideal performance of these applications. The presented topology of the dual-translinear loop consumed slightly more power than that of prior works. In view of this result, future work on low-voltage, low-power methods such as level-shifting techniques can be proposed.

References

[1] Choi J, Park J, Kim W, Lim K, Laskar J. High multiplication factor capacitor multiplier for an on-chip PLL loop filter. Electron Lett 2009; 45: 239–240.

[2] Shin M, Grigoryan V, Kumar P. Frequency-doubling optoelectronic oscillator for generating high-frequency microwave signals with low phase noise. Electron Lett 2007; 43: 242–244.

[3] Yuce E. Design of a simple current-mode multiplier topology using a single CCCII+. IEEE T Instrum Meas 2008; 57: 631–637.

[4] Liu W, Liu SI. Design of a CMOS low-power and low-voltage four-quadrant analog multiplier. Analog Integr Circ S 2010; 63: 307–312.

[5] Naderi A, Khoei A, Hadidi K, Ghasemzadeh H. A new high speed and low power four-quadrant CMOS analog multiplier in current mode. Int J Electron Comm 2009; 63: 769–775.

[6] Tanno K, Ishizuka O, Tang Z. Four-quadrant CMOS current-mode multiplier independent of device parameters. IEEE T Circuits Syst 2000; 47: 473–477.

[7] Wu R, Xing J. MOS translinear principle based analog four-quadrant multiplier. In: IEEE 2012 International Conference on Anti-Counterfeiting, Security and Identification; 24–26 August 2012; Taipei, Taiwan. New York, NY, USA: IEEE. pp. 1–4.

[8] Andreou A, Boahen KA. Translinear circuits in subthreshold CMOS. Analog Integr Circ S 1996; 9: 141–166.

[9] Gravati M, Valle M, Ferri G, Guerrini N, Reyes L. A novel current-mode very low power analog CMOS four quadrant multiplier. In: IEEE 2005 Solid State Circuits Conference; 12–16 September 2005; Grenoble, France. New York, NY, USA: IEEE. pp. 495–498.

[10] Kumngern M, Kobchai D. Versatile dual-mode class-AB four-quadrant analog multiplier. Int J Signal Process 2005; 2: 214–221.

[11] Alikhani A, Ahmadi A. A novel current-mode four-quadrant CMOS analog multiplier/divider. Int J Electron Comm 2012; 66: 581–586.

[12] López-Martín A, Carlosena A. Current-mode multiplier/divider circuits based on the MOS translinear principle. Analog Integr Circ S 2001; 28: 265–278.

[13] Menekay S, Tarcan R, Kuntman H. Novel high-precision current-mode circuits based on the MOS-translinear principle. Int J Electron Comm 2009; 63: 992–997.

[14] Kaedi S, Farshidi E. A new low voltage four-quadrant current mode multiplier. In: IEEE 2012 20th Iranian Conference on Electrical Engineering; 15–17 May 2012; Tehran, Iran. New York, NY, USA: IEEE. pp. 160–164.

[15] Chaisayun I, Piangprantong S, Dejhan K. Versatile analog squarer and multiplier free from body effect. Analog Integr Circ S 2012; 71: 539–547.

[16] Ibaragi E, Hyogo A, Sekine K. A CMOS analog multiplier free from mobility reduction and body effect. Analog Integr Circ S 2000; 25: 281–290.

[17] Lopez-Martin A, de La Cruz Blas C, Ramirez-Angulo J, Carvajal RG. Current mode CMOS multiplier/divider circuit operating in linear/saturation regions. Analog Integr Circ S 2011; 66: 299–302.

[18] Ryan, C. Applications of a four-quadrant multiplier. IEEE J Solid-St Circ 1970; 5: 45–48.

[19] El-Atta MA, El-Ela A, El Said MK. Four-quadrant current multiplier and its application as a phase-detector. In: Proceedings of the 19th National Radio Science Conference; 21 March 2002; Alexandria, VA, USA. New York, NY, USA: IEEE. pp. 502–508.

[20] De la Cruz-Blas C, López-Martín A, Carlosena A. 1.5-V MOS translinear loops with improved dynamic range and their applications to current-mode signal processing. IEEE T Circuits Syst 2003; 50: 918–927.

[21] Siripruchyanun M, Jaikla W. A current-mode analog multiplier/divider based on CCCDTA. Int J Electron Comm 2008; 62: 223–227.

[22] Miguel JMA, de la Cruz Blas C, Lopez-Martin A. Fully differential current-mode CMOS triode translinear multiplier. IEEE T Circuits Syst 2011; 58: 21–25.