

Three-phase multilevel inverter with high value of resolution per switch employing a space vector modulation control scheme

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Abstract: A special cascaded configuration of asymmetric multilevel inverter is presented in this paper. This configuration cancels the redundancy of output voltage steps and maximizes the number of levels in the output voltage. This structure is built by using series connected stages, which minimize the number of semiconductor switches, gate drive arrangements, occupying area, and cost. It is a modular type inverter model and the number of voltage levels can be increased by adding new stages without changing the previous connection. Space vector modulation has been applied as the control strategy. A prototype of the proposed inverter topology has been built in the laboratory. The attached hardware results indicate the accuracy of the proposed model, which include the topology as well as the control technique.

Key words: Cascaded multilevel inverter, space vector control, core unit, THD, modular type

1. Introduction

Neutral point clamped topology was the first multilevel inverter (MLI), proposed by Nabae et al. [1]. The MLI topologies can be categorized in three basic groups: the neutral point clamped (NPC) MLI, flying capacitor (FC) MLI, and cascaded H-bridge (CHB) MLI [2–4].

The CHB MLI consists of a number of H-bridge units. The final output voltage is synthesized by the combination of the input dc voltages of all series connected units [5,6]. H-bridge units may have low voltage components. This topology has a modular characteristic, since all the units are similar and the control strategy is the same for all the units. Therefore, it is very easy to replace if any unit becomes faulty. Even without discontinuing the load, it is possible to bypass the faulty module by applying an efficient control technique [7].

The CHB topology can be divided into two groups: symmetric structure and asymmetric structure. In the case of the symmetric structure, there are equal dc sources and N-numbers of H-bridge cells per phase arm. The number of levels in the output voltage should be $2N+1$. All the units are similar. Each unit consist of four switches and one isolated input dc source, which can be obtained by single-phase or three-phase diode-based rectifier arrangement [8,9]. Transformers are used to ensure proper electrical isolation. Nowadays, high frequency link transformer (HFL) based modules have been used for efficient design [9,10]. During high power applications the conventional diode rectifier based dc–dc converters become bulky, but a high frequency link dc–dc converter reduces the size of the transformer [11]. These HFLs are also well suited for regenerative applications.

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Unequal input dc supplies are used in asymmetrical cascaded H-bridge (ACHB) inverters [12]. This configuration provides the best option to increase the number of levels in the output voltage, with remarkable reduction in total harmonic distortion (THD) and semiconductor switching losses. It shows high efficiency (up to 80%) at the fundamental frequency [13,14].

On the other hand, the number of levels in the output voltage is maximized in ACHB topology, when the input dc voltages are arranged in a ratio of three geometric sequences [15]. This ratio is very useful to design high number of levels generation and therefore it shows a small voltage distortion [16,17]. Research shows that the conventional high frequency PWM control technique is not enough for this ratio of three dc source configuration, since the high voltage stage faces high switching loss for high switching frequency [18–20].

Nowadays, the CHB inverter is developing by multilevel dc-link and it gives a high number of levels in the final output AC voltage [21]. Actually, the multilevel dc-link voltage can be generated using cascaded NPC or FC topologies [22]. The multilevel dc link voltage is supplied to a full bridge inverter and the full bridge inverter generates the bipolar AC voltage. These configurations are applicable for high power applications. The inverter topology based on the multilevel dc link topology and a full bridge inverter configuration has been presented in [23]. However, the dc-link voltage topology becomes inefficient if the symmetrical cascaded method is applied, when the input dc supplies are equal to each other [22,24]. A new family of ACHB inverter topology has been presented in [25], where a higher number of voltage levels is possible without using the full bridge inverter [24]. An algorithm to choose the dc sources has been presented. However, the given algorithm does not serve in creating all the output voltage levels (odd and even). A large number of switches are required to produce a certain number of levels in the output voltage. The aforementioned problems have been overcome in [26], where it is possible to generate all the even and odd levels [27]. It is important to note that both of the configurations in [28] focus on reducing the number of semiconductor switches and gate driver circuits. However, the topology was not extended for three-phase configuration. Even the inverter model does not explain any control technique.

This paper proposes a special topology for a three-phase asymmetrical cascaded multilevel inverter with maximum number of odd and even levels. The proposed topology emphasizes the reduction of semiconductor switches, gate drive circuits, voltage stress on the switches, installation area, cost, and semiconductor losses. The input dc supplies are selected in such a way that the output gives the maximum voltage level.

The first section of this paper shows the research advances in present cascaded multilevel inverter topologies. In section 2, the proposed topology has been explained properly in terms of working principles, voltage levels, and selection of input dc voltages. Section 3 explains the modulation technique in detail. In Section 4, the performances of the inverter have been analyzed with respect to different modulation indexes and the inverter has been verified for n-number of voltage levels. Section 5 presents a brief comparison between the proposed topology and the existing common multilevel inverter topologies. Lastly, the semiconductor losses have been presented in section 6.

2. Operational principle of the proposed MLI

Figure 1a shows the core unit of the proposed inverter. Here, two switches are used with one input dc voltage to get output two dc voltage levels 0 and V . S_1 and S_2 are always in complementary mode. When the switch S_1 is ON it gives $V_o = V$ and when S_2 is ON $V_o = 0$. However, S_1 and S_2 are never switched on at the same time to avoid short circuit. Table 1 shows the different switching sequences of the basic core unit.

Figure 1b shows a complete three-phase configuration of the proposed asymmetrical cascaded inverter topology for ‘n’-level. Each of the phase arms consists of a number of core units and all the core units are

connected in series. A certain number of core units are chosen in each phase arm to the get desired number of levels in the output voltage. In Figure 1b, it works under asymmetrical topology since the input dc sources are unequal to each other.

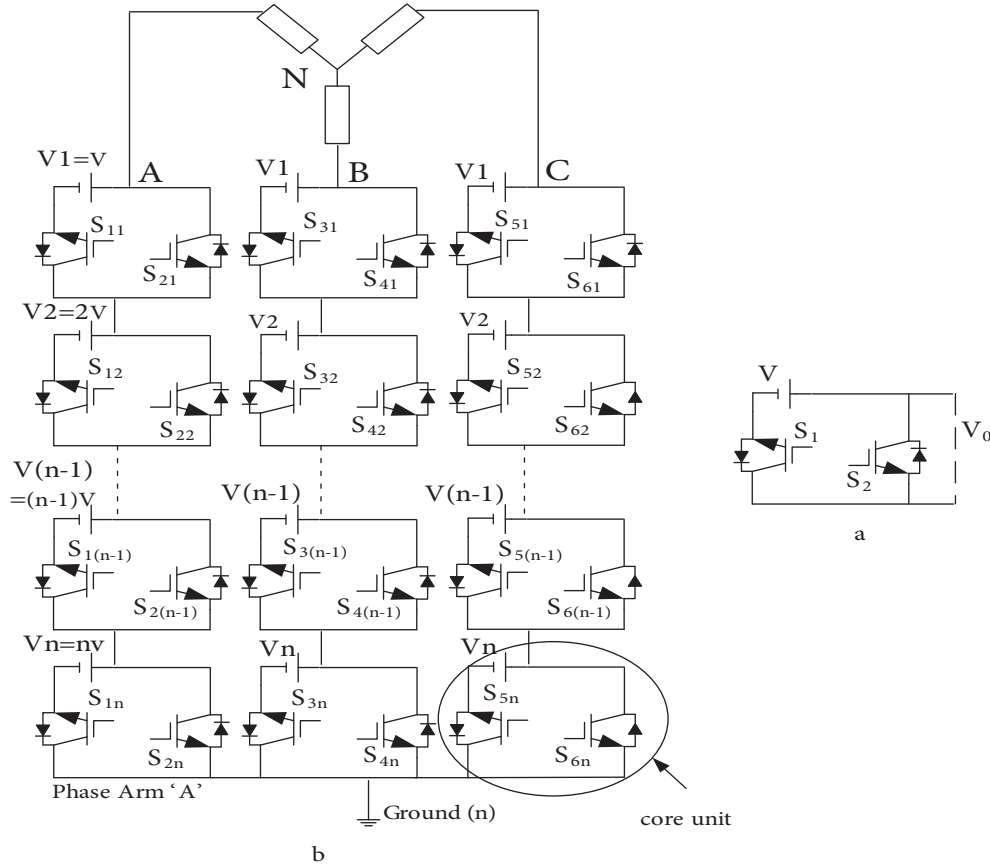


Figure 1. a. The core unit, b. the proposed 3-phase n-level asymmetrical cascade inverter.

Table 1. Switching states of the basic auxiliary cell.

State	Switching states		V ₀
	S ₁	S ₂	
1	ON	OFF	V
2	OFF	ON	0

To get a very high number of output voltage levels requires a high number of isolated input dc supplies. In such case, the dc supplies can be replaced by renewable energy sources like photovoltaic or fuel cells. Even high frequency toroid transformer link supply may be applied for managing all the input dc supply [9]. The value of each core unit input dc supply for any phase arm can be presented as follows (according to Figure 1b):

$$V_1 = V; V_2 = 2V; V_3 = 3V; \dots; V_n = nV \tag{1}$$

where n = number of stages = 1, 2, 3, 4...

The node voltage ($T = v_{A_n} \text{ or } v_{B_n} \text{ or } v_{C_n}$) from phase arm top (A or B or C) to ground (n) is synthesized by summing the output voltages of all the core units for a certain phase arm. This can be expressed in Eq. (2).

$$T = V_1 + V_2 + V_3 + \dots + V_n \tag{2}$$

The maximum output multilevel node voltage (T) can be obtained by combining (1) and (2)

$$T = V + 2V + 3V + \dots + nV \tag{3}$$

$$T = (1 + 2 + 3 + \dots + n)V = V \sum_{i=1}^n i \ , \tag{4}$$

where n = number of stages or number of core units per phase arm = 1, 2, 3, ...

The number of generated levels in the output AC line voltages can be written by Eq. (5).

$$l = (2 \sum_{i=1}^n i) + 1 \tag{5}$$

Here n is the number of stages.

The line-to-line voltages can be calculated from the pole inverter voltages $v_{An}, v_{Bn}, \text{ and } v_{Cn}$ are given by Eq. (6):

$$v_{AB} = v_{An} - v_{Bn}, \quad v_{BC} = v_{Bn} - v_{Cn}, \quad v_{CA} = v_{Cn} - v_{An} \tag{6}$$

The phase voltages $v_{AN}, v_{BN},$ and v_{CN} of Y-connected balanced three-phase loads are related to the pole voltages and that can be calculated by Eq. (7):

$$\begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{An} \\ v_{Bn} \\ v_{Cn} \end{bmatrix} \tag{7}$$

Using Park's transformation, the voltage vector of any inverter state can be identified by Eq. (8).

$$\begin{bmatrix} v_D \\ v_Q \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{AN} \\ v_{BN} \\ v_{CN} \end{bmatrix} \tag{8}$$

The voltage vector approximation method is well suited for inverters with a large number of levels. The l -level inverter has $[3 \times l \times (l-1) + 1]$ equally spaced voltage vectors in its voltage space diagram.

3. Operational principle of the proposed MLI

Space vector modulation has been applied successfully as a control strategy. According to Figure 1b, the number of levels in the output line voltage can be expressed as $N_{level} = (2 \sum_{i=1}^n i) + 1$. Actually each switching state generates specific node voltages (v_{An}, v_{An}, v_{Cn}) with respect to the reference neutral point (n) of the dc bus voltage. This can be presented by Eq. (9).

$$v_{An} = k_A V_{dc}, v_{Bn} = k_B V_{dc}, v_{Cn} = k_C V_{dc} \tag{9}$$

Here k_A, k_B , and $k_C \in [0, 1, 2, \dots, n]$ and the switching states of the inverter line voltages (v_{AB}, v_{BC} , and v_{CA}) follow Eq. (10).

$$v_{AB} = (k_A - k_B) V_{dc} v_{BC} = (k_B - k_C) V_{dc}, v_{CA} = (k_C - k_A) V_{dc} \quad (10)$$

Eq. (11) presents the matrix form of Eq. (10).

$$V_{l-l(k_A, k_B, k_C)} = V_{dc} [(k_A - k_B) (k_B - k_C) (k_C - k_A)]^T \quad (11)$$

The reference line to line voltage vector can be shown by Eq. (12) in steady-state condition.

$$V_{REF} = V_{l-l} [\cos(\omega t) \cos(\omega t - 2\pi/3) \cos(\omega t + 2\pi/3)]^T \quad (12)$$

Now Eqs. (11) and (12) can be presented in d-q stationary plane by Eq. (13):

$$[V_{(l-l)d} V_{(l-l)q}]^T = V_{l-l}^* = \begin{bmatrix} 1 e^{j \frac{2\pi}{3}} & e^{j \frac{4\pi}{3}} \end{bmatrix} V_{l-l(k_{ab}, k_{bc}, k_{ca})} \quad (13)$$

Eq. (14) shows the reference voltage vector V_{REF}^* .

$$V_{REF}^* = [V_{(REF)d} V_{(REF)q}]^T = \begin{bmatrix} 1 e^{j \frac{2\pi}{3}} & e^{j \frac{4\pi}{3}} \end{bmatrix} V_{REF} \quad (14)$$

Using the definition of vector normalization, the length of the reference vector $|V_{REF}^*|$ is given by Eq. (15).

$$|V_{REF}^*| = \sqrt{V_{REF} \cdot V_{REF}} = V_{l-l} \sqrt{\frac{3}{2}} \quad (15)$$

Again, the length of the largest voltage space vector can be expressed by Eq. (16) according to the above definition.

$$|V_{l-l(k_{ab}, k_{bc}, k_{ca})}|_{max} = \sqrt{2} (q - 1) V_{dc} \quad (16)$$

The radius of the largest circle gives the maximum length of the reference vector. Hence, the maximum length of the reference vector is given by Eq. (17).

$$|V_{REF}|_{max} = |V_{l-l(k_{ab}, k_{bc}, k_{ca})}|_{max} \cos\left(\frac{\pi}{6}\right) \quad (17)$$

Figure 2 shows the switching vectors for a three-level inverter and the reference vector position of the equivalent phase switches are fixed by Eq. (14). The length of the largest space vector is found from Eq. (17), which is $|V_{l-l(k_{ab}, k_{bc}, k_{ca})}|_{max}$. The largest space vector also represents the limit of the linear modulation index (M_a). In Figure 2, the largest reference vector has been represented by the radius of a circle, which touches the outer hexagon. The length of the maximum length of the reference vector ($|V_{REF}|_{max}$) is equal to $2\sqrt{2} V_{dc} \cos(\frac{\pi}{6})$. The term modulation index is the ratio of reference voltage vector length ($|V_{REF}|$) to the length of largest space vector $|V_{l-l(k_{ab}, k_{bc}, k_{ca})}|_{max}$.

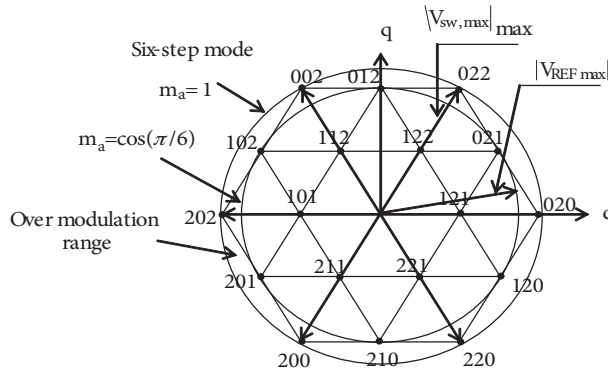


Figure 2. Switching-state vectors of three-level converter in the complex d-q plane and modulation range.

Hence the modulation index, $M_a = \frac{|V_{REF}|}{2\sqrt{2}V_{dc}}$.

The radius of the circle in Figure 2 indicates the largest reference voltage vector $|V_{REF_{max}}|$. It also represents the limit of operation. At the periphery of that circle the modulation index is $M_a = \cos(\frac{\pi}{6}) = 0.866$. $m_a = \cos(\pi/6) = 0.866$

The reference voltage vector V_{REF}^* , which has already been derived from Eq. (12), is sampled at low frequency rate (f_s). The sampling interval ($T_s = \frac{1}{f_s}$) is accomplished over three subcycles $t_1, t_2, and t_3$. The V_{REF}^* is an arbitrary complex quantity and it is approximated by the suitable space vectors, given in Eq. (13). A different switching sequence is generated during each subcycle ($t_1, t_2, and t_3$).

There is another approach to normalize the reference voltage vector and locate its sector [29,30]. The following steps summarize the procedure.

Step 1: The normalization of the reference space vector can be presented by Eq. (18). Hence the normalized voltage vector is

$$V_{REF}^* = (l - 1) \frac{V_{REF}}{V_{dc}} \tag{18}$$

Here $l =$ the number of voltage levels = 3, 7, 13,..

Step 2: The normalized voltage vector V_{REF}^* is transformed into V_n , where the imaginary part of V_{REF}^* is multiplied by $\frac{1}{\sqrt{3}}$, which flattens the normalized hexagon as shown in Figures 3a and 3b. The transformation of V_{REF}^* into V_n makes it possible to avoid online computation time of the switching states. Zone 1, zone 2, and zone 3 can be obtained from the complex d-q plane, which depends on the angle ϑ of V_n .

$\vartheta = (\frac{180}{\pi}) \tan^{-1}(\frac{V_{qn}}{V_{dn}})$, where V_{dn} and V_{qn} are the d-q components (real and imaginary parts) of the V_{REF}^* .

$$\vartheta = \begin{cases} 0^\circ \text{ to } 135^\circ; & \text{for zone 1} \\ 135^\circ \text{ to } 225^\circ; & \text{for zone 2} \\ 225^\circ \text{ to } 360^\circ; & \text{for zone 3} \end{cases}$$

Step 3: After calculating the three vectors ($V_1, V_2, and V_3$) of the triangle where the vector V_n is located, the nearest three switching states and their corresponding switching times ($t_1, t_2, and t_3$) are calculated; then calculation starts for the next step.

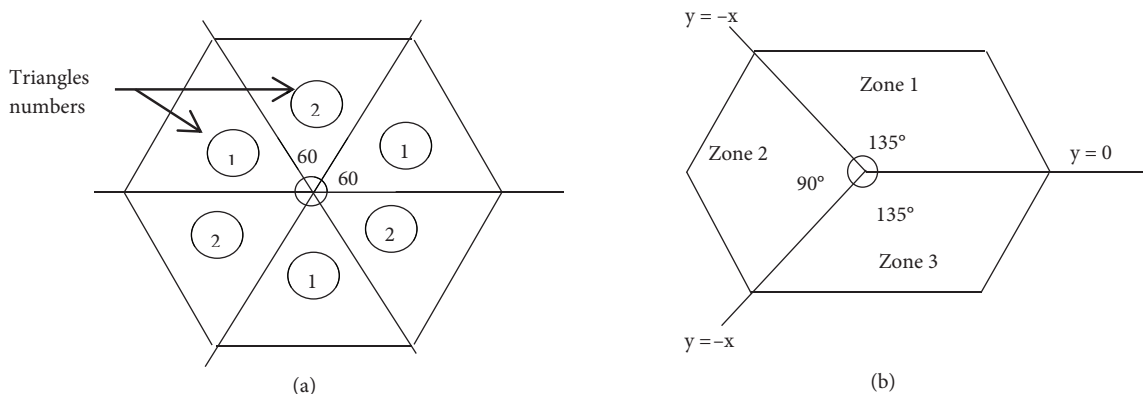


Figure 3. a. The normal hexagon, b. the flat hexagon.

Step 4: Replacing $k_{AB}, k_{BC},$ and k_{CA} in Eq. (10), the values of $k_A, k_B,$ and k_C can be evaluated.

$$\begin{bmatrix} 1 & -10 \\ 0 & 1 \\ -1 & 0 \end{bmatrix} \begin{bmatrix} k_A \\ k_B \\ k_C \end{bmatrix} = \frac{1}{V_{dc}} \begin{bmatrix} v_{AB} \\ v_{BC} \\ v_{CA} \end{bmatrix} = \begin{bmatrix} k_{AB} \\ k_{BC} \\ k_{CA} \end{bmatrix} \quad (19)$$

It should be noted that the third row can be derived from the summation of the first two rows of Eq. (19). It means that Eq. (13) gives two equations with the unknowns k_A, k_B and k_C . The solutions of these set of equations are not unique. To find proper solutions for these equations, one of the techniques is to assume a solution for one of the three unknowns. Assuming the solution for k_c is k , and substituting it into Eq. (13), another two variables can be expressed by Eq. (20).

$$k_C = k, k_A = k - k_{CA}, k_B = k + k_{BC} \quad (20)$$

To ensure that the results of the variables (k_A, k_B and k_C) are located inside their boundary limits [for seven levels the limit is 0, 1, 2, 3], the values of k can be limited by Eq. (21).

$$\begin{aligned} 0 \leq k_A \leq 3 &\implies 0 \leq -\frac{v_{CA}}{V_{dc}} + k \leq 3 \\ 0 \leq k_B \leq 3 &\implies 0 \leq -\frac{v_{BC}}{V_{dc}} + k \leq 3 \\ 0 \leq k_C \leq 3 &\implies 0 \leq -\frac{v_{BC}}{V_{dc}} + k \leq 3 \end{aligned} \quad (21)$$

To satisfy Eqs. (20) and (21), the condition for choosing a proper value of k is derived and it has been found as follows:

$$k = \max \left(0, \max \left(-\frac{v_{BC}}{V_{dc}}, \frac{v_{CA}}{V_{dc}} \right) \right)$$

4. Experimental results and discussion

To verify the proposed inverter topology, it has been simulated in MATLAB/Simulink software. The inverter concept has been implemented and a laboratory prototype has been built. Insulated-gate bipolar transistors

(IGBTs) with antiparallel diode (IRG4PH50UDPBF, 24 A, 1200 V) have been chosen as switching device. A digital signal processor (DSP, TMS320F2812) has been used to generate the switching gate signal for the inverter.

The performance of the space vector control technique has been clearly examined by using the simulation and hardware results. As described earlier, for every phase arm the input dc supply voltage of each core unit is different from that of the other unit. This phenomenon has been described by Eq. (1).

During hardware implementation, the input dc supply voltage of the core units has been adjusted for $V = 50$ volts and $2V = 100$ volts in each phase arm. The modulation index has been considered as $M_a = 0.8$, with switching frequency $f_c = 2000$ Hz. Figure 4 shows the two-stage configuration of the proposed inverter, which consists of six dc supplies, 12 switching devices (IGBTs), DSP, and three-phase Y-connected RL load ($R = 120 \Omega$ and $L = 90$ mH per phase). Figures 5(a) and 5(b) show the complete control block diagram and experimental setup of the proposed inverter for 7-level two-stage ($n = 2$) configuration, respectively. Experimental results have been obtained for a single stage ($n = 1$) and two stages ($n = 2$) per phase structure.

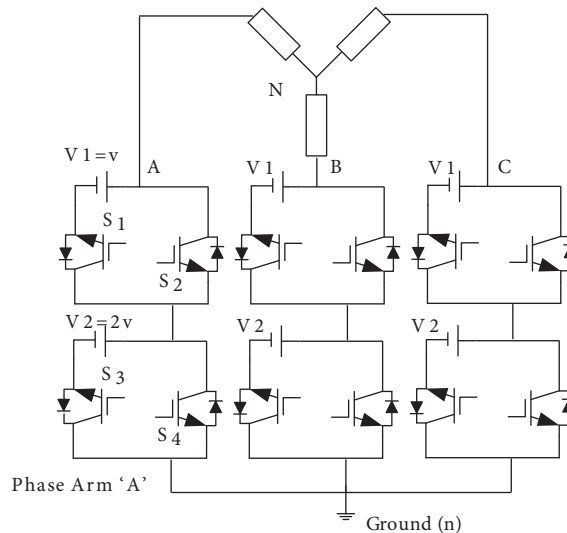


Figure 4. Proposed three-phase hybrid seven-level inverter, when the total number of stages is two ($n = 2$).

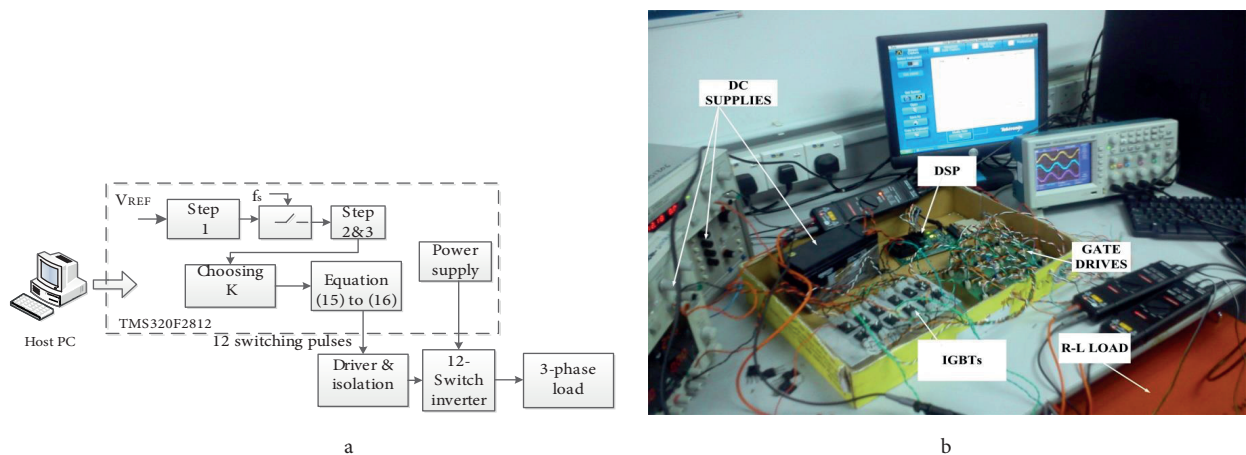


Figure 5. a. Complete control block diagram of the proposed inverter when number of stages is two ($n = 2$), 5b. prototype of the proposed multilevel inverter.

Figures 6a–6c and 7a–7c show several hardware results for single stage ($n = 1$) and double stage ($n = 2$), respectively. Similarly, it can be checked for n-number of stages. Figures 6a and 7a show the switching gate signals for single stage ($n = 1$) and double stage ($n = 2$), respectively. Figures 6b and 7b show the phase voltages (v_{An} , v_{Bn} , and v_{Cn}) from the phase arm (A, B, C) top to the ground for single and double stage, respectively. During the single stage the node voltages contain two levels (0 and V). In the case of two-stage configuration the phase voltages have four voltage levels (0, V, 2V, and 3V). The three-phase line to line voltages are formed by using these multilevel phase voltages, who have been expressed by Eq. (6). Table 2 shows the switching states of the seven-level two-stage inverter for the phase arm-A.

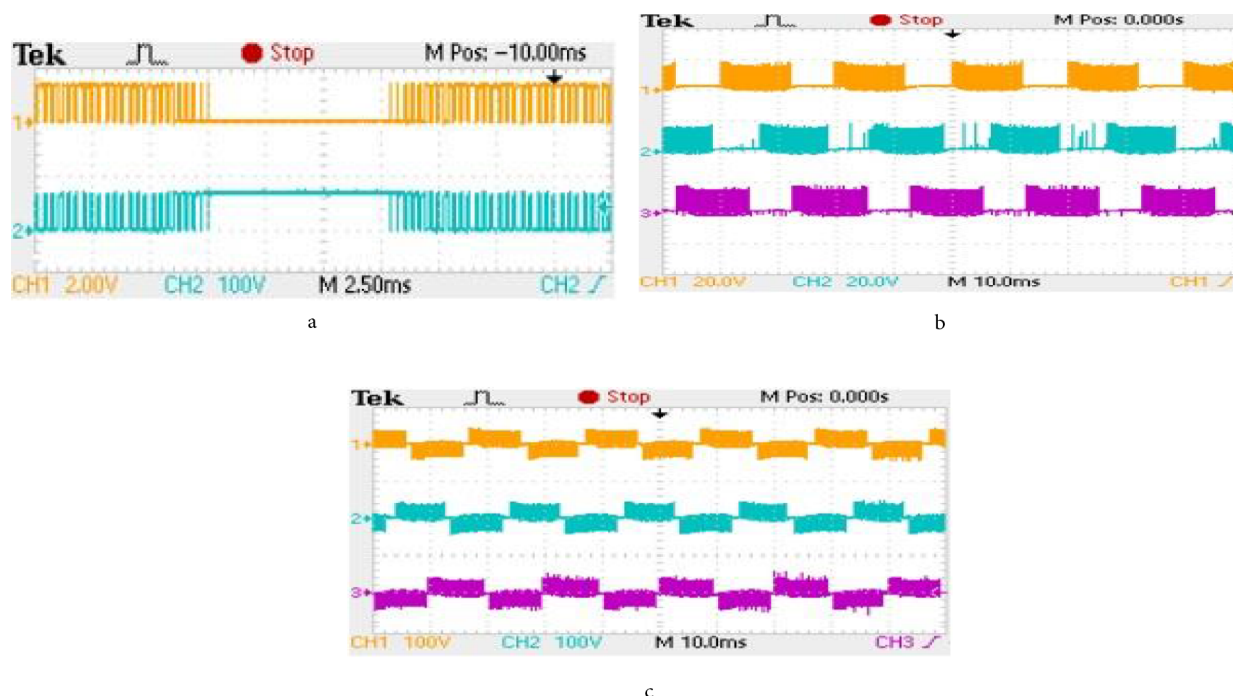


Figure 6. a. Switching signal for S1 and S2, respectively, b. phase voltages (V_{An}, V_{Bn}, V_{Cn}), 6c. three-phase line voltages (V_{AB}, V_{BC}, V_{CA}).

Table 2. Switching states of phase arm V_{An} .

Node voltage	Switches of arm ‘A’			
v_{An}	S_1	S_2	S_3	S_4
$0V_{dc}$	0	1	0	1
$1V_{dc}$	1	0	0	1
$2V_{dc}$	0	1	1	0
$3V_{dc}$	1	0	1	0

This is also one superiority of the proposed three-phase configuration, i.e. there is no necessity to use any extra switches for creating a negative half-cycle of the AC voltage. Figures 6c and 7c show the three-phase AC line voltages (V_{AB}, V_{BC}, V_{CA}) of the single-stage ($n = 1$) and double-stage ($n = 2$) configuration, respectively. According to Figure 1b and Eq. (5), the number of voltage levels in the line voltage for the n-stage inverter can be written by the following equation:

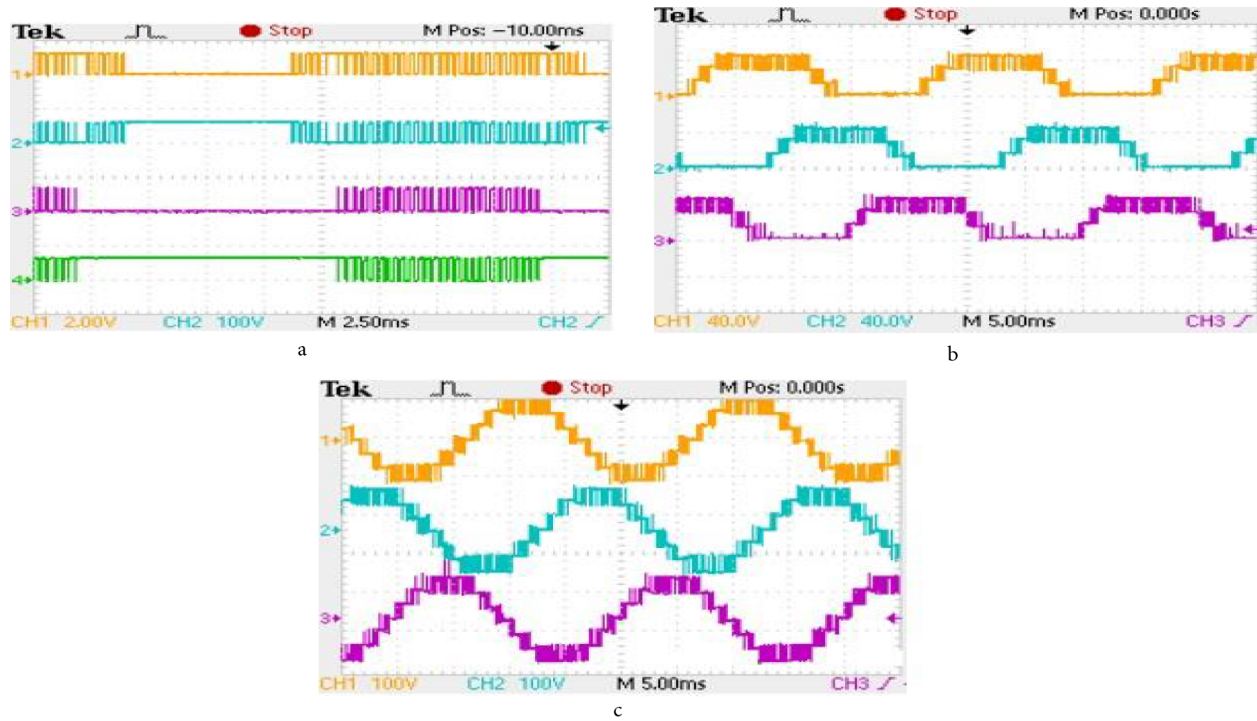


Figure 7. a. Switching signal for S1, S2, S3, and S4, respectively, b. phase voltages (V_{An}, V_{Bn}, V_{Cn}), respectively, c. three-phase line voltages (V_{AB}, V_{BC}, V_{CA}), respectively.

$$l = (2 \sum_{i=1}^n i) + 1, \text{ where } n = \text{number of stages} = 1, 2, 3, \dots$$

This includes positive, zero (0), and negative voltage levels. Hence, the number of levels in the line voltages of the single stage ($n = 1$) and double stage ($n = 2$) inverter should have three and seven levels, respectively. The amplitudes of these three and seven levels can be written as $V, 0, -V$ and $3V, 2V, V, 0, -V, -2V, -3V$, respectively.

In the method proposed in [23], six basic units (half bridge cell) and one full bridge inverter have been used to generate thirteen voltage levels per phase (shown in experimental results). Here each unit contains two switches and one dc input source. Hence, for thirteen voltage levels, it needs a total of 18 switches and six isolated input dc supplies. Therefore, for three-phase configuration, the total number of required switches should be $18 \times 3 = 54$. On the other hand, it is possible to generate 13-level three-phase line voltage using the proposed three-stage ($n = 3$) configuration. In the case of 13 levels, each of the phase arms consist of six switches and three input dc supplies. Therefore, 18 switches and nine input dc supplies are required for generating three-phase line voltages.

The proposed two-stage ($n = 2$) inverter topology has been tested under different modulation indexes. According to Eq. (17), the reference of the space vector is calculated by the modulation index and the switching region. For two-stage configuration, when the modulation index is below 0.5 the low voltage stage works only and shows three-level line voltages. When the modulation index is 0.7, the line voltage shows five levels. When the modulation index is 0.8, the inverter line voltage shows seven-level output. Figure 8 shows the three-, five-, and seven-level line voltages for modulation index 0.3, 0.7, and 0.8, respectively.

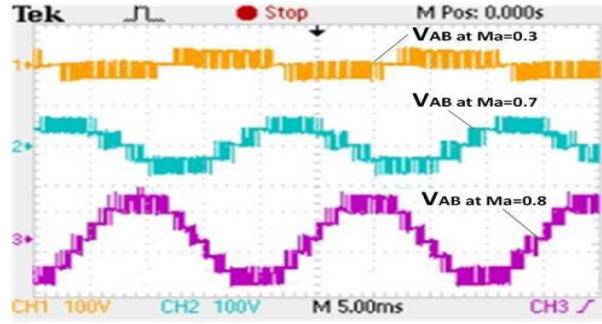


Figure 8. Line voltages at different modulation index.

The THD of the line current can be obtained by the following equation:

$$THD = \frac{\sqrt{\sum_{n=3,5,7,\dots}^{\infty} I_n^2}}{I_1},$$

where I_1 and n are the fundamental component and harmonic order, respectively. Figure 9a shows the variation in line current THD with the modulation index for the line current in the case of two-stage ($n = 2$) configuration. This figure indicates that the THD is inversely related to the modulation index (M_a). It should be clearly noted that the lower THD content in the output line current is available at higher modulation index. A “YOKOGAWAWT 1800” precision power analyzer has been used to capture the frequency spectrum of the line current. Figures 9b and 9c show the line current and line current spectra for two-stage configuration ($n = 2$) during modulation index = 0.8. A FLUKE 435 series power analyzer has been used to capture the frequency spectrum of the line voltage. Figures 9d–9f show line voltage spectra during modulation index = 0.3, 0.7, and 0.8.

Figure 10 shows the THD of the line current during modulation index $M_a = 0.8$ for different levels in the output voltages. It shows the relation between the number of voltage levels and the THD of the line current. The lower THD content in the output line current is available at higher number levels in the line voltage. Hence, the number of inverter stages should be increased to get better output.

There is another way to obtain a higher number of output voltage steps in this proposed topology. To do so, the inverter stages and the input dc supplies should have a relation in binary form (power of two) [31]. If ‘ n ’ is the number of stages, then each core unit per phase arm input voltage should be ‘ $2^n \times V$ ’, where $n = 1, 2, 3, 4, \dots$. The number of levels in the line voltages can be written as $(2^{n+1} - 1)$.

According to Figure 1b for three-stage configuration ($n = 3$), there should be three core units per phase arm. If the input dc supply voltage of the first core unit is $V = 200$ volts, then the second and third unit input supply voltages should be 600 volts and 800 volts, respectively. It means two and four 200 v dc supplies will be connected in series for the second and third units, respectively. Table 3 compares the required components and the output voltage levels between two input dc supply voltage determining methods.

According to Table 3, it is clear that the binary related technique generates higher voltage with a larger number of levels in the output voltage. However, extra dc supplies are required in the third unit and the switching devices are subjected to high voltage. Therefore, it is mandatory for this method to use different types of switches for high voltage blockage. Since the voltage standing on the switches is lower, the applied method is used to generate the maximum number of voltage levels using similar numbers of switches. Therefore, better modularity is achieved compared to other asymmetrical cascaded topologies.

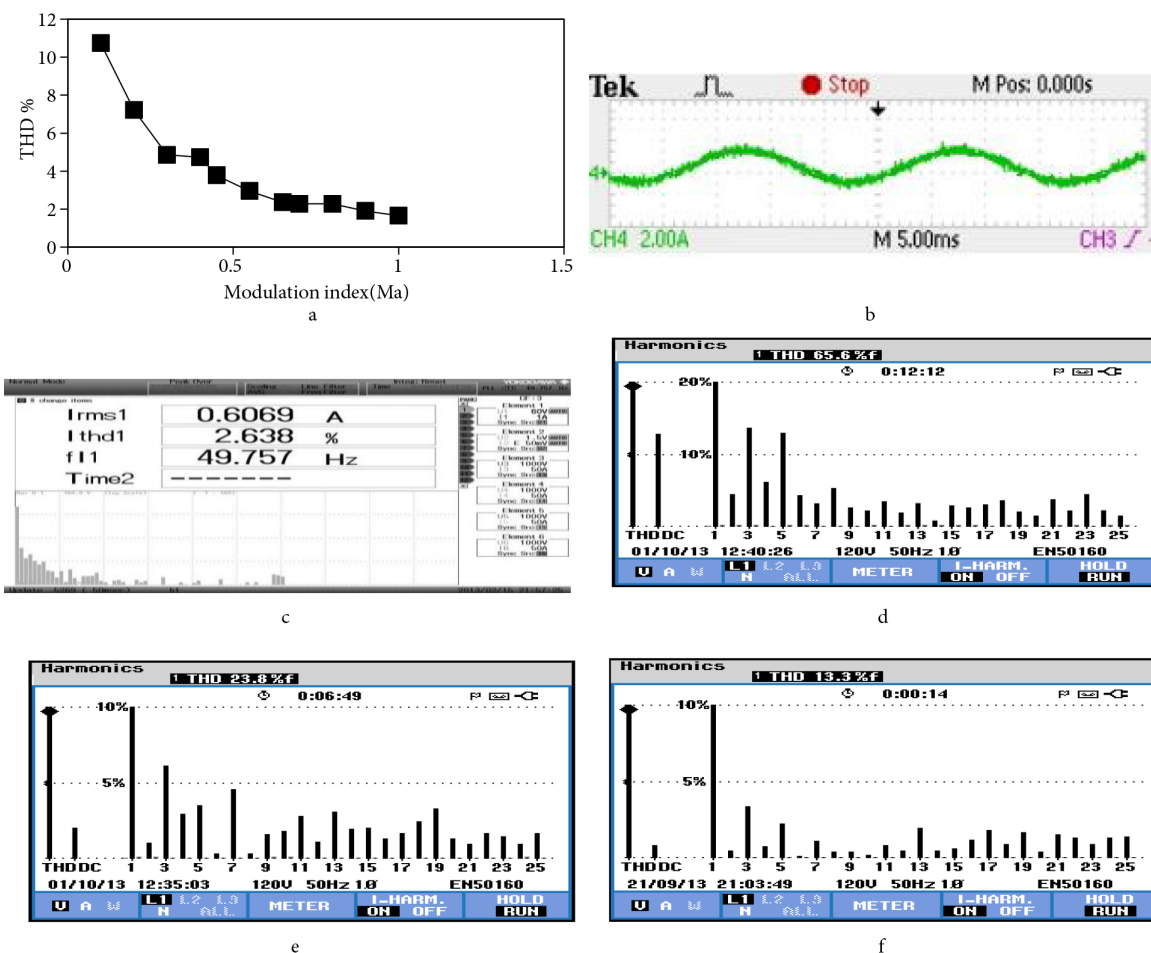


Figure 9. a. Modulation index (M_a) against line current THD, b. line current during two-stage configuration ($n = 2$), c. harmonic spectra of the above line current using “YOKOGAWA WT 1800” precision power analyzer, d. harmonic spectra of the line voltage at $M_a = 0.3$, e. harmonic spectra of the line voltage at $M_a = 0.7$, f. harmonic spectra of the line voltage at $M_a = 0.8$.

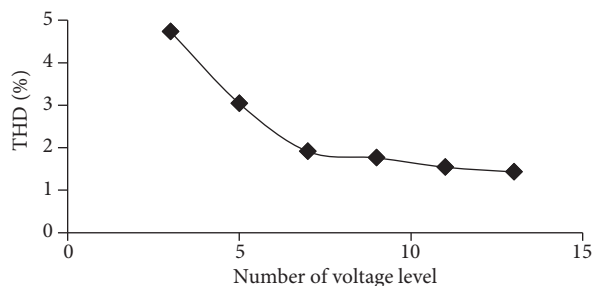


Figure 10. Relation between the number of voltage levels and the THD of the line current.

Another vital issue in inverters is the ratings of the semiconductor switches, as the current and voltage ratings of switches are responsible for the cost and efficiency. Since all the inverter cells are connected in series, the maximum current rating of any switch equals the load peak current. On the other hand, blocking voltage or the voltage stress of any switch equals the input dc voltage of its cell circuit. Thus the maximum blocking

voltage or the voltage stress in this proposed topology should be on the first cell switches' ($n = 1$) voltage and is equal to nV_{dc} .

Table 3. Comparison between the two methods followed to determine the values of dc supplies for the introduced inverter.

	Binary [31]	Proposed method
Number of switches	18	18
Number of utilized dc sources (200 V units)	4	3
Number of levels	15	13
Voltage of the third stage units	800 volts	600 volts
Similarity of the switches	No	yes

5. Comparison of the proposed topology with other topologies

Table 4 presents a clear comparison between the conventional cascaded MLI and the proposed inverter topology for seven-level output voltage. The diode clamped is very attractive for high-voltage topology. The deviating voltage at the neutral point remains a remarkable feature of this topology. Therefore, voltage balancing is one of the difficulties in this topology. The flying capacitor (FC) topology uses capacitors for voltage balancing. For some specific applications these topologies are very advantageous. Less operation is performed by the transformer and redundant phase arm states, which makes the semiconductor switches share equal voltage stress. However, for the high voltage level the model becomes bulky, since it needs an excessive number of storage capacitors. Table 5 presents a basic comparison between the proposed inverter and the conventional well-known MLI topologies, NPC and FC, based on the same number of switches. Table 6 represents a comparison among the conventional topologies according to the number of levels (l) in the line voltage and components. According to Table 6, the number of components of the proposed topology is lower than that of other topologies.

Table 4. Comparison of the proposed three-phase seven-level inverter with the well-known seven-level inverters.

	Diode clamp	Flying capacitor	New MLI topology [32]	Half-bridge modules topology [33]	Proposed topology
Switching devices and gate drivers	36	36	30	18	12
Main diodes	36	36	30	18	12
Clamping diodes	90	0	0	0	0
Dc buses/ isolated supply	6	3	3	7	6
Balancing capacitor	0	9	0	0	0

Table 5. Comparison of the implemented 12-switch inverter with some other well-known 12 switch inverters.

	Diode clamp	Flying capacitor	H-bridge inverter	Proposed topology
Number of levels	3	3	3	7
Level/switch ratio (RLS)	0.25	0.25	0.25	0.58
Number of dc bus/ isolated supply	1	1	3	6
No. of diodes	18	12	12	12

Table 6. Number of components for three-phase inverters.

Inverter type	Diode clamped	Flying capacitor	Cascaded H-bridge	Proposed topology
Main switches	$6(l-1)$	$6(l-1)$	$6(l-1)$	$3\{\sqrt{(4l-3)-1}\}$
Main diodes	$6(l-1)$	$6(l-1)$	$6(l-1)$	$3\{\sqrt{(4l-3)-1}\}$
Clamping diodes	$3(l-1)(l-2)$	0	0	0
Dc bus capacitors/ isolated supplies	$(l-1)$	$(l-1)$	$\frac{3(l-1)}{2}$	$\frac{3}{2}\{\sqrt{(4l-3)-1}\}$
Flying capacitors	0	$\frac{3(l-1)(l-2)}{2}$	0	0
Total numbers	$(l-1) \times (3l+7)$	$\frac{3(l-1)(3l+20)}{2}$	$\frac{27(l-1)}{2}$	$\frac{15}{2}\{\sqrt{(4l-3)-1}\}$

6. Semiconductor losses

Generally, semiconductor losses in a MLI can be divided into two types: the conduction loss and the switching loss. The voltage drop across the active semiconductor device due to the current conduction is responsible for the conduction loss. The switching loss is closely related to the switching frequency. To analyze the semiconductor losses, we have tested a 250 KW MATLAB/Simulink model of the proposed seven-level two-stage ($n = 2$) structure. We have selected IGBT (5SNE0800M170100) as a switching device, since it conducts negligibly small leakage current while in turn off state. The maximum voltage and current ratings are 1700 V and 800 A, respectively. The DC supplies are selected as $V1 = V = 800$ volts and $V2 = 2V = 1600$ per arm. The conduction loss of an IGBT mainly depends on the forward voltage drop $V_{on,IGBT}$ and the instantaneous current $I(t)$.

$$P_{cond,IGBT} = \frac{1}{T} \int_0^T V_{on,IGBT} I(t) dt$$

Similarly, the conduction loss of a diode can be expressed as

$$P_{cond-d}(t) = i_F * (V_{FO} + R_F \cdot I_F(t)),$$

where V_{FO} is the forward voltage drop during forward current (I_F) passes over the diode. R_F is the diode resistance, which is available is the on state resistance slope of the datasheet.

The switching loss occurs at each switching action. Two types of switching losses are available during switching actions: turn on energy loss (E_{on}) and turn off energy loss (E_{off}). The values of E_{on} and E_{off} depend on the collector current, which is available in the product data sheet. The average switching power losses (turn on and off) in an IGBT and freewheeling diode can be written as

$$P_{on}^- = \frac{1}{T} \cdot \int_0^T E_{on}(t) dt$$

$$P_{off}^- = \frac{1}{T} \cdot \int_0^T E_{off}(t) dt$$

$$P_{off,D}^- = \frac{1}{T} \cdot \int_0^T E_{off,D}(t) dt$$

Figure 11 shows the semiconductor power loss distribution during 2 KHz switching frequency for phase A of the proposed two-stage ($n = 2$) MLI configuration. D_1, D_2, D_3, D_4 are the built-in freewheeling diodes of the switches S_1, S_2, S_3, S_4 , respectively.

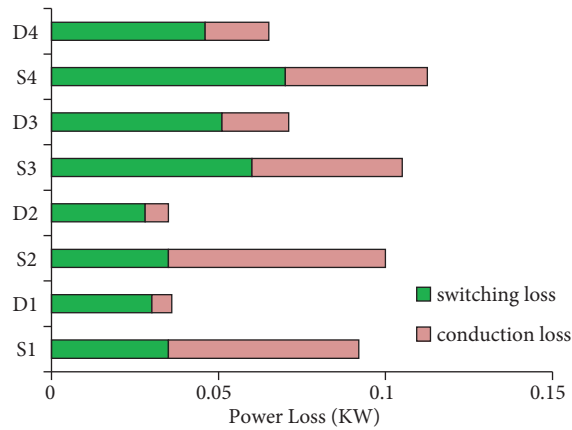


Figure 11. Loss distribution among the semiconductor devices in phase (A).

7. Conclusion

An efficient three-phase cascaded multilevel inverter topology has been proposed with successful experimental verification. The configuration needs reduced number of switches, gate drive circuits, and other circuit arrangements. It needs reduced installation area and cost. The voltage standing on the switches has been minimized by optimizing the voltage levels and applying special switching control using SVM.

This topology has been extended for ‘ n ’ number of levels. In order to verify the performance of the proposed MLI, three-level single-stage ($n = 1$) and seven-level two-stage ($n = 2$) configuration have been implemented in the laboratory. The desired hardware results ensure a highly efficient inverter for three-phase Y-connected applications. This work will be extended for grid-connected supply in future.

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