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FGMOS-based differential difference CCCII and its applications

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Abstract: A novel floating gate MOS (FGMOS) transistor-based differential difference controlled current conveyor (DDCCC) is proposed in this paper. Major advantages of the FGMOS-based DDCCC are low power dissipation and simplicity. The proposed circuit is designed using only 14 MOS transistors. The total power dissipation of the proposed circuit is equal to 7.38 μW. The other advantage of this circuit is that intrinsic resistance seen at port X of the DDCCC can easily be tuned by a biasing current. The tuning range of the intrinsic resistance is rather wide. Additionally, a current controlled universal filter and tunable positive and negative active resistors are presented as applications of the proposed circuit. The DDCCC and its applications are simulated using SPICE in 0.18 μm CMOS technology.

Key words: Current mode circuit, current conveyor, FGMOS transistor, low power

1. Introduction

Current mode circuits for electronic circuit design have advantages such as high linearity, good slew rate, wide bandwidth, low power dissipation, and simpler circuit structure compared with voltage mode circuits [1–4]. The second-generation current conveyor (CCII) used commonly in current mode circuit design was proposed by Sedra and Smith in 1970 [5]. The current controlled current conveyor (CCCII) proposed by Fabre in 1995 is a type of CCII [6]. The CCCII has a parasitic resistor whose value can be adjusted by biasing current at the input port X. Differential voltage signals are frequently employed in analog electronic circuits. However, the CCII and CCCII structures are not suitable considering some differential inputs. Differential voltage current conveyor (DVCC) and differential difference current conveyor (DDCC) structures are convenient to use for differential signals and these structures were reported in [7,8]. These structures suffer from incapability of electronic adjustability. Therefore, a new circuit, called a current controlled differential difference current conveyor, was introduced in the literature [9]. This circuit contains too many components and has tunable intrinsic resistance. In terms of the electronic circuit design, intrinsic resistances are generally considered as a disadvantage, but the intrinsic resistance at the input port of the DDCCC can be used instead of passive resistors to decrease the number of passive components. Adjustability of the intrinsic resistance by the biasing current also provides some advantages [10].

The FGMOS transistor, a kind of MOSFET transistor, has a floating gate that is completely isolated within the oxide. This structure also has two or more gate terminals, which are coupled capacitively to the

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floating gate. FGMOS transistors have advantages such as functional structure and wider dynamic range. These structures can facilitate the design of circuits working with low voltage and low power. Considering these advantages, FGMOS transistors have been commonly utilized to design analog circuit applications such as current mirror, analog multiplier, current conveyors, adjustable and highly linear resistors, filters, digital-to-analog converters, and operational transconductance amplifiers [11–21].

In this study, a new DDCCC structure that is designed by employing FGMOS transistors is proposed. The novelties of the proposed DDCCC are having a very simple structure using FGMOS transistors and tunability. The proposed circuit also consumes very low power. It can be tuned to a wide range of intrinsic resistance values at the input terminal of the DDCCC. As applications of the proposed DDCCC, a current controlled universal filter and tunable positive and negative active resistor structures have been demonstrated. In order to confirm the theoretical approaches, the proposed DDCCC, the universal filter, and the active resistor structures have been simulated by SPICE.

2. FGMOS transistor

The symbol and the equivalent circuit of an n-type FGMOS transistor that has two or more gate terminals are shown in Figures 1a and 1b.

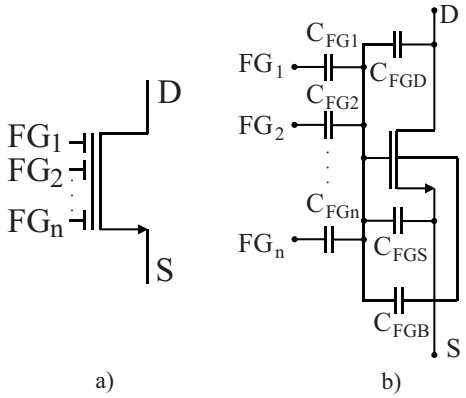

Figure 1. The n-type FGMOS transistor: a) symbol, b) equivalent circuit.

$FG_1, FG_2, \ldots FG_n$ are the input gate terminals. The input gates are coupled to the floating gate capacitively and the input capacitances are C_{FG1}, C_{FG2}, $\ldots C_{FGn}$. The floating gate is also coupled capacitively to the drain, source, bulk, and gates. These parasitic capacitances are C_{FGD}, C_{FGS}, and C_{FGB} as depicted in Figure 1b. Voltages of the input gates, drain, source, and bulk terminals affect the effective floating gate voltage in proportion to the coupling capacitances. The total capacitance C_T between the floating gate and the other terminals can be written as:

$$C_T = C_{FGD} + C_{FGS} + C_{FGB} + \sum C_{FGi}. \tag{1}$$

If the relation belonging to the total capacitances is written as $C_{FGD} + C_{FGS} + C_{FGB} << \sum C_{FGi}$, then C_T is approximately equal to $\sum C_{FGi}$. Here V_{FG} is the effective floating gate voltage and it can be defined as:

$$V_{FG} = \sum_{i=1}^{n} \frac{C_{FGi}}{C_T} \cdot V_{FGi} + \frac{Q_{FG}}{C_T}, \tag{2}$$

where Q_{FG} is the residual charge trapped at the floating gate during the fabrication process. This charge can be eliminated as explained in [21].

The drain current I_{DS} for the FGMOS transistor in the subthreshold region is determined as:

$$I_{DS} = I_Z \cdot S \cdot e^{\frac{\kappa \cdot V_{FGB}}{U_t}} \left(e^{-\frac{V_{SB}}{U_t}} - e^{-\frac{V_{DB}}{U_t}} \right), \tag{3}$$

where I_Z is the zero-bias current. V_{FGB}, V_{SB}, and V_{DB} are voltages of the floating gate-bulk, source-bulk, and drain-bulk, respectively. S and κ denote the aspect ratio of the channel and the electrostatic coupling coefficient between the gate and the channel. Additionally, U_t can be described as the thermal voltage [21,22].

3. Proposed DDCCC circuit

The block diagram of the DDCCC is seen in Figure 2.

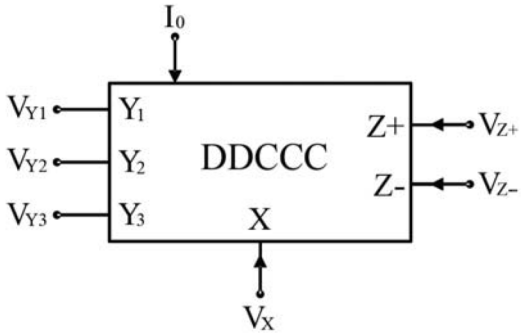

Figure 2. Symbol of the DDCCC.

For an ideal DDCCC, input impedances at Y terminals are equal and infinite. The input impedance of the X terminal is an intrinsic resistance and its value can be controlled by the biasing current of the DDCCC. The output impedance of the Z terminal is infinite. The DDCCC can be defined by the following matrix equation.

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_Z \end{bmatrix} = \begin{bmatrix} R_X & 1 & -1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \end{bmatrix} \cdot \begin{bmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_Z \end{bmatrix} \tag{4}$$

The circuit diagram of the proposed FGMOS transistor-based DDCCC is shown in Figure 3. As shown in Figure 3, the designed DDCCC with +Z output terminal contains 14 transistors. If the circuit is designed by adding one more output terminal (–Z terminal), it requires 12 more transistors. Therefore, a DDCCC having both +Z and –Z output terminals can be designed using 26 transistors.

V_{FGS7} and V_{FGS8} are the voltage differences between the effective floating gate and source terminal for the M_7 and M_8 transistors, respectively.

V_{FG7} and V_{FG8} are the effective floating gate voltages of the M_7 and M_8 transistors. If a loop equation is written from the floating gate of M_8 to the floating gate of the M_7 transistor, Eq. (5) is obtained as:

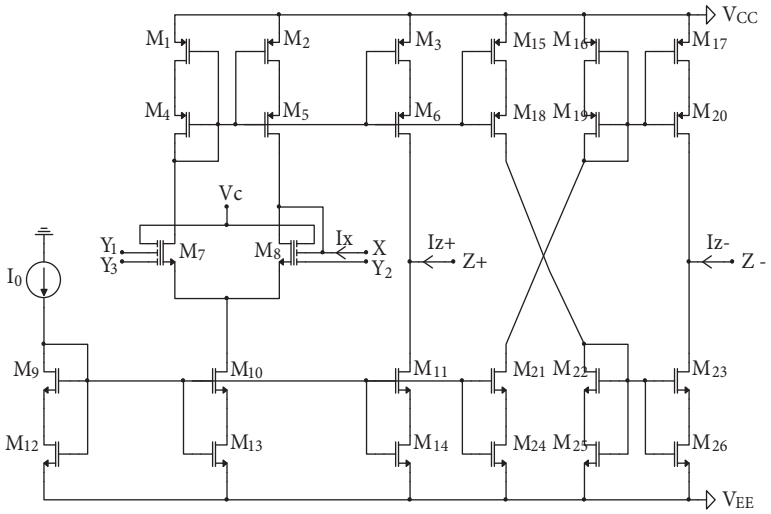

Figure 3. Proposed FGMOS-based DDCCC circuit.

$$V_{FG8} - V_{FGS8} + V_{FGS7} - V_{FG7} = 0. \tag{5}$$

The effective floating gate voltages shown in Eq. (5) can be expressed as:

$$V_{FG7} = \frac{C_{FG}}{C_T}\left(V_{Y1} + V_{Y3} + V_C\right), \tag{6a}$$

$$V_{FG8} = \frac{C_{FG}}{C_T}\left(V_X + V_{Y2} + V_C\right), \tag{6b}$$

where V_C is utilized to increase the input voltage swing of FGMOS transistors. Assuming the perfect matching of the transistors, Eq. (7) is obtained as follows:

$$V_{FGS8} - V_{FGS7} = \frac{C_{FG}}{C_T}\left(V_X - V_{Y1} + V_{Y2} - V_{Y3}\right), \tag{7}$$

where all input capacitances are equal to C_{FG}. If the M_7 and M_8 transistors are assumed to be operating in the subthreshold region, the current I_X at the X terminal, which is equal to the difference between I_{D8} and I_{D7}, can be written as:

$$I_X = I_0 \cdot \tanh\left(\frac{\kappa \cdot V_{DM}}{2 \cdot U_t}\right), \tag{8}$$

where I_0 is the biasing current and V_{DM} is the difference voltage between V_{FG8} and V_{FG7} [22].

From Eq. (8), if the expression belonging to the voltages is assumed as $\kappa \cdot V_{DM} << 2 \cdot U_t$, current I_X can be found as:

$$I_X = I_0 \cdot \frac{\kappa \cdot V_{DM}}{2 \cdot U_t}, \tag{9}$$

where V_{DM} is equal to (1/3) ($V_X - V_{Y1} + V_{Y2} - V_{Y3}$). If it is assumed that V_{Y1}, V_{Y2}, and V_{Y3} are grounded, I_X is found as:

$$I_X = I_0 \cdot \frac{1}{6} \cdot \frac{\kappa \cdot V_X}{U_t}. \tag{10}$$

From Eq. (10), the intrinsic resistance R_X providing the controllability of the DDCCC is written as:

$$R_X = \frac{V_X}{I_X} = \frac{6 \cdot U_t}{I_0 \cdot \kappa}. \tag{11}$$

As shown in Figure 3, two separate current mirrors are composed with M_1–M_6 and M_9–M_{14}. Considering the general characteristics of the DDCCC, the current at the X terminal must be equal to the current at the Z terminal. Therefore, the channel width of M_3 should be chosen as twice as much channel width of M_1 and M_2. In the same manner, this situation is valid for M_4, M_5, and M_6 transistors.

4. Simulation results

The circuit shown in Figure 3 is simulated by using SPICE for 0.18 μm TSMC CMOS parameters. The model presented in [21] is used to simulate FGMOS transistors. Input capacitances belonging to FGMOS transistors are taken as 50 fF. The supply voltage is equal to $\pm$0.6 V and V_c is chosen as –0.6 V to increase the input voltage swing of the FGMOS transistors. Transistor dimensions used in the proposed DDCCC are given in Table 1.

Table 1. Transistor dimensions of the proposed DDCCC.

Transistor	W (μm)	L (μm)
M_1, M_2, M_{16}, M_{17}	2	2
M_3, M_{15}	4	2
M_4, M_5, M_{19}, M_{20}	2	0.5
M_6, M_{18}	4	0.5
M_7, M_8	3	1
M_9–M_{11}, M_{21}–M_{23}	5	0.5
M_{12}–M_{14}, M_{24}–M_{26}	5	2

Figure 4 shows the current transfer characteristics from the X terminal to the Z terminal for $I_0 = 5$ μA. As shown in the graph, the output current at the Z terminal is correctly copied from the X terminal.

Figure 5 indicates the DC characteristics between the X terminal and the Y terminals of the DDCCC. Voltage transfer error of the Y terminals to the X terminal is about 10 mV for $\pm$0.4 V input voltage.

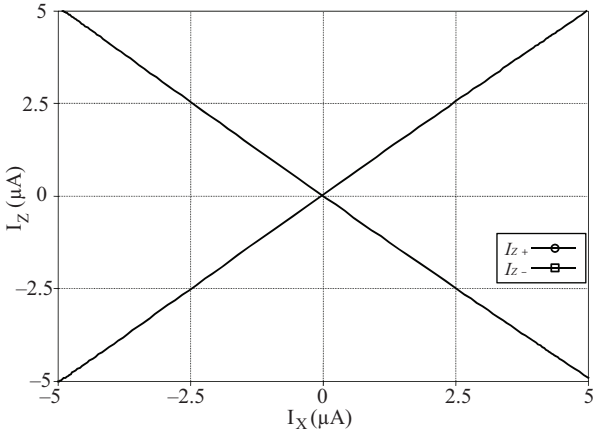

Figure 4. DC curves I_Z vs. I_X.

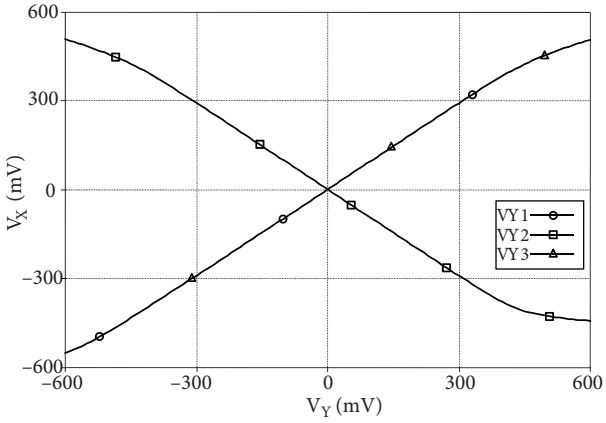

Figure 5. DC characteristics V_X vs. V_Y.

Figure 6 displays the intrinsic resistance R_X at the input X terminal versus I_0. As shown in Figure 6, the value of the intrinsic resistance can be controlled between 17 MΩ and 30 KΩ while I_0 varies from 10 nA to 10 μA. The output impedance at the Z terminal is 5.88 MΩ for $I_0 = 1$ μA.

Figure 7 depicts the voltage and current transfer gains. It is seen from Figure 7 that the frequency responses of the voltage and current follower are equal to 48 MHz and 23 MHz, respectively.

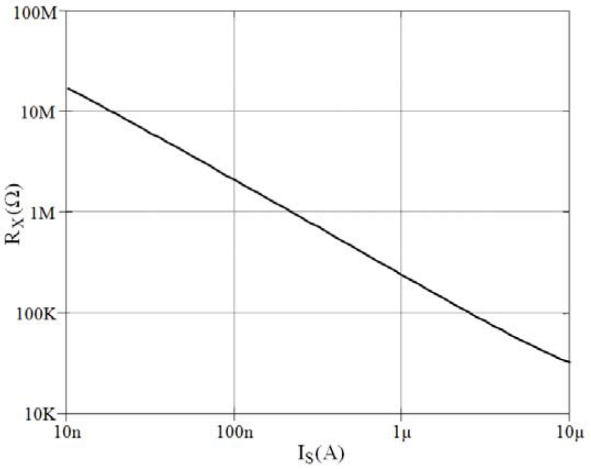

Figure 6. Variation of the intrinsic resistance R_X with the biasing current I_0.

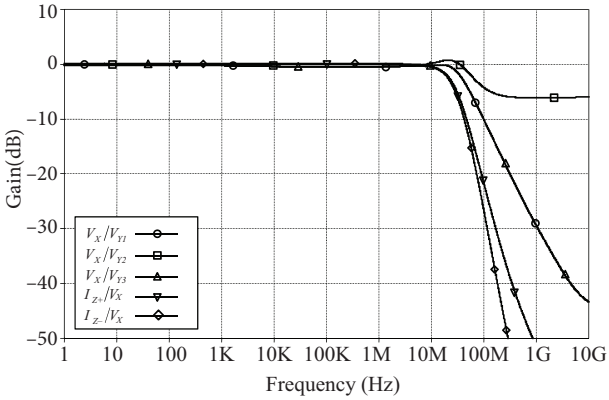

Figure 7. The frequency responses of the voltage gains (V_X/V_Y) and the current gains (I_Z/I_X).

Figure 8 shows that the total harmonic distortion (THD) is 1.27% when V_{Y1}–V_{Y2} is equal to 700 mV_{P-P}. The result shows that the THD remains below 1% for difference input signals with amplitude lower than 600 mV peak to peak, which confirms the practical utility of the proposed circuit. This result is reasonable. The power dissipation of the proposed DDCCC is 7.38 μW for $I_0 = 10$ μA.

As seen in Table 2, the proposed DDCCC is compared with some presented current conveyors in the literature.

Table 2. The performance parameters of the current conveyors.

	Proposed circuit	[9]	[18]	[23]	[24]	[25]	[26]
Supply voltage (V)	±0.6	±1.25	±0.5	±1	+1	±0.75	±1.5
Power consumption (μW)	7.38	1350	10	865	21	1340	1740
Electronically tunability	Yes	Yes	No	Yes	No	No	No
Input voltage range (V)	±0.4	±0.3	±0.5	±0.4	0.7	NA	±0.9
3 dB BW I_Z/I_X (MHz)	23	1000	10.2	48.75	11	159	120
3 dB BW V_X/V_Y (MHz)	48	100	2.9	NA	11	200	85
DC voltage error (mV)	10	4	NA	NA	NA	NA	NA
DC current error (μA)	0.080	NA	NA	NA	NA	NA	NA
R_X (Ω)	30 K to 17 M	1–12 K	70	NA	0.4	1.84	9
R_Y (Ω)	55 G	NA	0.993 T	NA	NA	300 G	NA
R_Z (Ω)	5.88 M	NA.	55.7 M	NA	0.4 M	1.5 M	NA
Number of transistors	14	23	21	19	24	NA	24
Technology (μm)	0.18	0.25	0.18	0.35	0.18	0.5	0.25

It is clear that the proposed current conveyor circuit has a good performance. As seen in Table 2, the proposed structure consumes lower power than the other circuits and the supply voltage is desirable. The proposed circuit employs only 14 transistors and it can be electronically tuned by the intrinsic resistance at the input terminal. The tuning range of this resistance is also wider than that of the other circuits. Additionally, the bandwidth of circuits operating at low power is narrower than the others. It is obviously seen that the proposed circuit has wider bandwidth than those in [18] and [24]. DC voltage transfer error is related to dynamic input range and it is observed that the error is higher than in [9]. The dynamic input ranges of the proposed circuit and that of [9] are ± 0.4 V and ± 0.3 V as clearly shown in Figure 9 for ± 0.6 V and ± 1.25 V supply voltages, respectively. When viewed from this aspect, the voltage transfer error value of the proposed circuit can be assessed as reasonable. Voltage transfer characteristics of these circuits are illustrated in Figure 9.

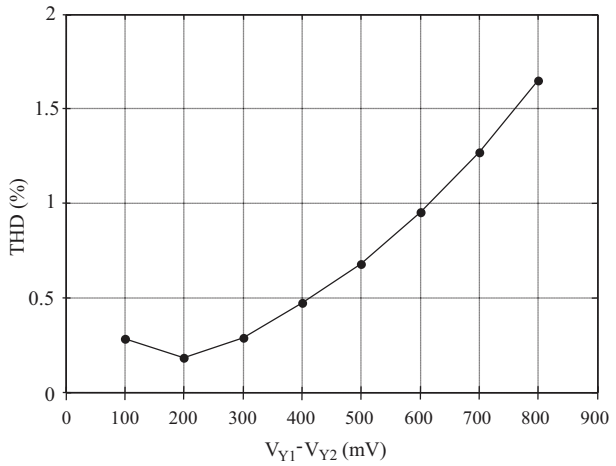

Figure 8. Total harmonic distortion for V_X at 1 MHz.

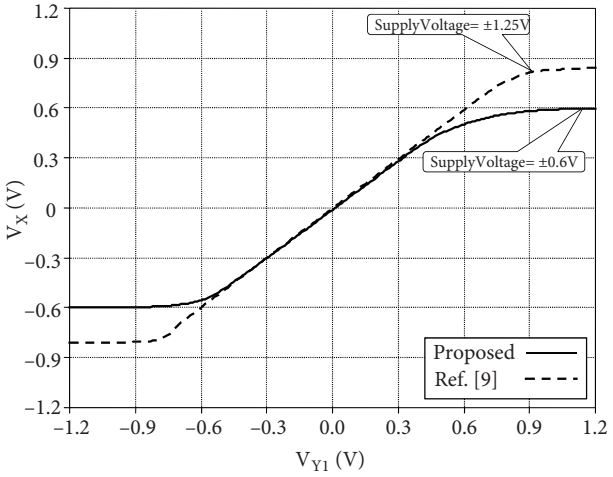

Figure 9. The comparison of the voltage transfer characteristics.

5. Applications

5.1. DDCCC-based current controlled universal filter application

The controllable universal filter structure shown in Figure 10 is obtained by modifying the filter in [27]. This structure has three inputs and one output to provide realization of the low pass (LP), high pass (HP), band pass (BP), and band reject (BR) filters.

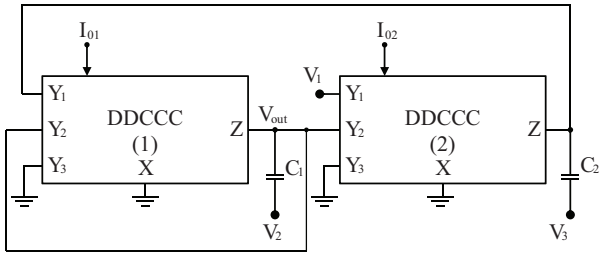

Figure 10. DDCCC-based universal filter.

The universal filter seen in Figure 10 is composed of two DDCCCs and two capacitors. The output functions of the filter can be written as:

$$V_{out} = \frac{s^2 C_1 C_2 V_2 + s\frac{C_2}{R_X} V_3 + \frac{1}{R_X^2} V_1}{s^2 C_1 C_2 + s\frac{C_2}{R_X} + \frac{1}{R_X^2}}, \tag{12}$$

where R_X is the intrinsic resistance at the X terminals of the DDCCCs and all biasing currents are equal to I_0. The cut-off frequency and quality factor of this structure can be given as follows:

$$w_0 = \frac{1}{R_X \sqrt{C_1 C_2}}, \tag{13}$$

$$Q = \sqrt{\frac{C_1}{C_2}}. \tag{14}$$

From Eq. (13), it is seen that the cut-off frequency can be tuned by the biasing current I_0. According to Figure 10, input voltage combinations of different filter characteristics can be given by Table 3.

Table 3. Input voltage combinations for different filter characteristics.

Filter type	V1	V2	V3
LP	V_{in}	0	0
BP	0	0	V_{in}
HP	0	V_{in}	0
BR	V_{in}	V_{in}	0

Figure 11 depicts the simulated frequency responses of the universal filter for the LP, HP, BP, and BR configurations.

The simulated frequency responses of the BP filter at different biasing currents are given in Figure 12. This graph illustrates the electronic tuning capability of the filter. Figure 13 displays the simulated frequency and phase responses of the BR filter.

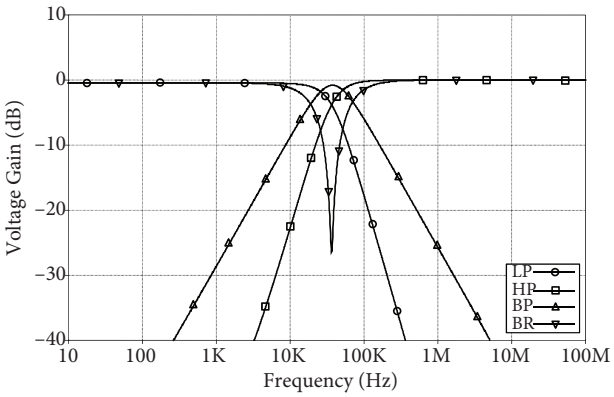

Figure 11. The frequency responses of the DDCCC-based universal filter for LP, HP, BP, and BR.

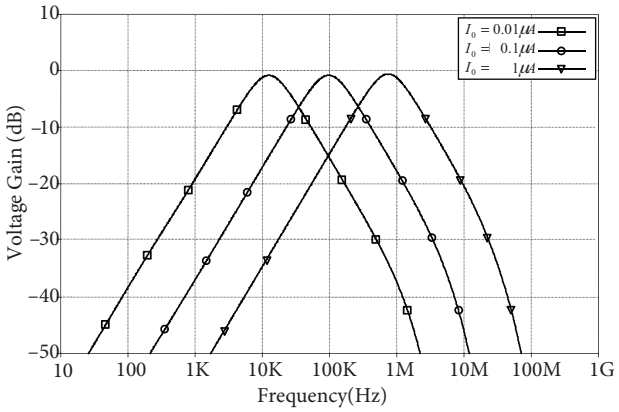

Figure 12. The frequency responses of the BP filter for different values of the biasing current I_0.

5.2. DDCCC-based tunable active resistor application

Figure 14 displays two types of active resistors designed by using only two DDCCCs. The proposed active resistors might be tuned by the biasing current of the DDCCC. The resistance value of the resistors is defined as:

$$|R_{AB}| = \frac{V_{AB}}{I_{AB}} = 2 \cdot R_X, \tag{15}$$

where all biasing currents are equal to I_0. The I-V characteristics of the designed positive and negative resistors are shown in Figures 15 and 16, respectively.

Behaviors of the resistors are extremely linear between –300 mV and +300 mV as seen in Figures 15 and 16.

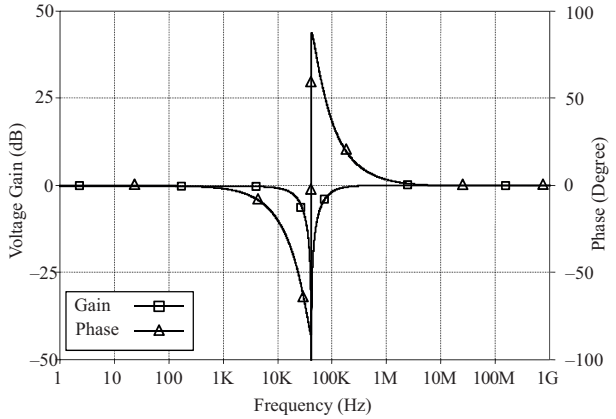

Figure 13. Frequency and phase responses of the band reject filter.

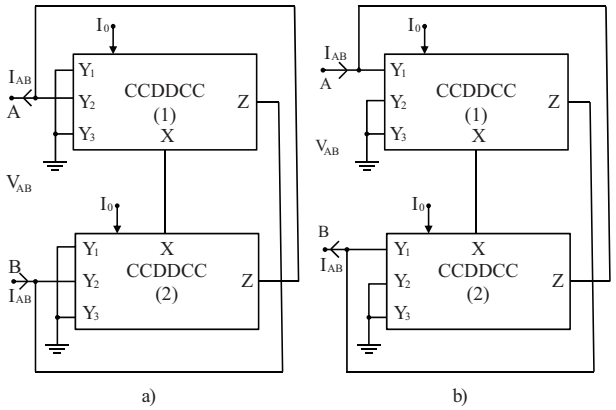

Figure 14. The DDCCC-based a) negative active resistor and b) negative active resistor.

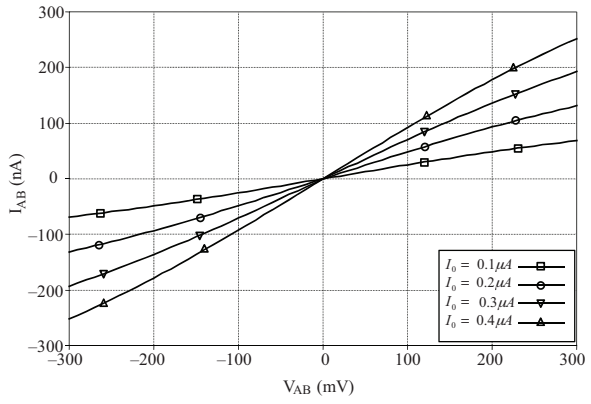

Figure 15. The I-V characteristics of the positive active resistor.

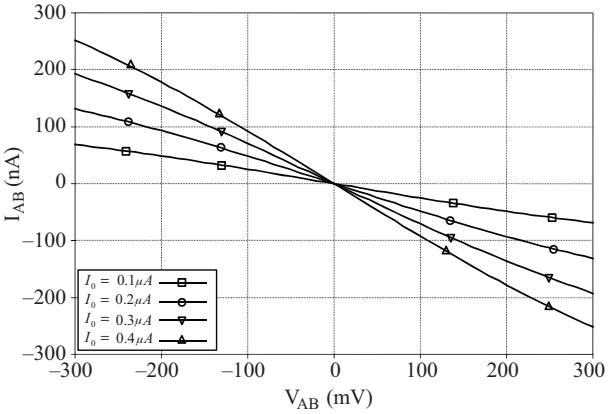

Figure 16. The I-V characteristics of the negative active resistor.

To test the applicability of the designed active resistor, an inverting amplifier based on the AD712 op-amp is built as shown in Figure 17.

Figure 18 shows the voltage gain of the inverting amplifier for the various biasing currents. The voltage gain of the amplifier can be defined as $-R_{AB2}/R_{AB1}$. It is seen that the gain of the amplifier can be controlled by the biasing current.

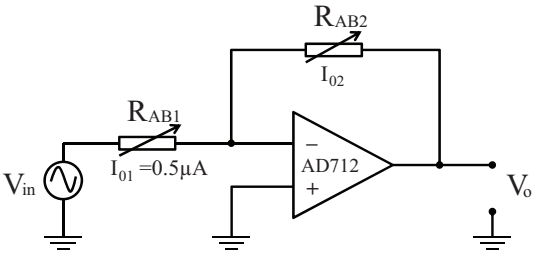

Figure 17. The inverting amplifier using an active resistor.

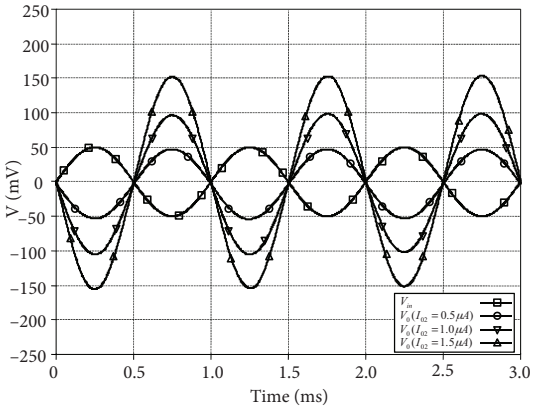

Figure 18. The voltage gain variations of the inverting amplifier for the different biasing currents.

It is clear that the simulation results confirm the theoretical approach of the proposed resistor based on the DDCCC.

6. Discussion and conclusion

A novel FGMOS-based DDCCC structure is proposed in this study. The proposed circuit designed using FGMOS transistors offers some novelties required recently such as low power consumption, wide tuning range of the intrinsic resistance, and simplicity of the circuit structure. The circuit employs only 14 transistors. The proposed circuit is theoretically analyzed and simulated by SPICE. It is observed that the simulation results confirm to the theoretical approaches. The value of the intrinsic resistance at the input port of the DDCCC can be varied from 30 KΩ to 17 MΩ by changing the value of the control current I_0, with excellent correspondence between the theoretical and simulation results. The proposed circuit requires a low voltage as well as ± 0.6 V. This circuit consumes only 7.38 μW. It is highly suitable for low-power applications. The maximum THD value of the proposed circuit is 1.65% for 800 mV_{pp}. This is a reasonable value when it is compared with other studies. To demonstrate the applicability of the theory, a current controlled universal filter and tunable positive and negative active resistor structures are designed using the proposed DDCCC. Satisfactory results are obtained from applications. The development of the proposed circuit has a main advantage in the ability to provide low-power system implementations. Ultimately, such electronic controllability of the proposed circuit is an attractive feature in general electronic circuit design and the circuit is a useful structure for low-voltage applications requiring low power consumption.

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