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Cascaded half-full-bridge PWM multilevel inverter configuration

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Abstract: This paper presents a single-phase, cascaded half-full-bridge PWM multilevel inverter topology. It is made up of a main inverting H-bridge legs and level-clamping half-bridge circuits, each having its own dc source. The single-carrier, multilevel PWM scheme is employed to generate gating signals for the power switches. The modulation scheme is hybridized to enable the output voltage of the proposed inverter configuration to inherit the features of switching-loss reduction from fundamental PWM and good harmonic performance from multiple sinusoidal PWM. Moreover, a simple base PWM circulation scheme is also introduced in this work to obtain a resultant sequential switching hybrid PWM (SSHPWM) circulation that balances power dissipation among the four power switches of the main H-bridge module. Operational principles with switching functions are given. For a modulation index of 0.9, the proposed inverter configuration was subjected to an R-L load and the respective numbers of output voltage level were synthesized. FFT analyses of the output voltage waveforms were carried out and the corresponding THD value of 13.16% was obtained. To verify the performance of the proposed inverter architecture, simulations and experiments were carried out on a 2.95 kW rated prototype of the proposed inverter for an R-L load and adequate results were obtained.

Key words: Inverter, multilevel, PWM, H-bridge, cascade

1. Introduction

Numerous industrial applications have begun to require higher power apparatus in recent years [1]. Power-electronic inverters are becoming popular for various industrial drive applications [2]. A multilevel inverter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. Recently, multilevel power conversion technology has been developing in the area of power electronics very rapidly with good potential for further developments. As a result, the most attractive applications of this technology are in the medium to high voltage ranges [3]. A multilevel inverter not only achieves high power ratings, but also enables the use of renewable energy sources. Renewable energy sources such as photovoltaic, wind, and fuel cells can be easily interfaced to a multilevel inverter system for a high power application.

The advantage of multilevel inverters is their smaller output voltage step, which results in high voltage capability, lower harmonic components, lower switching losses, better electromagnetic compatibility, and high power quality [1,4]. In addition, it can operate at both fundamental switching frequency and high switching frequency PWM. It must be noted that lower switching frequency usually means lower switching loss and higher efficiency [5].

The results of a patent search show that multilevel inverter circuits have been around for more than 25 years. Today, multilevel inverters are extensively used in medium voltage levels with high-power applications [6].

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The field applications include use in industrial medium-voltage motor drives [7], utility interface for renewable energy systems [8], flexible AC transmission systems (FACTS), and traction drive systems [9,10]. Subsequently, several multilevel inverter configurations have been developed [11–16] in addition to the fundamental topologies: cascaded multicell with separate dc sources, diode clamped (neutral-clamped), and capacitor-clamped (flying capacitors) [1].

Abundant modulation techniques and control paradigms have been developed for multilevel converters such as sinusoidal pulse width modulation (SPWM), selective harmonic elimination (SHE-PWM), and space vector modulation (SVM) [17,18].

One clear disadvantage of multilevel power conversion is the great number of power semiconductor switches needed. Another disadvantage of multilevel power converters is that the small voltage steps are typically produced by isolated voltage sources or a bank of series capacitors. Isolated voltage sources may not always be readily available and series capacitors require voltage balance [19].

Although low-voltage-rated switches can be utilized in a multilevel converter, each switch requires a related gate driver and protection circuits. This may lead to the overall system being more expensive and complex [20]. Therefore, in practical implementations, a decrease in the number of switches and gate driver circuits is very important [21].

In response to the aforementioned need in a multilevel inverter system, a new topology of a symmetrical 11-level single-phase inverter is proposed herein. In the proposed inverter topology, half-bridge inverter configurations are linked with H-bridge module through dc sources. With this arrangement of circuit devices, the component count of the proposed inverter configuration is reduced when compared with the conventional CHB inverter, for the same output voltage level. Operational principles and switching functions are analyzed. Simulation and experimental results are presented to verify the validity of the proposed inverter.

2. Principle of operation of the proposed inverter

The proposed cascaded half-full-bridge PWM multilevel inverter topology is shown in Figure 1. It is made up of a main inverting H-bridge leg and level-clamping half-bridge circuits; each has its own dc source.

Proper switching of the cells can produce eleven output-voltage levels with a maximum value of 5Vs: Vs, 2Vs, 3Vs, 4Vs, 5Vs, 0, –Vs, –2Vs, –3Vs, –4Vs, –5Vs. With the employed modulation scheme herein, any voltage level below this maximum can be synthesized by adjusting the modulation index. The switching combinations that generate the output voltage levels, (Vs, 2Vs, 3Vs, 4Vs, 5Vs, 0, –Vs, –2Vs, –3Vs, –4Vs, –5Vs) for one cycle are shown in Table 1. Figures 2 and 3 typify switching combinations that synthesize Vs and 5Vs, respectively, wherein the current conduction paths in the proposed inverter configuration are shown.

3. PWM scheme

A single carrier sinusoidal PWM (SCSPWM) scheme is employed for the generation of gating signals. The basic principle of the proposed switching strategy is to generate gating signals by comparing rectified sinusoidal modulating/reference signals, at the fundamental frequency, with only one triangular carrier wave that has higher switching frequency compared to the fundamental. For n-level SCSPWM, k numbers of rectified sinusoidal modulating signals have the same fundamental frequency, f_m, and amplitude, A_m, with dc bias of A_c (peak–peak amplitude of the triangular carrier signal) as a difference between each two successive signals of these signals [22,23]. The switching/modulation scheme adopted in the proposed cascaded multilevel inverter is illustrated in Figure 4.

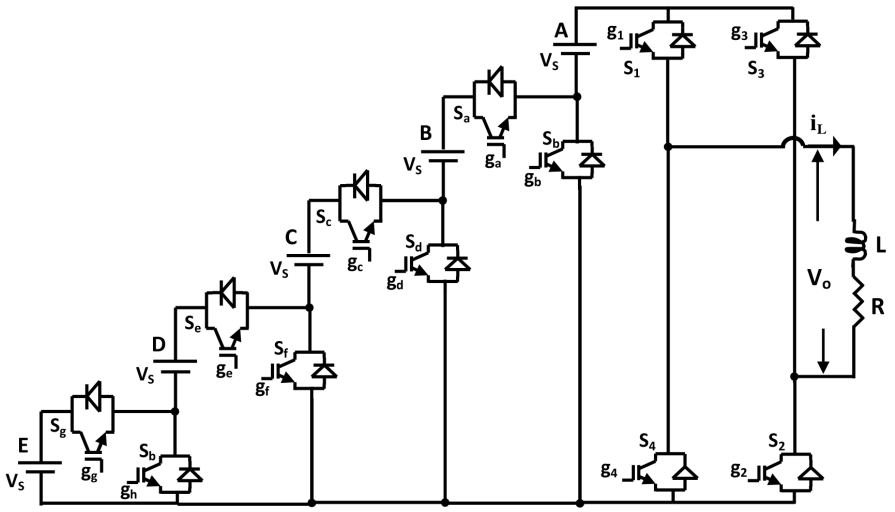


Figure 1. Power circuit of the proposed single-phase PWM multilevel inverter.

Table 1. Output voltage according to the switches on–off conditions.

v_o	i_L	S_1	S_2	S_3	S_4	S_a	S_b	S_c	S_d	S_e	S_f	S_g	S_h
V_S	positive	on	on	off	off	off	off	off	off	off	off	off	off
V_S	negative	off	off	off	off	off	on	off	off	off	off	off	off
$2V_S$	positive	on	on	off	off	on	off	off	off	off	off	off	off
$2V_S$	negative	off	off	off	off	off	off	off	off	off	off	off	off
$3V_S$	positive	on	on	off	off	on	off	on	off	off	off	off	off
$3V_S$	negative	off	off	off	off	off	off	off	off	off	on	off	off
$4V_S$	positive	on	on	off	off	on	off	on	off	on	off	off	off
$4V_S$	negative	off	off	off	off	off	off	off	off	off	off	off	on
$5V_S$	positive	on	on	off	off	on	off	on	off	on	off	on	off
$5V_S$	negative	off	off	off	off	off	off	off	off	off	off	off	off
0	positive	S_{1U} on,		off	off	off	off	off	off	off	off	off	off
0	negative	off	off	S_{3U} on,		off	off	off	off	off	off	off	off
$-V_S$	positive	off	off	off	off	off	on	off	off	off	off	off	off
$-V_S$	negative	off	off	on	on	off	off	off	off	off	off	off	off
$-2V_S$	positive	off	off	off	off	off	off	off	on	off	off	off	off
$-2V_S$	negative	off	off	on	on	on	off	off	off	off	off	off	off
$-3V_S$	positive	off	off	off	off	off	off	off	off	off	on	off	off
$-3V_S$	negative	off	off	on	on	on	off	on	off	off	off	off	off
$-4V_S$	positive	off	off	off	off	off	off	off	off	off	off	off	on
$-4V_S$	negative	off	off	on	on	on	off	on	off	on	off	off	off
$-5V_S$	positive	off	off	off	off	off	off	off	off	off	off	off	off
$-5V_S$	negative	off	off	on	on	on	off	on	off	on	off	on	off

Hybrid modulation is the combination of fundamental frequency modulation (FPWM) and multisinusoidal PWM (MSPWM) in the H-bridge inverter cell operation, so that the inverter outputs inherit the features of switching-loss reduction from FPWM and good harmonic performance from MSPWM. In this modulation technique, the four switches of the H-bridge inverter cell, S_1–S_4, are operated at two different frequencies; one leg of the inverter is being commutated at FPWM, while the other leg is simultaneously switched at MSPWM, for a cycle. The order of switching is reversed between the legs in the next succeeding cycle of the output voltage.

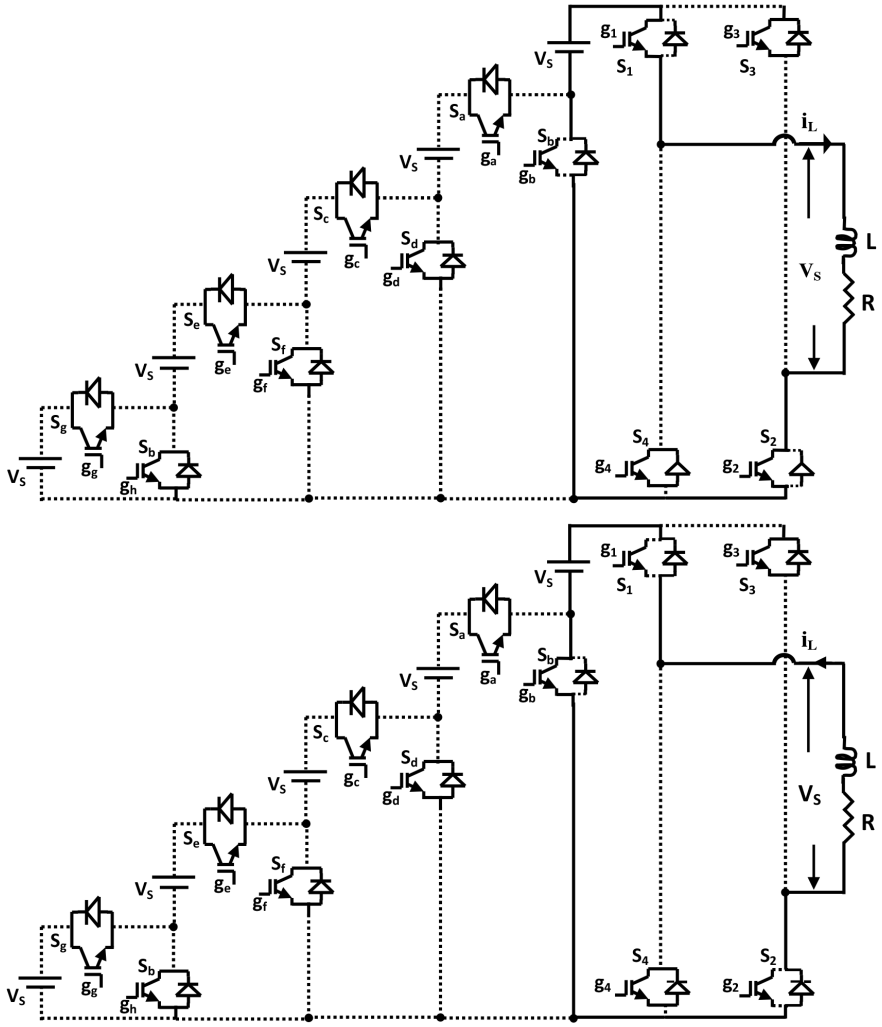


Figure 2. Typical operational states of switches according to the switches on–off conditions for the synthesis of V_S in the proposed single-phase PWM multilevel inverter.

Therefore, the resultant switching patterns are the same as those obtained with MSPWM. The logic signals A and B, at the fundamental frequency f_m, in Figure 4 are used to hybridize the modulation process herein. It can be observed from the proposed switching waveforms in Figure 4 that the concept and implementation of hybrid modulation make the average switching waveform of all the switches in the H-bridge cell the same. As a result, the power switches in the H-bridge cell operate in a balanced condition with the same power-handling capability and switching losses.

The frequency and amplitude modulation index expressions for multilevel inverters [24,25] still hold for the proposed inverter configuration. They are given, respectively, as

$$M_f = \frac{f_c}{f_m} \tag{1}$$

$$M_a = \frac{A_m}{A_c(k-1)} \tag{2}$$

where f_c and A_c are the frequency and peak-to-peak value of the triangular carrier signal, respectively. f_m

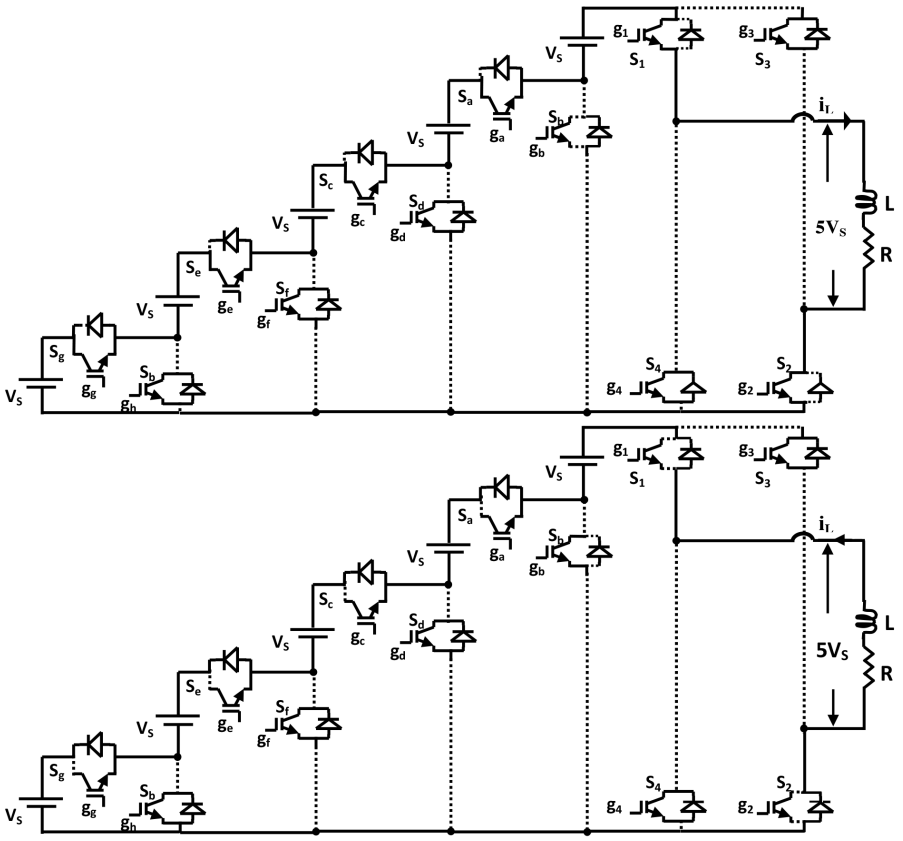


Figure 3. Typical operational states of switches according to the switches on–off conditions for the synthesis of $5V_S$ in the proposed single-phase PWM multilevel inverter.

and A_m are the same defined variables corresponding to the modulating signals. k is the number of voltage level synthesized, per half-cycle; in this case, $k = 5$.

The basic principle in generating all the gate signals begins from the comparison of the respective modulating signals with the carrier wave. The actual gate signals for the H-bridge switches are produced by the logical combinations of the results of such comparisons and the synchronized base square waveforms, having frequency of $\frac{f_m}{2}$. These square waves can be easily obtained from basic J-K flip-flops configured in toggle mode and clocked at the fundamental frequency.

All the gating signals of the proposed single-phase, multilevel inverter can be derived from the use of basic logical comparator, AND, OR, and NOT gates.

$$g_1 = [(\{[((R_1 > T).A) + ((R_1 < T).B)]\}.C) + A.D] \tag{3}$$

$$g_2 = [(\{[((R_1 > T).A) + ((R_1 < T).B)]\}.D) + A.C] \tag{4}$$

$$g_3 = \overline{g_2} \tag{5}$$

$$g_4 = \overline{g_1} \tag{6}$$

$$g_a = (R_2 > T) \tag{7}$$

$$g_b = \overline{g_a} \tag{8}$$

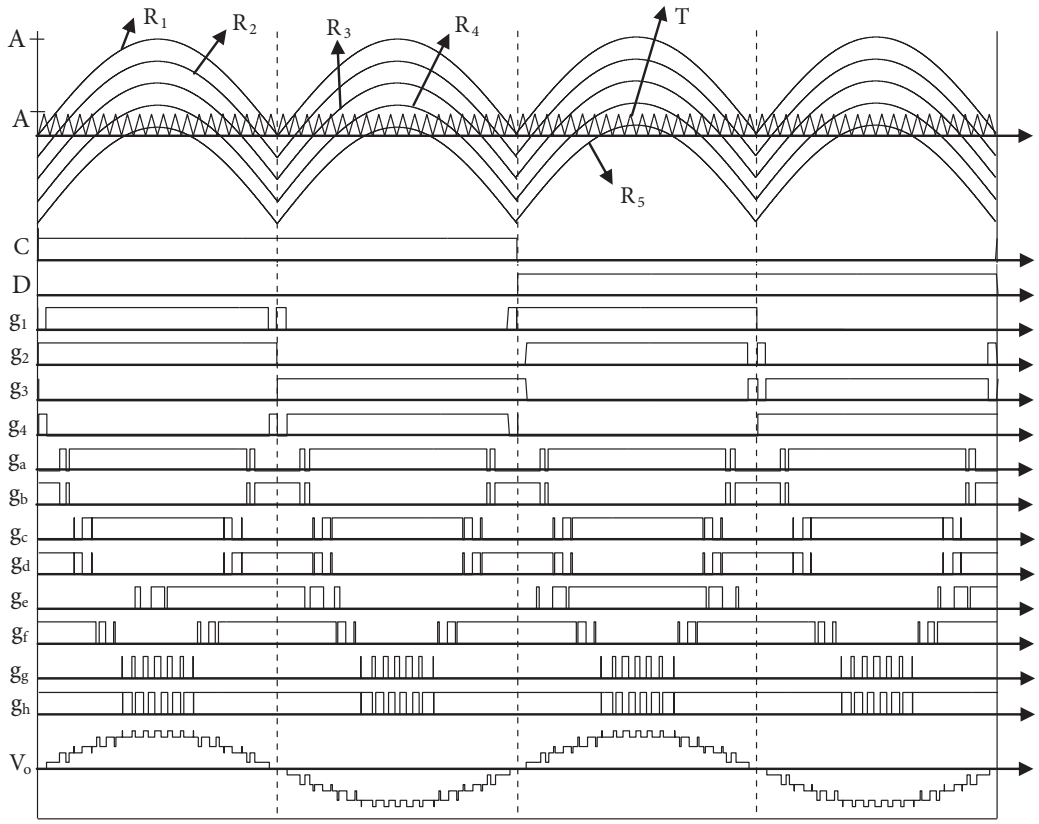


Figure 4. Switching scheme of the proposed cascaded half-full-bridge PWM multilevel inverter topology.

$$g_c = (R_3 > T) \tag{9}$$

$$g_d = \overline{g_c} \tag{10}$$

$$g_e = (R_4 > T) \tag{11}$$

$$g_f = \overline{g_e} \tag{12}$$

$$g_g = (R_5 > T) \tag{13}$$

$$g_h = \overline{g_g} \tag{14}$$

Note that A and B are square waves at the fundamental frequency and synchronized to the reference signals.

Analytical expressions for the average power losses in the main power semiconductor switches can be obtained in terms of the voltage and current amplitudes, depth of modulation, and power factor for typical conditions prevailing in pulse width modulated inverters [26]. For each of the active switches (IGBT) used herein, a good approximation for the average on-state loss, P_T, is

$$P_T = \frac{V_{TO} I_m}{2\pi}\left\{1 + \frac{\pi}{4} M_a \cos\varphi\right\} + \frac{K_T I_m^2}{2\pi}\left\{\frac{\pi}{4} + \frac{2}{3} M_a \cos\varphi\right\} \tag{15}$$

where $V_{TO}, K_T, I_m, M_a, and \varphi$ are the constant on-state voltage across a switch, on-state resistance, peak load current through a device, applied modulation index, and power factor angle, respectively. The first term in (15)

is the loss due to the constant components of on-state voltage V_{TO}, while the second term is the loss due to the linear dependence on current of the on-state voltage as expressed in terms of K_T. Hence, (15) can be rewritten in terms of these two components as

$$P_T = P_{TC} + P_{TV} \tag{16}$$

Moreover, the conduction loss expression, P_D, for the diodes in the power circuit can be written as

$$P_D = \frac{V_{DO} I_m}{2\pi}\left\{1 - \frac{\pi}{4} M_a \cos\varphi\right\} + \frac{K_D I_m^2}{2\pi}\left\{\frac{\pi}{4} - \frac{2}{3} M_a \cos\varphi\right\}, \tag{17}$$

where $V_{DO} and K_D$ are the constant on-state voltage across a diode and on-state resistance, respectively. Similarly, (17) can be rewritten as

$$P_D = P_{DC} + P_{DV} \tag{18}$$

Equations (15) and (17) can be normalized to have the 3-dimensional plots of $\frac{2\pi}{V_{TO} I_m} P_T$, $\frac{2\pi}{K_T I_m^2} P_T$, $\frac{2\pi}{V_{TO} I_m} P_D$, $\frac{2\pi}{K_T I_m^2} P_D$ against the modulation index and the load power factor as depicted in Figure 5.

The two components of the switch's losses can be seen increasing while the corresponding diode losses decrease complimentarily as the load power factor improves. Similar trends are apparent as depth of modulation increases.

4. Simulation and experimental results

4.1. Simulation results

MATLAB SIMULINK simulated the proposed single-phase, cascaded inverter in accordance to the switching scheme presented in section 3. The PWM switching patterns are generated by the implementation of the single-carrier PWM concept for multilevel inverter topologies. Herein then, a single triangular carrier, at the desired switching frequency is compared, respectively, with five rectified sinusoidal reference waves at fundamental frequency of 50 Hz, as depicted in Figure 4. Subsequently, the logical combination of the base waveforms with the comparing process produced PWM gating signals for the power switches. Figure 6 shows the simulated waveforms of the output voltage and load current for an RL load, when modulation index is 0.9; V_s = 100 V, R = 35 Ω, L = 50 mH, and the triangular carrier wave switching frequency is 5 kHz. The fundamental component of the output load voltage is also attached therein, depicting its high/absolute dominance to other harmonic components. Displayed in Figure 7 is the corresponding harmonic profile of the proposed inverter output voltage. Beside this loading condition, the inverter is further subjected to extreme loading conditions: purely inductive and capacitive loading. The resultant output waveforms and spectral of the output voltages are shown in Figure 8.

Following the implemented modulation scheme, the current profile of the dc sources is provided in Figure 9. All the sources are of equal voltage and current rating. However, the different rate of discharge of these sources is a drawback of this inverter topology.

The maximum blocking voltage profile of the power switches is shown in Figure 10. The use of half-bridge circuits allows five out of the eight power switches in the half-bridge circuits to have the maximum blocking voltage of V_S.

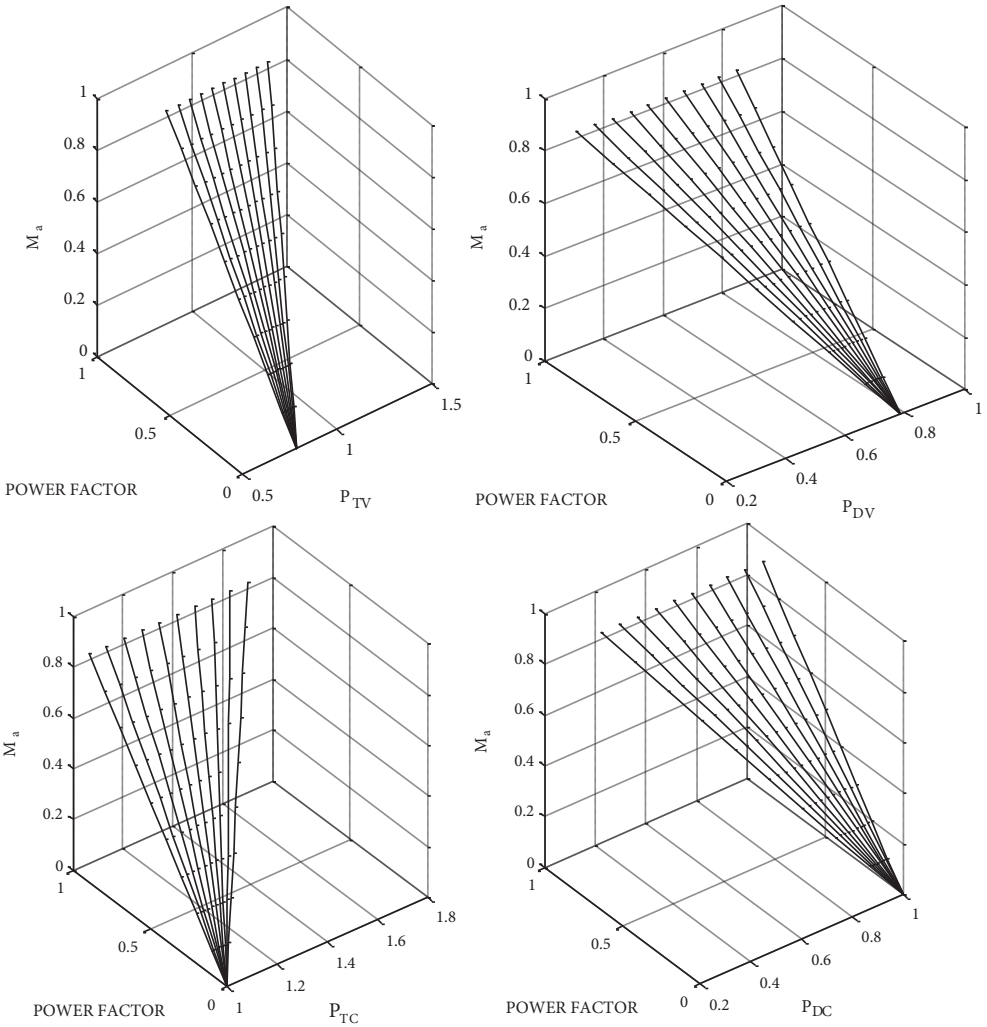


Figure 5. Normalized plots of P_{TC}, P_{DC}, P_{TV}, and P_{DV} and their variation with power factor and depth of modulation.

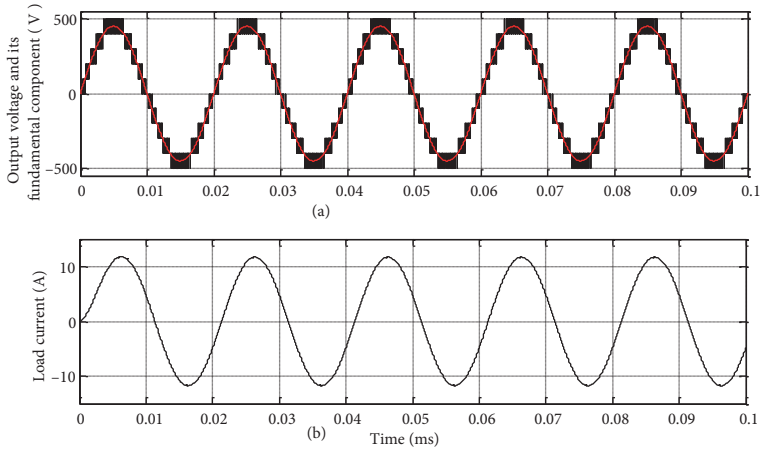


Figure 6. Simulation results of output voltage and current for RL load: (a) Output voltage of the multilevel inverter and its fundamental component. (d) Load current.

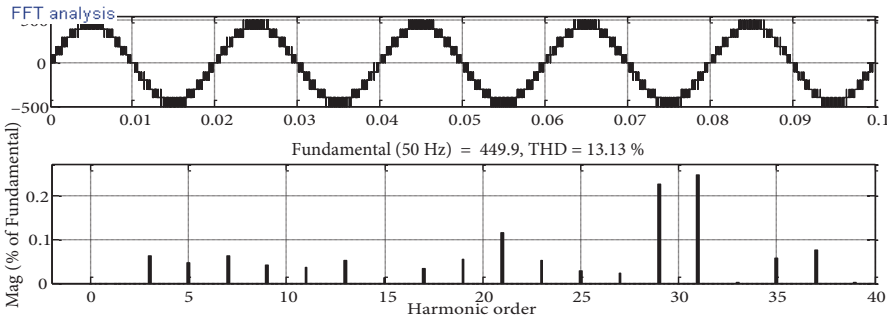


Figure 7. Harmonic profile of the inverter output voltage for RL load.

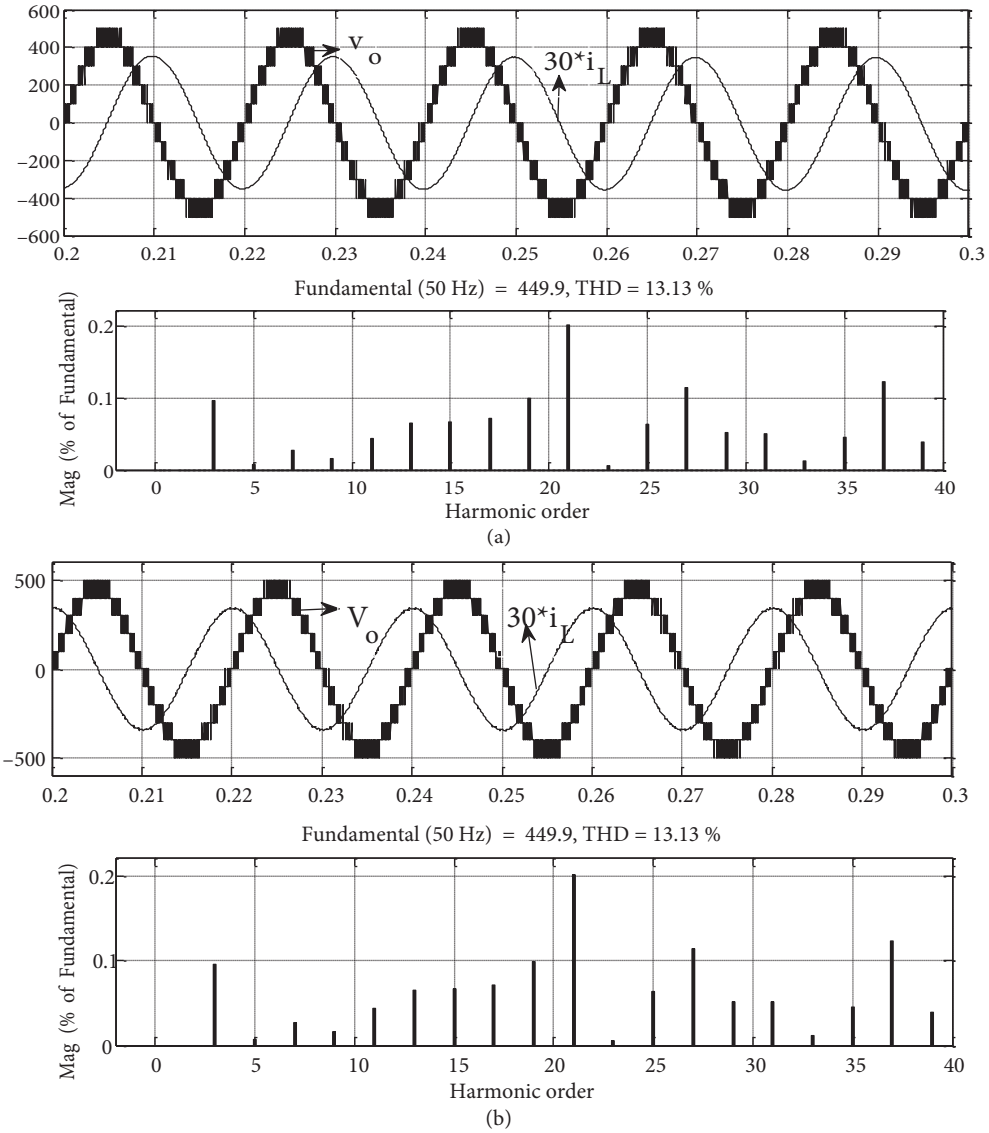


Figure 8. Simulation results of output voltage and current and the corresponding output voltage frequency spectrum for purely inductive and capacitive loading condition: (a) Pure inductive load (d) Pure capacitive load.

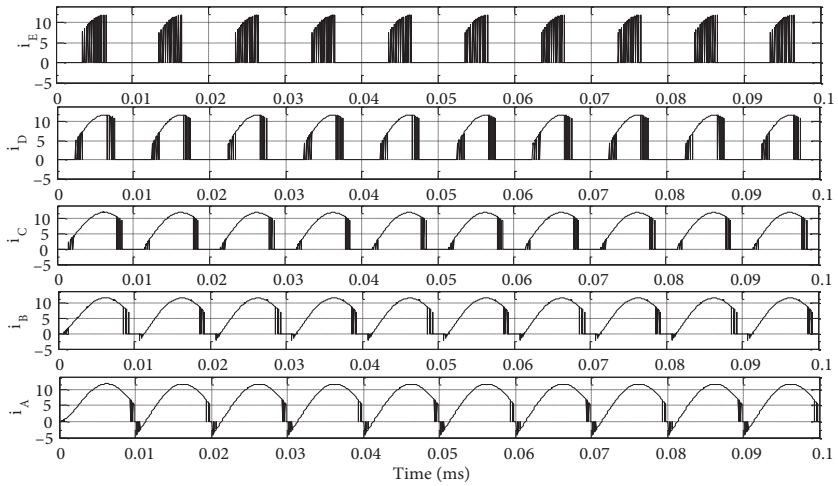


Figure 9. Current profile of the dc voltage sources.

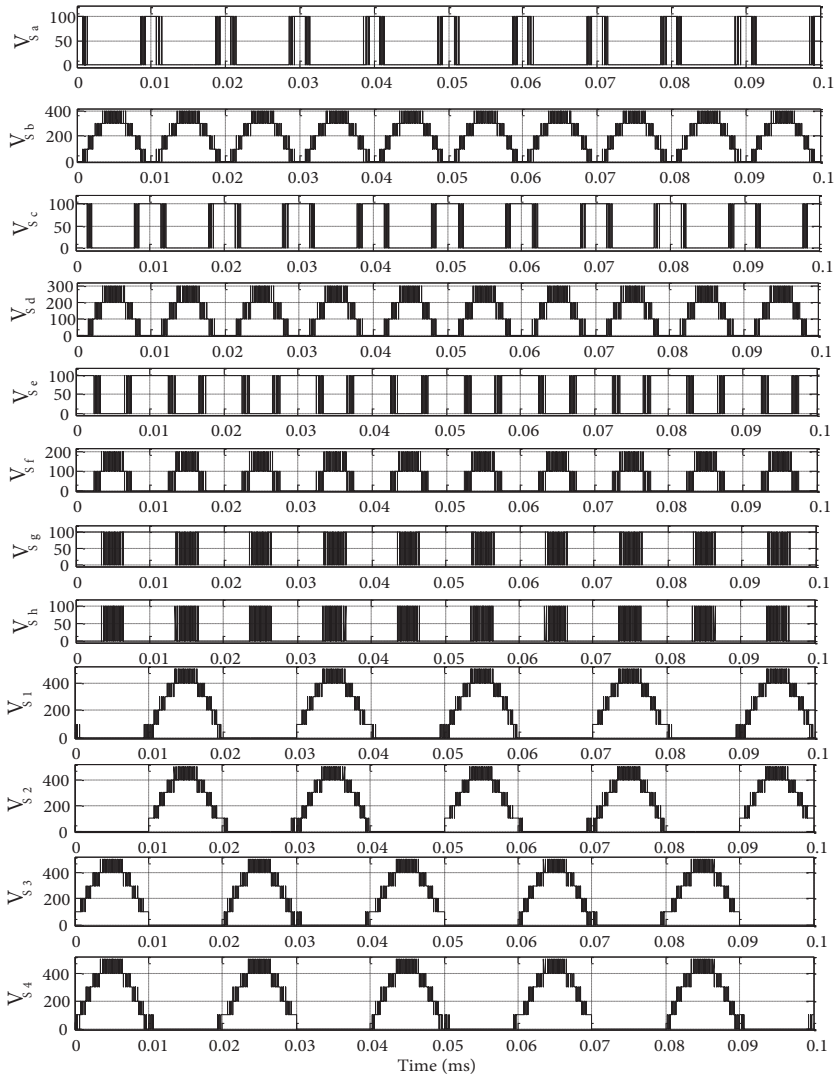


Figure 10. Maximum blocking voltage profile of the power switches in the proposed half-full-bridge inverter configuration.

4.2. Experimental results

Following the simulation results, a laboratory prototype (shown in Figure 11) of the multilevel PWM inverter was set up and tested to verify its validity. Table 2 gives the prototype specifications and parameters.

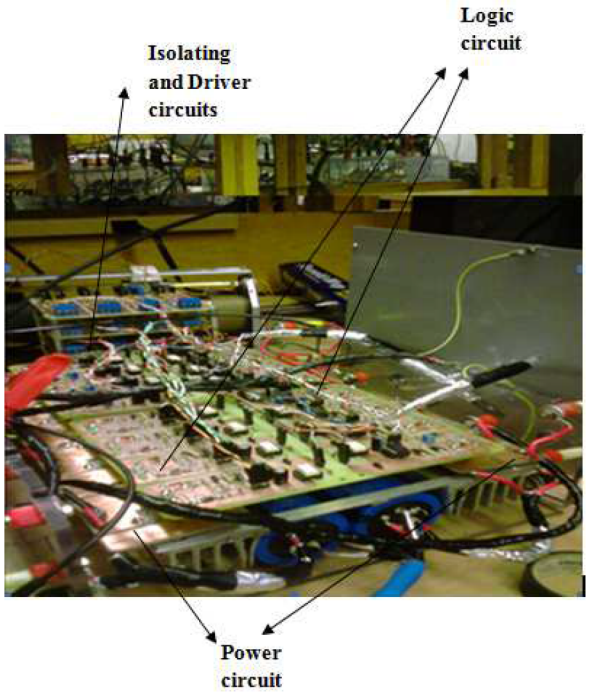


Figure 11. Laboratory prototype setup for the proposed single-phase, cascaded half-full-bridge PWM multilevel inverter configuration.

Table 2. Prototype specification.

Power circuit switches: IXXS FII40-06D
V_S : 100 V
R = 35 Ω, L = 50 mH

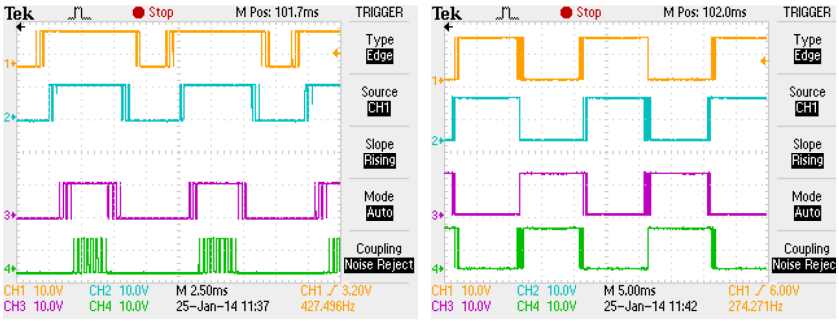
Both the triangular carrier wave, at switching frequency of 5 kHz, and reference rectified sinusoidal signals, at fundamental frequency of 50 Hz, were generated using IC TL084. In addition, the base square waves were generated using 4027 dual J-K flip-flop CMOS IC connected in toggle mode and clocked as earlier indicated in section 3. Figure 12 shows typical experimental gating signal waveforms.

Figure 13 shows the experimental waveforms of the inverter output voltages and load current corresponding to a modulation index of 0.9.

For this operating condition and with the specified R-L load in Table 2, Table 3 gives the measured parameters of the implemented prototype.

Table 3. Parameters of the implemented prototype.

Output voltage (rms): 353.55 V
Load current (rms): 8.34 A
Measured output power: 2.95 kW



(a) *(b)*

Figure 12. Experimental gating signals: (a) g_a (CH1), g_c (CH2), g_e (CH3), g_g (CH4). (b) g_1 (CH1), g_2 (CH2), g_3 (CH3), g_4 (CH4).

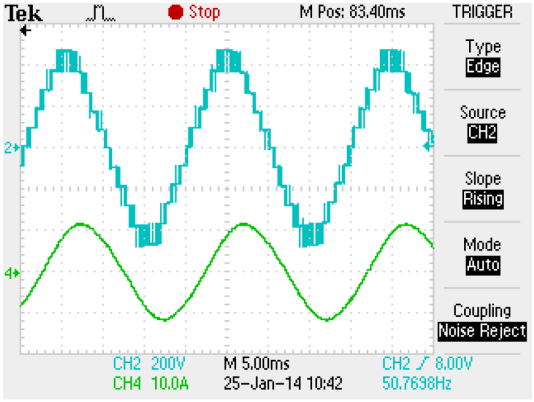


Figure 13. Experimental results of output voltages and load current.

5. Conclusion

A single-phase multilevel inverter configuration with reduced number of switches for medium and high power applications is proposed. The proposed inverter can generate a greater number of voltage levels with the same number of separate dc voltage sources and reduced number of power switches when compared with the conventional cascade H-bridge multilevel inverter. Therefore, the size and power consumption of driving circuits of inverter are reduced. It has been shown that the modulation method adopted enables the proposed inverter output voltage to inherit the features of switching-loss reduction from FPWM and good harmonic performance from MSPWM. The synthesized output voltage of the proposed inverter achieved a harmonic profile of 13.16% total harmonic distortion (THD) under the specified loading condition. The performance of the proposed inverter topology has been presented through simulations and experiments on a 2.95 kW rated prototype of the proposed inverter for an R-L load; the results obtained were adequate.

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