Implementation of a modified SVPWM-based three-phase inverter with reduced switches using a single DC source for a grid-connected PV system

Venkatesan MANI[1,*], Rajeswari RAMACHANDRAN[2], Devarajan NANJUNDAPPAN[2]
[1]Anna University, Chennai, Tamil Nadu, India
[2]Department of Electrical Engineering, Government College of Technology, Coimbatore, Tamilnadu, India

Abstract: Application of multilevel inverters has been an active research area in recent years due to their growing importance in various diversified electrical utilities. A three-phase inverter with a single DC source employing a three-phase transformer for a grid-connected photovoltaic (PV) system controlled using the modified space vector pulse width modulation technique (MSVPWM) for fifteen switches is presented in this paper. An MSVPWM technique is implemented through a field-programmable gate array (FPGA) and generates high quality gate pulses to the switches in the inverter. The main advantages of the proposed inverter topology are reduced number of power switches, transformers and minimum total harmonic distortion (THD). The perturb and observe maximum power point algorithm is used to obtain the maximum power from the PV panel at all climatic conditions. The performance of the proposed system is validated through MATLAB/Simulink as well as an FPGA-based prototype model.

Key words: Multilevel inverter (MLI), PV, single DC source, MSVPWM, FPGA

1. Introduction

Nowadays, a number of research works focus on renewable energy-based multilevel inverters (MLIs), particularly in grid-connected applications due to their potential excellence in maintaining the harmonic standards of IEEE 519-1992. Among the various renewable energy sources, PV systems have been extensively utilized as they are pollution free and have the largest energy potential. A large number of nonlinear loads have been deployed for commercial and noncommercial purposes due to the demand from electrical utilities, where the PV panel has been used as the input DC source. Conventional three-level inverters have major drawbacks such as high dv/dt, high power losses, electromagnetic interference problems, and high THD. Hence MLIs are extensively used especially in grid-connected applications [1–5]. MLIs can be classified into three topologies, namely diode clamped, flying capacitors, and H-bridge cells with separate DC sources. Among these inverter topologies, clamped diode needs complex pulse width modulation control because additional capacitors and diodes are necessary for generating more levels and more power losses. In the case of flying capacitor MLIs, the capacitor voltage balancing problem dominates and requires a complex switching algorithm to solve. Moreover, flying capacitor MLIs are not suitable for high voltage and high power applications. In order to control the MLIs various types of control strategies and modulation schemes are presented [6–9]. In recent years, the cascaded H bridge multilevel inverter has been widely used in high voltage and high power applications with separate DC sources that could easily be interfaced to the MLIs to deliver higher output voltages with minimum THD.

---

*Correspondence: venkatesangct@gmail.com

However, the major limitation is that cascade MLIs require a greater number of DC sources for an M level inverter ($[(M-1)/2] \times 3$). Additionally, a short circuit may take place across the independent DC sources and the topology comprises a greater number of switches, which in turn results in excessive power losses, increases the converter size and cost, and reduces the reliability of the system [10,11]. Cascade MLIs employing a three-phase transformer with a single DC input are proposed in the literature, but this requires additional transformers, which results in increased system size and cost [12,13]. To overcome the above-stated problems, an MSVPWM-based three-phase inverter with reduced switches using a single DC source for a grid-connected PV system is presented in this paper. A proportional integral (PI) controller is used as a current controller in this paper [14–16]. Different types of maximum power point tracking (MPPT) algorithms are presented in the literature [17,18]. Based on the survey, the perturb and observe (P&O) MPPT algorithm can be chosen to obtain the maximum power from the PV panel at all climatic conditions. In the proposed work the number of switches required for the inverter is reduced and this results in reduced switching losses and the THD is reduced. The proposed topology is validated through MATLAB/Simulink and implemented using the FPGA-based prototype model.

2. PV system description

A semiconductor device that converts solar irradiation into electrical energy is named a photo voltaic cell and this effect is called the photovoltaic effect. The PV panel acts as the input DC source for the inverter. The electrical power generated by a solar PV panel mainly depends on the operating conditions, solar irradiation in w/m^2, temperature in degree Celsius, number of cells, short circuit current (I_{sc}), etc. In this proposed system, in order to attain the maximum power from the PV panel, the P&O MPPT algorithm has been used [19–22]. The voltage and current relations for a single diode model array can be expressed as

$$I = I_L - I_0 (\exp\left[\left(\frac{q}{\gamma k T_c}\right)?\,(V + IR_s)\right]$$ (1)

where I_L is the photon current, I_0 is the reverse saturation current of the diode, q is the electron charge constant (1.6×10^{-19} C), k is the Boltzmann constant, and T_c is the cell temperature in $^\circ$ C. The boost converter comprises a current smoothening inductor L_1, MOSFET, and diodes. The boost converter is used to boost the input DC voltage and is pumped to the inverter. This step up conversion is carried out by injecting the gate pulses to the MOSFET switch S_1, as shown in Figure 1. The two capacitors are used in the DC bus C_1, C_2 with the same rating.

3. Proposed three-phase inverter configuration

Figure 1 shows the proposed MSVPWM-based three-phase inverter with reduced switches using a single DC source for a grid-connected PV system. Each of the single-phase circuits consists of an auxiliary circuit along with the full bridge inverter. The auxiliary circuit comprises four power diodes, namely D_1, D_2, D_3, and D_4, with a single power switch M_1 and the full bridge inverter circuit consists of four power switches namely M_2, M_3, M_4, and M_5. R_+ and R_- are the phase and neutral outputs of the first phase of the inverter.

This proposed topology comprises three single inverters, which are connected in parallel with a common DC bus. The outputs for the three single-phase five-level inverter circuit (R_+, R_-, Y_+, Y_-, $B_+ B_-$) are shown in Figure 1. Each single phase inverter produces the five-level output voltage, which is synthesized from the single DC bus voltage. These outputs are fed to the three-phase transformer. The MSVPWM technique is used
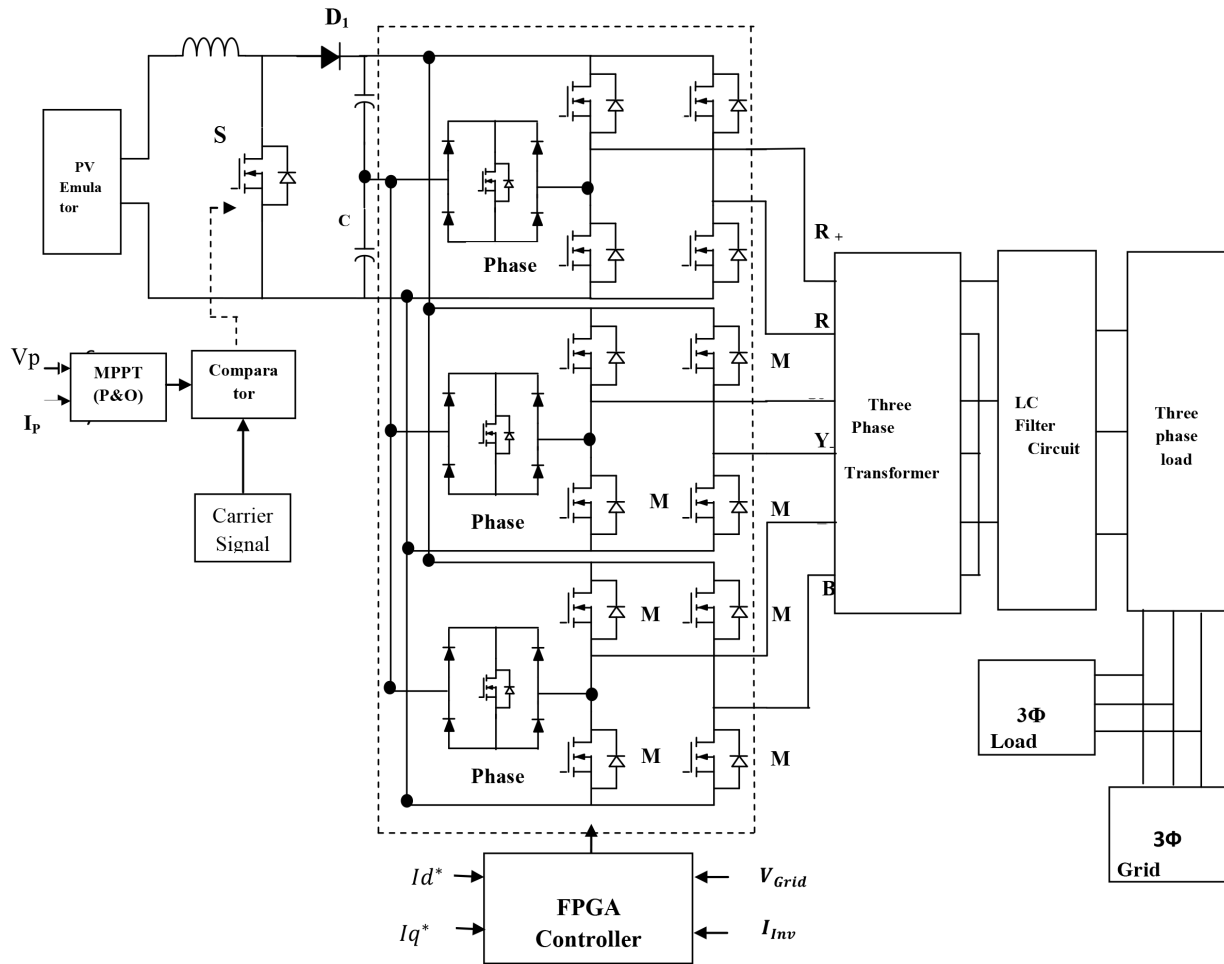
Figure 1. Proposed three-phase inverter configuration with a single DC source employing a three-phase transformer.

to generate the proper gating pulses to the switches in the inverter. The filtered sinusoidal output from the inverter is fed to the isolation transformer. The isolation transformer is connected to the grid and the filtered sinusoidal waveform could be stepped up, stepped down, or sent as such depending on the requirement and is interfaced with the grid. The proposed three-phase inverter topology with single DC source is modified from the references [23,24].

3.1. Design of LC filter

The three-phase LC filter circuit is designed to filter the current injected into the grid. The injected current must be sinusoidal with low harmonic distortion. The values of L and C obtained from Eqs. (2) and (3) are as follows:

Filter inductance (H) is given by the equation

$$L = \frac{1}{8} * \frac{V_a}{\Delta i_{lmu} * fs} \tag{2}$$

where Δi_{lmu} is the ripple current. This can be 10% of rated current.

Filter capacitor in C is given by

$$C = \frac{15\% P_{rated}}{3 * 2\pi f * V_{rated}^2} \tag{3}$$

where

$\text{V}_{rated}^2 = 400$ V, $\text{P}_{rated} = 6.6$ kW, $f = 50$ Hz.

The values of L and C are obtained using equations.

4. Control strategy of the proposed inverter

In this proposed approach, a Park transformation control strategy is used to separate the active and reactive component of the overall current. The distortion in the current is minimized by using a PI controller.

The formulations of Park transformation (abc to dqo) are given by the following equations:

Instantaneous active current component I_d is given by

$$I_d = \frac{2}{3} * [I_a \sin(\omega t) + I_b \sin\left(\omega t - \frac{2\pi}{3}\right) + I_c \sin\left(\omega t + \frac{2\pi}{3}\right)] \tag{4}$$

Instantaneous reactive current component I_q is given by

$$I_q = \frac{2}{3}[I_a \cos(\omega t) + I_b cos\left(\omega t - \frac{2\pi}{3}\right) + I_c \cos\left(\omega t + \frac{2\pi}{3}\right)] \tag{5}$$

Zeroth current is given by

$$I_o = \frac{1}{3}[I_a + I_b + I_c] \tag{6}$$

The formulations of the inverse Park transformation (dqo to abc) to convert the filtered current is as below.

Reference voltage V_a is given by

$$V_a = V_d \sin(\omega t) + V_q \cos(\omega t) + V_0 \tag{7}$$

Reference voltage V_b is given by

$$V_b = V_d \sin\left(\omega t - \frac{2\pi}{3}\right) + V_q cos\left(\omega t - \frac{2\pi}{3}\right) + V_0 \tag{8}$$

Reference voltage V_c

$$V_c = V_d \sin\left(\omega t + \frac{2\pi}{3}\right) + V_q cos\left(\omega t + \frac{2\pi}{3}\right) + V_0 \tag{9}$$

where

$I_a = $ Phase a inverter current, $I_c = $ Phase c inverter current,

$I_b = $ Phase b inverter current, $V_q = $ Instantaneous active voltage component,

$V_q = $ Instantaneous reactive voltage component, $V_0 = $ Zeroth voltage component.

4.1. Pulse width modulation technique

The PWM technique comprises a current control strategy, space vector pulse width modulation, reference wave generator, and comparator as shown in Figure 2. The inputs to the current controller are grid voltage, inverter current, reference instantaneous active current component from the DC link capacitor, and the reference instantaneous reactive current component, which is set as zero in this approach [25].
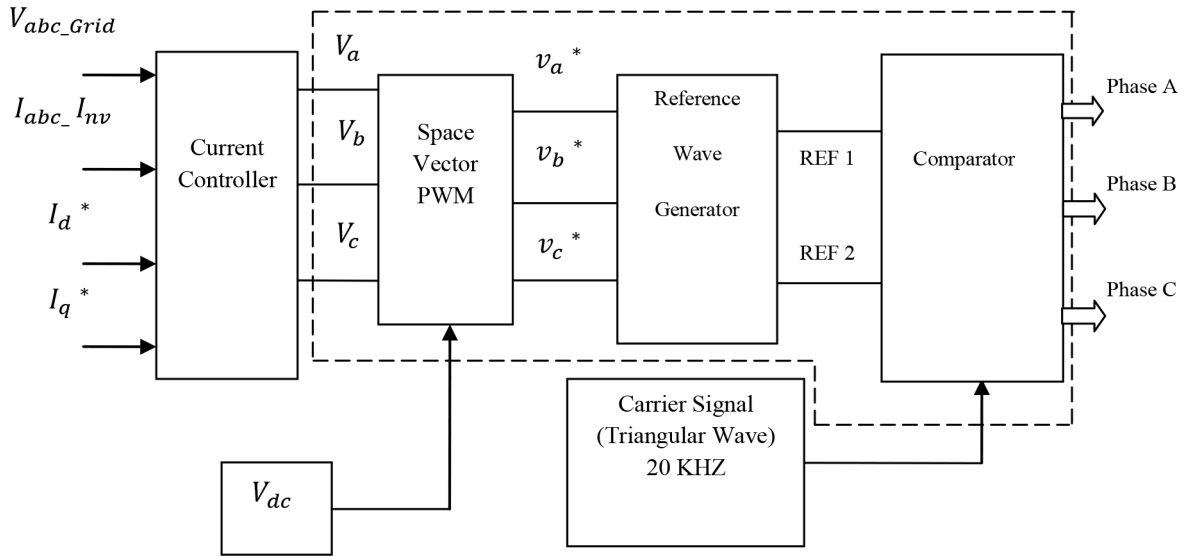
Figure 2. PWM pulse generation.

4.2. PI controller

The reason behind the extensive use of the PI controller is its effectiveness in the control of steady-state error of a control system and also its easy implementation. K_p and K_i are the proportional and integral gains, respectively; these gains depend on the system parameters. Err is the error signal, which is the difference between the instantaneous active current component I_d and reference instantaneous active current component I_d*. Similarly, this error could also represent the difference between the instantaneous reactive current component I_q and reference instantaneous reactive current component I_q*.

$$y(t) = K_p * e(t) + K_i \int_0^t e(t)\, dt \tag{10}$$

In the above equation $y(t)$ represents V_d/V_q, which is clearly shown in Figure 3. The fundamental procedure for tuning the PI controller is to increase the proportional gain until a significant response is achieved. At this point, if the K_i value is tuned, the corresponding steady state error can be eliminated.

5. Space vector pulse width modulation

Space vector PWM comprises six sectors for five switches. Among the five switches, four switches belong to the H-bridge inverter and the other one belongs to the auxiliary inverter. PWM controls the inverter output voltage and minimizes the THD considerably. Moreover, filters such as LC and LCL may not eliminate the lower order harmonics effectively and hence in this paper space vector PWM has been used.
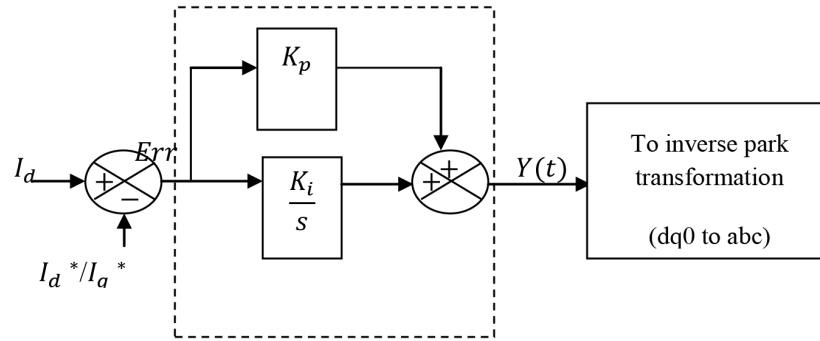
Figure 3. PI controller architecture.

6. Principle of space vector PWM

The working principle of MSVPWM is discussed in this section [26]. MSVPWM takes reference sine as the input from the current controller. From the grid voltage, instantaneous active voltage component (V_d) and instantaneous reactive voltage component (V_q) are separated using Park transformation. The magnitude estimation of V_d and V_q is given by $|V_{ref}|$. Then angle is extracted from the active and the reactive voltage component. The attained angle is compared with the angles such as $\left(-\frac{2\pi}{3}, -\frac{\pi}{3}, 0, +\frac{\pi}{3}, +\frac{2\pi}{3}\right)$ and the appropriate sector for that angle is identified. Now each sector represents $60°$. Then, based on the identified sector, the corresponding switching time vector is assigned as shown in Table 1. Figure 4 shows the basic switching vectors and sectors in MSVPWM. The adjacent vectors in each sector of MSVPWM need to be averaged. Two adjacent vectors and zero vectors are combined to generate the appropriate PWM signals.

Table 1. Switching time vector.

Sector	Switching time vector
1	$S_1 = T_1 + T_2 + (0.5 \times T_0)$ $S_2 = T_2 + (0.5 \times T_0)$ $S_3 = (0.5 \times T_0)$
2	$S_1 = T_1 + (0.5 \times T_0)$ $S_2 = T_1 + T_2 + (0.5 \times T_0)$ $S_3 = (0.5 \times T_0)$
3	$S_1 = (0.5 \times T_0)$ $S_2 = T_1 + T_2 + (0.5 \times T_0)$ $S_3 = T_2 + (0.5 \times T_0)$
4	$S_1 = (0.5 \times T_0)$ $S_2 = T_1 + (0.5 \times T_0)$ $S_3 = T_1 + T_2 + (0.5 \times T_0)$
5	$S_1 = T_2 + (0.5 \times T_0)$ $S_2 = (0.5 \times T_0)$ $S_3 = T_1 + T_2 + (0.5 \times T_0)$
6	$S_1 = T_1 + T_2 + (0.5 \times T_0)$ $S_2 = (0.5 \times T_0)$ $S_3 = T_1 + (0.5 \times T_0)$

6.1. Time duration calculation

The time durations, T_1, T_2, and T_z are clearly depicted in Figure 5. The formulations to determine the time durations are also evaluated.
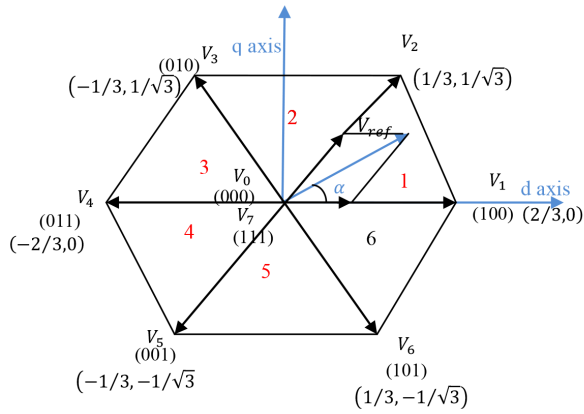
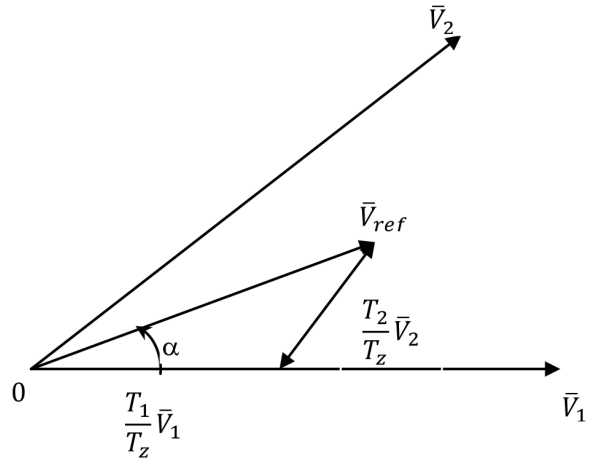**Figure 4.** Basic switching vectors and sectors.

Figure 5. Reference vector as a combination of adjacent vectors at sector.

$$T_1 = k \times \left(sin\left(\frac{\pi}{3} - \theta + \frac{n-1}{3}\pi \right) \right)$$

$$T_2 = k \times \left(sin\left(\theta - \frac{n-1}{3}\pi \right) \right)$$

$$T_0 = T_z - (T_1 + T_2),$$

where modulation index 'k' is defined as

$$k = \frac{\sqrt{3} \times T_z \times V_{ref}}{V_{dc}}$$

$T_z = \frac{1}{f_s}$; f_s = switching frequency.

6.2. Reference wave generator

Figure 2 shows two reference signals, 'REF 1' and 'REF 2', which are compared with the carrier wave at 20 kHz switching frequency. If REF 1 is greater than carrier wave peak amplitude, then REF 2 will be compared with the carrier wave until it crosses zero. Then again REF 1 is compared with the carrier wave until it exceeds the carrier wave. Switches M_1, M_2, and M_3 will be switching at the frequency of 20 kHz, whereas switches M_4 and M_5 will operate at a nominal frequency of 50 Hz. The switching sequences of the three-phase modified inverter are shown in Table 2, wherein '1' represents the 'ON' position and '0' represents the 'OFF' position. The levels of the inverter are decided based on this switching sequence.

7. Results and discussion
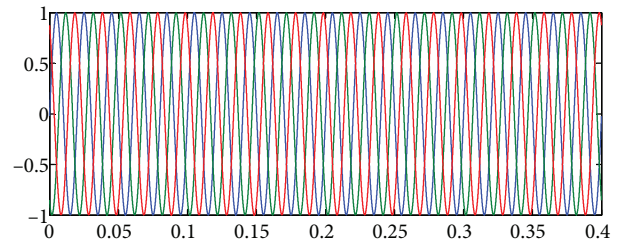
7.1. Simulation results

The MSVPWM-based three-phase inverter with a single DC source for a grid-connected PV system is simulated in MATLAB/Simulink. The simulations are carried out on a 6.6 kW (i.e. 400 V @ 5.5 A) and the PV panel is assumed to be operated at 1000 W/m^2 and implemented using a Spartan 6A FPGA development board. The simulation results are shown in Figures 6–8.
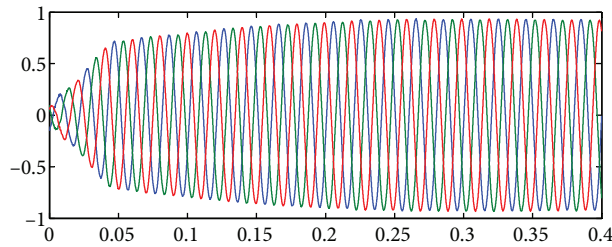
Table 2. Switching sequence.

M1	M2	M3	M4	M5	V_{inv}
1	0	0	0	1	$Va/_2$
0	1	0	0	1	$+V_a$
0 or 1	1 or 0	0 or 1	0 or 1	0 or 1	0
1	0	0	1	0	$-Va/_2$
0	0	1	1	0	$-V_a$
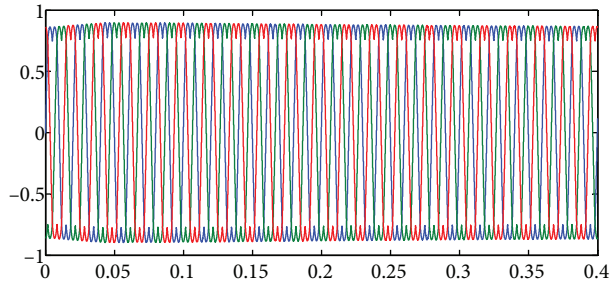
Figure 6. Three-phase space vector waveform.

Figure 7. Three-phase voltage waveform (simulation).

Figure 8. Three-phase current waveform (simulation).

7.2. Experimental results

The laboratory prototype model of the proposed three-phase inverter is implemented using a Xilinx Spartan 6A FPGA development board and the same is tested in the laboratory as shown in Figure 9. The output of the PV panel is connected to the boost converter, which is controlled by the pulses from the FPGA based on the MPPT algorithm developed using the P&O technique. The input for the mathematical modeling using MPPT is obtained by sensing the PV panel voltage and current, which are given as input to the FPGA. The output of the boost converter is maintained constant irrespective of changes in the input. The single input DC source of the boost converter is fed as input to the three-phase inverter. The pulses for the three-phase inverter are obtained by measuring the grid voltage and inverter current, which is given as input for the MSVPWM technique programmed in the FPGA development board. The FPGA generates pulses for the fifteen switches according to the input signals given for computation.

In the experimental setup 37 Tata BP Solar panels of the rating 6.6 kW (37 panels $\times$ 180 W) are used. The DC bus consists of two capacitors of 2600 mu F each; the DC bus voltage is set to 570 V. In the three-phase inverter 5 switches for each phase are used and one switch acts as auxiliary switch while the remaining four
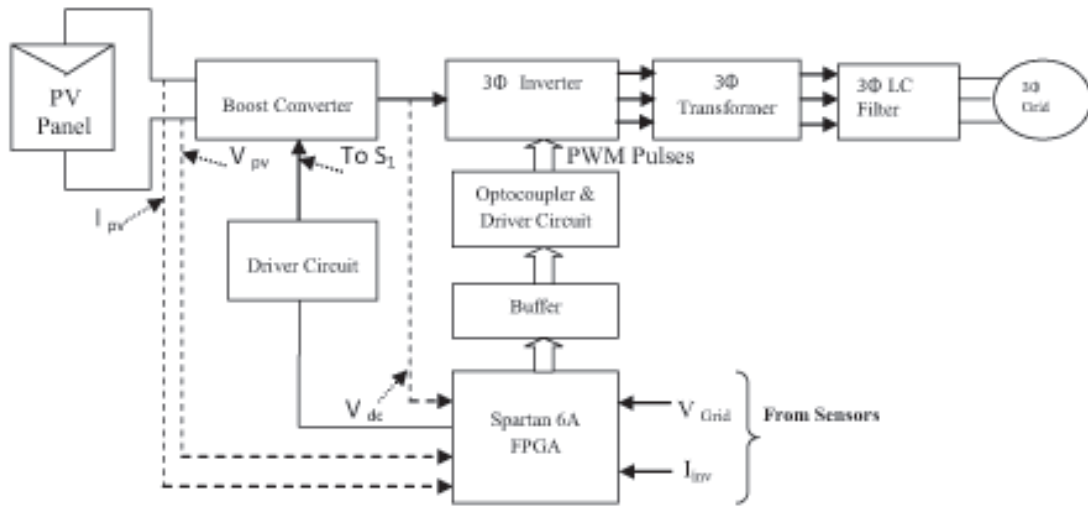
Figure 9. Simplified block diagram of the experimental setup

switches act as a normal H bridge inverter. IGBT SKM50GB12T4 is used for the inverter and four power diodes are used in parallel with the auxiliary switch. The gating pulses of the proposed inverter generated from the FPGA are shown in Figures 10–12. The output of the inverter is given to a three-phase transformer and the filtered sinusoidal voltage and current waveforms are obtained using three-phase LC filters. The filtered three-phase voltage and current are shown in Figures 13 and 14. The THD of the output waveform is 1.7% as shown in Figure 15 and photos of the experimental setup are shown in Figures 16(a) and 16(b). The devices used for the experimental setup are shown in Table 3.
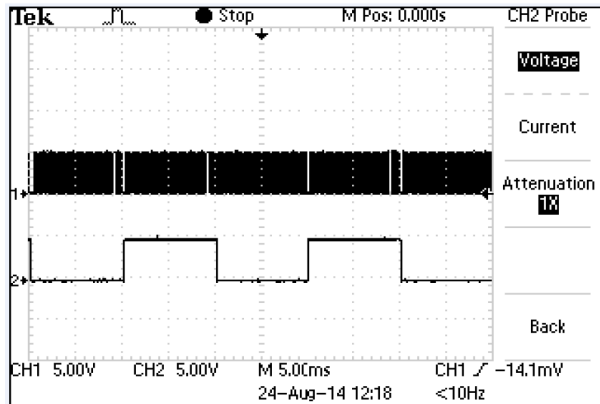

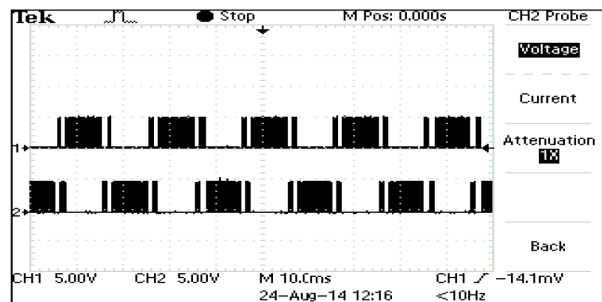**Figure 10.** Switching pulses for M_1 - Upper for Phase A.

Figure 11. Switching pulses for M2 & M3 for Phase A.

7.3. Device comparison

Table 4 shows the comparison of a number of power devices used in the proposed approach with two existing approaches inferred in [11] and [12]. The devices' comparison mainly includes the switches, input source, and transformer. It is observed from Table 4 that the switches used in the proposed approach number 15, whereas the existing approach [11] and [12] use 24 switches for the consideration of five levels.
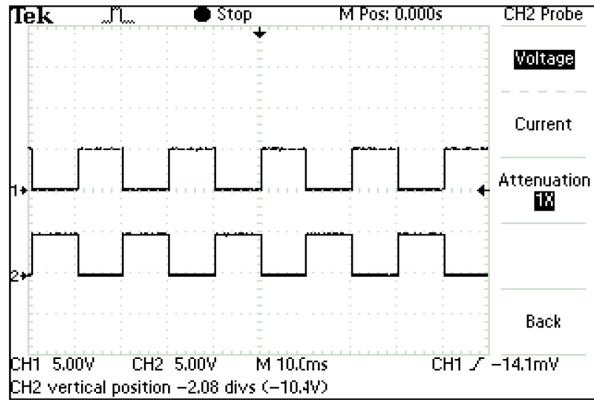
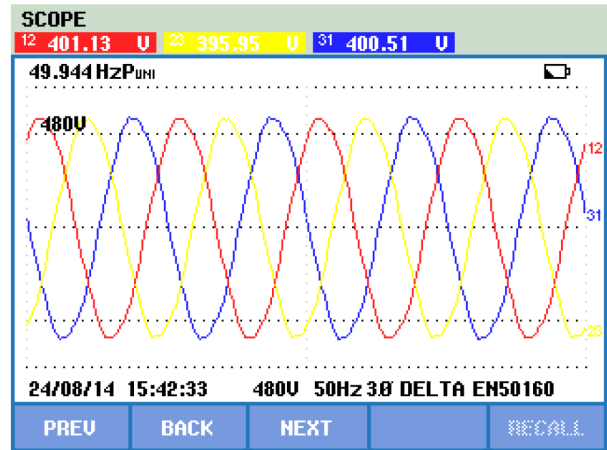**Figure 12.** Switching pulses for M4 & M5 for Phase A.
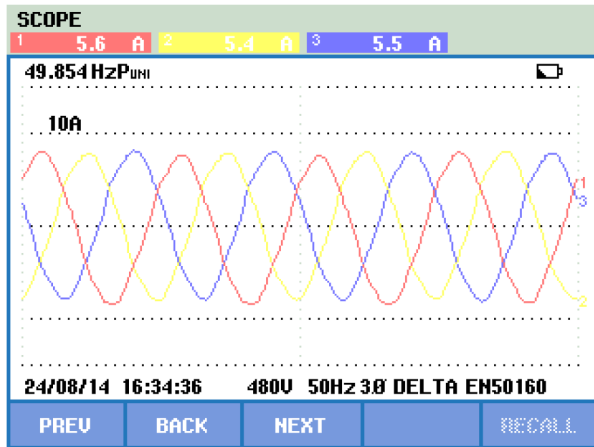

Figure 13. Three-phase voltage (experimental).

Figure 14. Three-phase current (experimental).
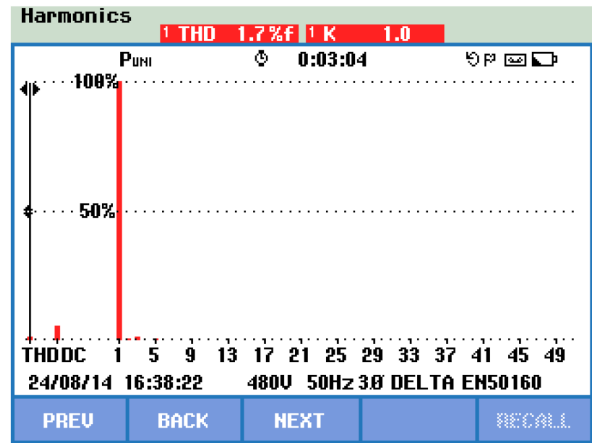

Figure 15. Harmonic profile (experimental).

Figure 16. (a) Photos of experimental setup, (b) solar panel.

Thus, the switching power losses are considerably reduced in the proposed approach. Additionally, the input DC sources used in the existing approach [11] number six, whereas the proposed approach uses only one DC source. Similarly, three transformers were used in the existing work [12], whereas the proposed approach

uses only one transformer. Thus, from Table 4 it is clearly observed that the proposed approach uses fewer devices, which in turn would result in lower complexity and cost. The THD performance of the proposed system is shown in Table 5.

Table 3. Hardware specifications.

IGBT for H- bridge	SKM 50GB12T4
DC bus capacitor	2600 μF, 900 V
Inductor (L)	1.5 mH, 10 A
Capacitor (C)	5 μF, 440 V
Controller	Spartan 6A, (FPGA- 250 MHz ,DSP slices)
Solar panel	37 panels, 180 W
Voltage sensor	LV25_ P
Current sensor	LTS25_ NP
Bidirectional switch	FIO 50_ 12BD

Table 4. Power device utility comparison.

Parameters	Proposed	Existing work [11]	Existing work [12]
Switches	15	24	24
I/P DC source	1	6	1
Transformer	1	-	3

Table 5. THD comparison.

Percentage of THD (simulation)	Percentage of THD (experimental)
1.2%	1.7%

8. Conclusion

In this paper, an efficient modified space vector pulse width modulation control strategy-based three-phase inverter with a single DC source for a grid-connected PV system has been presented. The proposed three-phase inverter system has a minimal number of switches and transformers, and offers minimum THD when compared with the existing system, which in turn minimizes the switching power loss and cost as well as weight. The other major advantage of this system is that the inverter connects with a single DC source with proper voltage balancing. Simulations are carried out in MATLAB/Simulink and a prototype model is also implemented using a Spartan 6A FPGA development board. The comparison of hardware results shows close agreement with simulation results.

Acknowledgment

References

[1] Franquelo LG, Rodriguez J, Leon JI, Kouro S, Portillo R, Prats MAM. The age of multilevel converter arrives. IEEE T Ind Electron 2008; 2: 28-39.

[2] Mariusz M, Gopakumar K, Rodriguez J, Marcelo A, Perez A. Survey on cascade multilevel inverter. IEEE T Ind Electron 2009; 57: 2197-2206.

[3] Carrasco JM, Franquelo LG, Bialasiewicz JT, Galvan E, Portillo Guisado RC, Prats MAM, Leon JI, Moreno AN. Power electronic systems for the grid integration of renewable energy sources: a survey. IEEE T Ind Electron. 2006; 53: 1002-1016.

[4] Kang FF, Park SJ, Eog CS, Kim CU, Ise T. Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems. IEEE T Energy Conver 2005; 20: 906-915.

[5] Kapila B, Tracy S, Janaka E. Photovoltaic applications for off grid electrification using novel multi-level inverter technology with energy storage. Renew Energ 2012; 37: 82-88.

[6] Rodriguez J, Jih-Sheng L, Fang Zheng P. Multilevel inverters: a survey of topologies, controls, and applications. IEEE T Ind Electron 2002; 49: 724-738.

[7] Rashid MH. Power Electronics Circuits, Devices, and Applications. 3rd ed., Upper Saddle River, NJ, USA: Prentice-Hall, 2007.

[8] Colak I, Kabalci E, Ramazan B. Review of multilevel voltage source inverter topologies and control schemes. Energ Convers Manage 2011; 52: 1114-1128.

[9] Alexander SA, Thatan M. Reduction of voltage harmonics in solar photovoltaic fed inverter of single phase stand alone power system. J Sol Energ-T ASME 2014; 136: 44501-44504.

[10] Peng FZ, Lai JS, McKeever JW, VanCoevering J. A multilevel voltage source inverter with separate DC sources for static VAR generation. IEEE T Ind Appl 1996; 32: 1130-1138.

[11] Valan Rajkumar M, Manoharan PS. FPGA based multilevel cascaded inverters with MSVPWM algorithm for photovoltaic system. Sol Energy 2013; 87: 229-245.

[12] Sung GS, Feel SK, Sung JP. Cascade multilevel inverter employing three phase transformer and single DC input. IEEE T Ind Electron 2009; 56: 2005-2014.

[13] Suresh Y, Panda AK. Research on cascade multilevel inverter by employing three phase transformer. IET Power Electronics 2012; 5: 561-570.

[14] Selvaraj J, Rahim N.A. Multilevel inverter for grid-connected PV system employing digital PI controller. IEEE T Ind Electron 2009; 56: 149-158.

[15] Ammasai Gounden N, Sabitha AP, Himaja N, Krithiga S. Fuzzy logic controller with MPPT using line-commutated inverter for three-phase grid-connected photovoltaic systems. Renew Energ 2009; 34: 909-915.

[16] Kazmierkowski MP, Malesani L. Current control techniques for three-phase voltage-source PWM converters: a survey. IEEE T Ind Electron 1998; 45: 691-703.

[17] Esram T, Chapman PL. Comparison of photovoltaic array maximum power point tracking techniques. IEEE Trans. Energ Convers Manage 2007; 22: 439-449.

[18] Jain S, Agarwal V. Comparison of the performance of maximum power point tracking schemes applied to single stage grid-connected photovoltaic systems. IET Electr Power App 2007; 1: 753-762.

[19] Ravi A, Manoharan PS, Vijay Anand J. Modelling and simulation of three phase multilevel inverter for grid connected photovoltaic systems. Sol Energy 2011; 85: 2811-2818.

[20] Sridhar R, Jayasankar KC Dash SS, Avasthy V. A single stage photovoltaic inverter with common power factor control and maximum power point tracking circuit. J Sol Energ-T ASME 2014; 136: 210201- 210207.

[21] Lun SX, Du CJ, Yang GH, Wang S, Guo TT, Sang JS, Li JP. An explicit approximate I–V characteristic model of a solar cell based on padé approximants. Sol Energy 2013; 92: 147-159.

[22] Kaliamoorthy M, Rajasekaran V, Gerald Christopher Raj I. Single phase fifteen level grid connected inverter for photovoltaic system with evolutionary programming based MPPT algorithms. Sol Energy 2014; 105: 314-329.

[23] Agelidis VG, Baker DM, Lawrance WB, Nayar CV. A multilevel PWM inverter topology for photovoltaic applications. In: IEEE 1997 IEEE International Symposium on Industrial Electronics; 7–11 July 1997; 02: Guimaraes: pp. 589-594.

[24] Rahim NA, Jeyraj S. Multistring five-level inverter with novel PWM control scheme for PV application. IEEE T Ind Electron 2010; 57: 2111-2123.

[25] Vander Broeck HW. Analysis of the harmonics in voltage fed inverter drives caused by PWM schemes with discontinuous switching operation. Proc. EPE Annual Meeting; 1991; Italy, pp. 261-266.

[26] Zhang Y, Wang S, Xia H, Ge J. A Novel MSVPWM Modulation Scheme. In: IEEE 2009 Applied Power Electronics Conference and Exposition; 15–19 June 2009; Washington, pp. 128-131.