Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2016) 24: 3838 – 3851
© TÜBİTAK
doi:10.3906/elk-1412-32

Comparative analysis of voltage and current source inverter based DSTATCOM systems

Pradeep KUMAR*, Niranjan KUMAR, Ashok Kumar AKELLA
Electrical and Electronics Engineering Department, National Institute of Technology Jamshedpur, Jamshedpur, Jharkhand, India

Received: 06.12.2014 • **Accepted/Published Online:** 11.06.2015 • **Final Version:** 20.06.2016

Abstract: This paper presents a comparative performance evaluation of voltage source inverter (VSI) as well as current source inverter (CSI) based DSTATCOM systems in terms of power quality improvement in a three-phase four-wire distribution network. Due to increasing use of high-performance semiconductor based power electronic switches, the CSI based DSTATCOM is developed as a suitable option in high power applications. However, the VSI based DSTATCOM system is the best suited for medium power applications. The VSI based DSTATCOM offers advantages over the CSI based DSTATCOM in terms of current harmonic compensation, power factor correction, lower losses (both conduction and power losses), and simplicity in both power and control circuits. The control strategies of both the DSTATCOM systems are based on conventional PI and synchronous reference frame (SRF) theory. The performance of the VSI and CSI based DSTATCOM systems is tested under unbalanced and nonlinear load conditions. Analytical expectations of complete DSTATCOM systems are verified using simulations in the MATLAB/Simulink environment.

Key words: Distribution static compensator (DSTATCOM), conventional PI (CPI) controller, synchronous reference frame (SRF) controller, power quality (PQ), total harmonic distortion (THD)

1. Introduction

Recently, three-phase four-wire distribution systems are facing problems from load reactive power burden and poor power quality such as current and voltage harmonics, low power factor, load unbalanced, and excessive neutral current, which are mentioned in the literature [1–7]. The adverse effects of poor power quality may result in insulation failure, overheating of transformers, nuisance tripping of circuit breakers, malfunctioning of UPS systems and generator systems, computer malfunctions, overvoltage problems, and premature failure of electronic equipment. At present, there are many schemes that have been developed to solve the problems related to power quality issues in three-phase four-wire systems [1,2,5–7]. In the analysis presented in [8], a capacitor supported DSTATCOM in a three-phase four-wire distribution system under nonideal supply voltage conditions has been implemented for harmonic current compensation. The reduced total harmonic distortion (THD) level of supply current is not too low in [8].

To overcome the above problem, a three-leg voltage and current source inverter (CSI) based DSTATCOM under sinusoidal voltage has been demonstrated to achieve much harmonic reduction in supply current. However, the voltage source inverter (VSI) based DSTATCOM gives a greater harmonic reduction as compared to the CSI based DSTATCOM. Various control techniques have been reported to derive the reference control signals for

*Correspondence: kumarcs08@gmail.com

the DSTATCOM. To control the DSTATCOM for a three-phase four-wire distribution system, instantaneous reactive power theory (IRPT), power balance theory (PBT), synchronous reference frame theory (SRFT) [9–13], Lyapunov-function-based control [14], nonlinear control [15], and feed forward training [16] have been proposed. However, SRFT is one of the best options due to reduced computation time and easy availability of input parameters such as load current, dc voltage, and PCC voltage.

Hence, in this paper, a control approach based on SRFT is proposed under sinusoidal supply condition. Moreover, the conventional PI control [17] approach has also been selected to investigate superior features of the proposed synchronous reference frame approach in terms of power quality improvement. The organization of the present paper is as follows. In section 2, the configuration of the three-phase DSTATCOM system based on both VSI and CSI based topologies is presented. Control strategies for both DSTATCOM systems are described in section 3. Section 4 represents the design of various parameters of the DSTATCOM. Simulation results with a discussion of the CSI and VSI based DSTATCOM systems are represented in section 5. Finally, section 6 concludes the paper.

2. Configuration of the DSTATCOM system

The DSTATCOM is installed in parallel to sensitive loads. Figure 1 shows how the DSTATCOM connects to the power system and depicts its structure. The DSTATCOM system consists of an inverter (Figures 2a and 2b), an energy storage device (i.e. dc inductor or dc capacitor), and a shunt connected transformer used to couple the inverter with the distribution line and control circuit. The function of the inverter is to convert the dc voltage developed in the energy storage device into three-phase AC voltage.

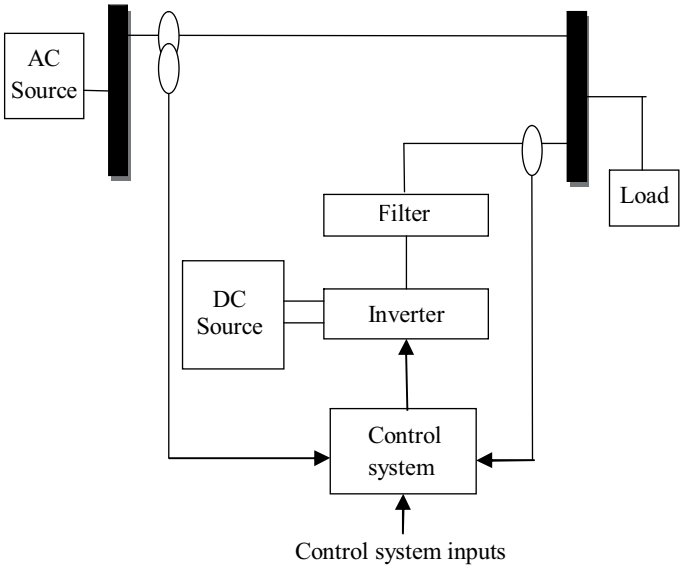

Figure 1. DSTATCOM with power system.

The flow of active and reactive power between the power system and DSTATCOM depends on controlling the phase angle difference between power system voltage and DSTATCOM voltage. If DSTATCOM voltage V_D is in phase with power system voltage V_P and V_D is greater than V_P, DSTATCOM delivers reactive power to the power system and if V_D is smaller than V_P, DSTATCOM absorbs reactive power from the power system. Actually V_P and V_D have some phase difference to reduce losses in transformer winding; hence, DSTATCOM absorbs some active power from the power system.

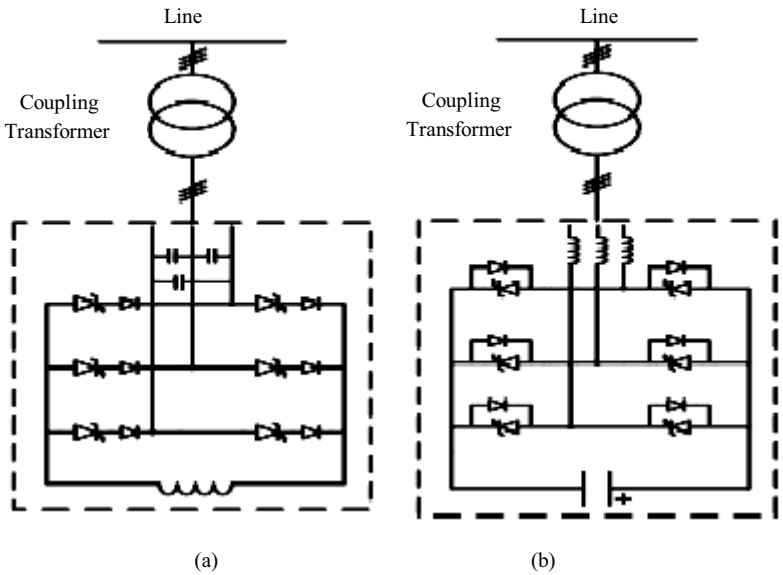

Figure 2. Inverters (a) Current source and (b) Voltage source.

3. Control strategies

3.1. Conventional PI controller

On comparing the reference voltage (set voltage) with the terminal voltage, an error signal is obtained. This signal is passed to a PI controller. The PI controller generates an angle δ. Angle δ should be such that the error signal for the PI controller tends to zero, i.e. the load rms voltage is brought near the reference voltage. Figure 3 represents a conventional PI controller that generates angle δ.

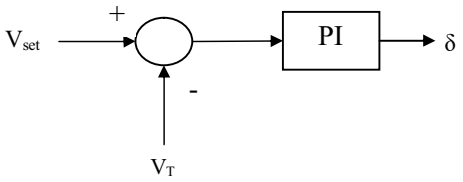

Figure 3. Conventional PI controller.

From the angle δ, three-phase sinusoidal signal $V_{control}$ is obtained as below:

$$\begin{aligned} V_A &= Sin(\omega t + \delta) \\ V_B &= Sin(\omega t + \delta - 2\pi/3) \\ V_C &= Sin(\omega t + \delta + 2\pi/3) \end{aligned} \tag{1}$$

Three-phase voltage signals V_A, V_B, and V_C are shifted by 0°, 120°, and 240°, respectively. Figure 4 represents phase modulation of control angle δ.

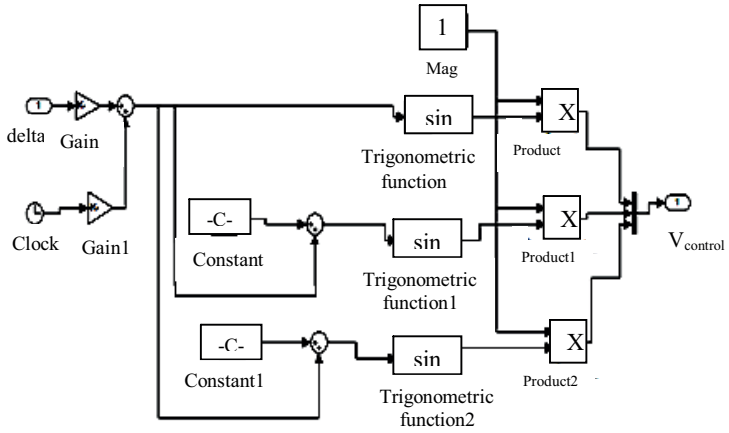

Figure 4. Phase modulation of the control angle δ.

Sinusoidal signal $V_{control}$ is fed to the PWM signal generator in order to generate switching pulses for IGBT switches of the inverter valves. Figure 5 shows the Simulink model of the DSTATCOM controller. The speed of performance and robustness of this control scheme are clearly shown in the simulation results.

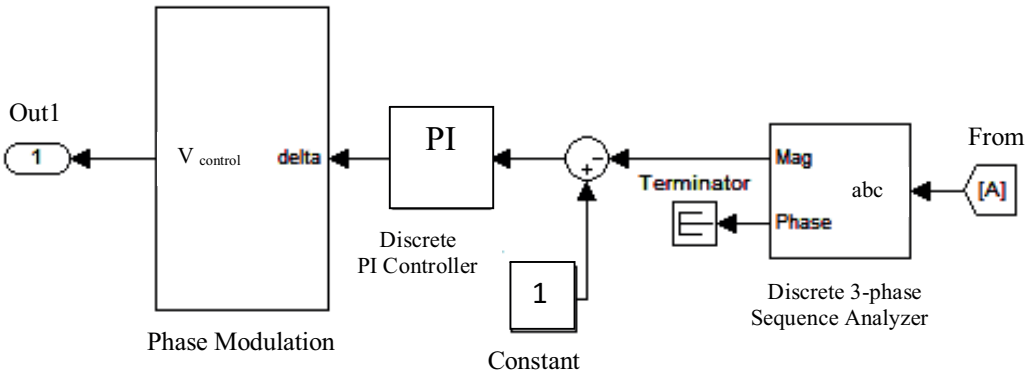

Figure 5. Simulink model of DSTATCOM controller.

3.2. Synchronous reference frame controller

Figure 6 shows a pictorial view of a synchronous reference frame controller. The three-phase load currents in the a–b–c frame are converted into the $\alpha-\beta$ frame and after that from the $\alpha-\beta$ frame into the d–q frame. From the above two transformations, it is possible to derive a third transformation, i.e. a–b–c to d–q transformation, as follows:

$$\begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix} = {}^{2}/_{3} \begin{Bmatrix} 1 & -{}^{1}/_{2} & -{}^{1}/_{2} \\ 0 & -{}^{\sqrt{3}}/_{2} & {}^{\sqrt{3}}/_{2} \end{Bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad \begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \begin{Bmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{Bmatrix} \begin{bmatrix} i_{L\alpha} \\ i_{L\beta} \end{bmatrix}$$

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = {}^{2}/_{3} \begin{Bmatrix} \cos\omega t & \cos\left(\omega t - {}^{2\pi}/_{3}\right) & \cos\left(\omega t + {}^{2\pi}/_{3}\right) \\ \sin\omega t & \sin\left(\omega t - {}^{2\pi}/_{3}\right) & \sin\left(\omega t + {}^{2\pi}/_{3}\right) \end{Bmatrix} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix}$$

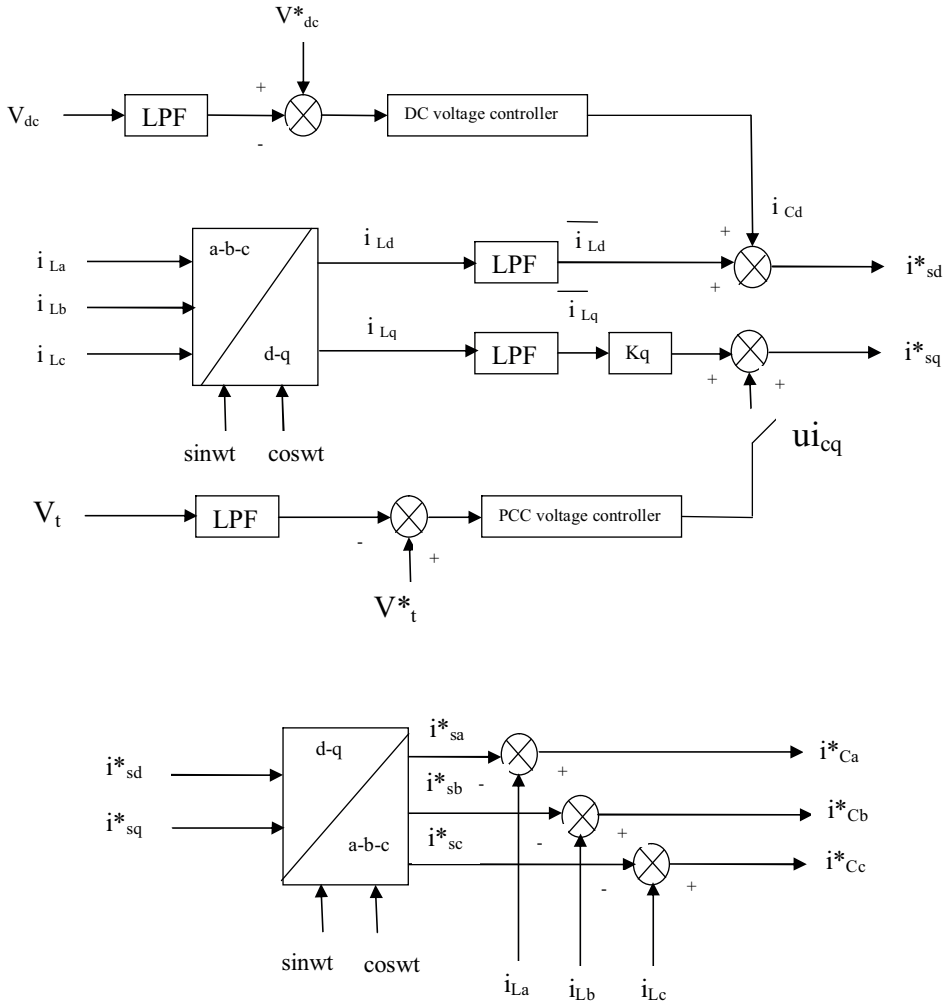

Figure 6. Diagrammatically view of synchronous reference frame.

$$K_q = {Q_s^*}/{\overline{Q_L}} \tag{2}$$

When power factor is to be controlled, K_q is determined as below

$$\bar{Q}_L = |V_t|\,\bar{i}_{Lq} \tag{3}$$

For unity power factor, $\cos\varphi = 1, so\ \varphi = 0 \quad Q_S^* = VI\sin\varphi = 0 \quad K_q = 0$

The reference values of source currents in the d–q frame are as follows:

$$i_{Sd}^* = \overline{i_{Ld}} + i_{Cd}$$

$$i_{Sq}^* = K_q\overline{i_{Lq}} + ui_{Cq} \tag{4}$$

The reference for the source current in the d–q frame are first converted to the $\alpha - \beta$ frame and then to the a–b–c frame using the following formulation:

$$\begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} = \begin{Bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{Bmatrix} \begin{bmatrix} i^*_{sd} \\ i^*_{sq} \end{bmatrix} \quad \begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = 2/3 \begin{Bmatrix} 1 & 0 \\ -1/2 & -\sqrt{3}/2 \\ -1/2 & \sqrt{3}/2 \end{Bmatrix} \begin{bmatrix} i^*_{s\alpha} \\ i^*_{s\beta} \end{bmatrix} \quad \begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix}$$

$$= 2/3 \begin{Bmatrix} \cos\omega t & \sin\omega t \\ \cos\left(\omega t - 2\pi/3\right) & \sin\left(\omega t - 2\pi/3\right) \\ \cos\left(\omega t + 2\pi/3\right) & \sin\left(\omega t + 2\pi/3\right) \end{Bmatrix} \begin{bmatrix} i^*_{sd} \\ i^*_{sq} \end{bmatrix}$$

The desired compensator currents (i^*_{Ca}, i^*_{Cb}, i^*_{Cc}) are obtained as

$$i^*_{Ca} = i_{La} - i^*_{Sa}$$

$$i^*_{Cb} = i_{Lb} - i^*_{Sb}$$

$$i^*_{Cc} = i_{Lc} - i^*_{Sc}$$

4. Design methodology of the DSTATCOM

To demonstrate the performance analysis of the DSTATCOM in terms of power quality improvement a case study has been considered for the three-phase four-wire distribution system under an unbalanced and nonlinear load condition [18]. Various parameters of the DSTATCOM such as dc link voltage, dc capacitor, ac inductors, dc inductor, coupling transformer, and controller gains are calculated as follows [19]:

(i) DC link voltage:

The DC link voltage (V_{dc}) is based on instantaneous energy available at the DSTATCOM. For a three-phase voltage source inverter, DC link voltage is calculated as

$$V_{dc} = 2\sqrt{2}V_{LL}/(\sqrt{3}m) \tag{5}$$

Here m is the modulation index and its value is taken as 1, and V_{LL} is the line to line output ac voltage for DSTATCOM. Hence, the calculated value of V_{dc} is 326.60 V for V_{LL} of 200 V and is selected as 400 V.

(ii) DC capacitor:

The energy conservation principle is applied as

$$(1/2)C_{dc}[V^2_{dc} - V^2_{dc1}] = 3V(aI)t, \tag{6}$$

where V_{dc} is the dc voltage and V_{dc1} is the minimum voltage level of the dc bus, a is the overloading factor, V is the phase voltage, I is the phase current, and t is time by which the dc bus voltage is to be recovered.

Considering 2% voltage ripple in the dc bus, the minimum voltage level of the dc bus, V_{dc1} = 392 V, and V_{dc}= 400 V, V = 239.60 V, I = 18.92 A, t = 750 μs, a = 1.2, the calculated value of C_{dc} is 3863.55 μF and it is selected as 4000 μF.

(iii) AC inductor:

On the inverter's ac side, the interfacing inductors (AC inductors) L_f are used to filter high-frequency components of compensating currents. By taking switching frequency (f_s) = 10 kHz, modulation index (m) = 1, dc voltage (V_{dc}) of 400 V, overload factor, a = 1.2, the L_f value of DSTATCOM is determined as

$$L_f = {}^{mVdc}/_{4af_s i_{cr(p-p)}} \tag{7}$$

By considering 7% ripple in the inductor current, and the current ripple, $i_{cr(p-p)}$ = 0.07 × 18.92 × 240/200 = 1.589 A, the calculated value of L_f is 5.24 mH and it is selected as 5.0 mH.

(iv) DC inductor:

The energy conservation principle is applied as

$$({}^1/_2)L_{dc}[I_{dc}^2 - I_{dc1}^2] = 3V(aI)t, \tag{8}$$

where I_{dc} is the dc current and I_{dc1} is the minimum current level at the dc bus, a is the overloading factor, V is the phase voltage, I is the phase current, and t is time by which the dc bus voltage is to be recovered. By selecting appropriate values of I_{dc} and I_{dc1}, the value of L_{dc} can be calculated and its value is 1 mH.

(v) Coupling transformer:

Two-winding transformers of rating 5 kVA, 240 V/200 V are selected. The selection of coupling transformer parameters has a large impact on the performance of the STATCOM. It plays an important role in the value of voltage regulation and power compensation that the STATCOM can provide.

(vi) Controller gain calculation:

The proportional and integral gains of the controllers are calculated from the Ziegler–Nichols step response method [20]. The gains of the controller are calculated using the following equations:

$$K_p = 1.2U/(GT) \tag{9}$$

$$K_i = 0.6U/(GT^2), \tag{10}$$

where U is the amplitude of a step input, G is the maximum gradient, and T is the point at which the line of maximum gradient crosses the time axis.

DC voltage P controller: K_{p1} = 0.6

PCC voltage PI controller: K_{p2} = 0.2, K_i = 6.5

5. Results and analysis

Verification of both DSTATCOM topologies, VSI-DSTATCOM and CSI-DSTATCOM based on the proposed SRF and conventional PI controller, has been carried out with the help of the power system simulation package MATLAB/Simulink. Simulations are performed in discrete mode with ode 45 (Dormand–Prince) solvers. The total simulation period is 1 s. A three-phase unbalanced R–L load, having different value of resistances and inductances, and nonlinear load as a three-phase diode bridge rectifier is connected to the feeder.

The simulation results for both the VSI and CSI based DSTATCOM topologies are presented in this section for better understanding of and comparative analysis between the two topologies. The main purpose of the simulation is to study two different performances of control aspects for both the VSI and CSI based DSTATCOM topologies: 1) harmonic compensation and power factor correction by conventional PI control; 2) harmonic compensation and power factor correction by synchronous reference frame control. The THD of the source current is measured under the condition of without DSTATCOM and with DSTATCOM by considering conventional PI and synchronous reference frame control strategies. The THD measurements are compared for conventional PI and synchronous reference frame control under both topologies as presented in Table 1.

Table 1. Measured THD for VSI and CSI based DSTATCOM under different control strategies.

Control strategy	VSI based DSTATCOM		CSI based DSTATCOM	
	Without DSTATCOM (%)	With DSTATCOM (%)	Without DSTATCOM (%)	With DSTATCOM (%)
Conventional PI	8.11	0.08	8.11	1.81
Synchronous reference frame	8.11	0.06	8.11	1.68

A. Harmonic compensation and power factor correction by conventional PI control

In this section, the behaviors of the VSI and CSI based DSTATCOM systems in response to harmonic compensation and power factor correction are illustrated. Since VSI and CSI are dual topologies, the characteristic of current in CSI is analogous to that of voltage in VSI and vice versa. The performance indices are dc voltage (V_{dc}), dc current (I_{dc}), source current (i_{Sa}), terminal voltage (V_{ta}), and THD. Figures 7a and 7b illustrate the voltage and current waveform on the dc side of the inverter for the VSI and CSI based DSTATCOM, respectively. In Figures 8a and 8b power factor is improved to unity by both VSI and CSI based DSTATCOM systems at the PCC. From Figures 8a and 8b it is seen that the VSI based DSTATCOM gives better power factor improvement as compared to the CSI based DSTATCOM.

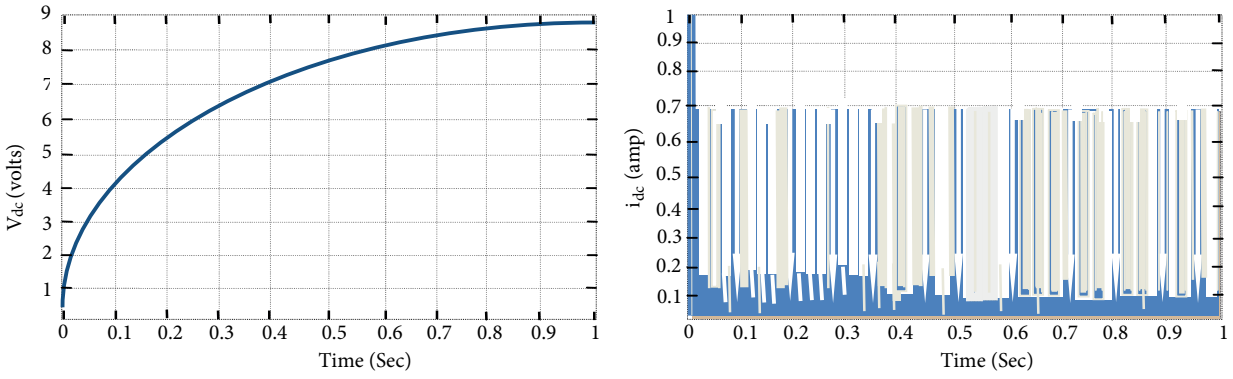

Figure 7. Voltage and current waveform on DC-side (a) DC voltage for VSI (b) DC current for CSI.

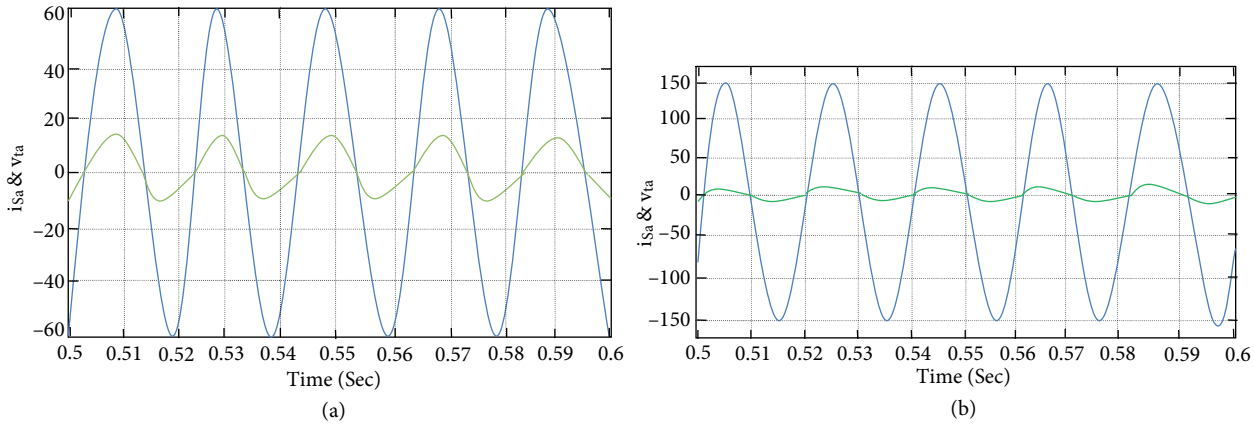

Figure 8. Power factor correction of (a) VSI based DSTATCOM (b) CSI based DSTATCOM.

Figures 9a and 9b show that the THD of the source current before compensation is 8.11%. After compensation the source current THD is significantly reduced to 0.08% by the VSI based DSTATCOM and 1.81% by the CSI based DSTATCOM.

From the FFT analysis of the DSTATCOM, it has been observed that the THD value of the source current is below 5% for both the VSI as well as the CSI based DSTATCOM topologies, which fall under the criteria of IEEE-519 standards for harmonic analysis [3,21]. From Figures 9a and 9b it has been also found that the VSI based DSTATCOM gives lower THD as compared to the CSI based DSTATCOM. This indicates better performance in terms of harmonic compensation in the VSI based DSTATCOM.

B. Harmonic compensation and power factor correction by synchronous reference frame control

The dynamic performance of the VSI and CSI based DSTATCOM in a three-phase four-wire system for the compensation of harmonics and power factor correction by synchronous reference frame control has been explained. The waveforms of the dc voltage (V_{dc}), dc current (I_{dc}), source current (i_{Sa}), and terminal voltage (V_{ta}) are presented to demonstrate the filtering performance of the DSTATCOM. Figures 10a and 10b illustrate the voltage and current waveform on the dc side of the inverter for the VSI and CSI based DSTATCOM, respectively.

It is observed from Figures 11a and 11b that the waveforms of source current (i_{Sa}) and terminal voltage (V_{ta}) are in the same phase; hence power factor correction (unity power factor) occurs by both VSI and CSI based DSTATCOM topologies. Moreover, the VSI based DSTATCOM gives better power factor correction in comparison with the CSI based DSTATCOM.

Figures 12a and 12b show the harmonic spectrum of the source current without and with the DSTACOM for both the VSI and CSI based DSTATCOM topologies. It is observed that the THD of the source current is reduced from 8.11% without the DSTATCOM to 0.06% with the DSTATCOM for the VSI based DSTATCOM and from 8.11% without the DSTATCOM to 1.68% with the DSTATCOM for the CSI based DSTATCOM. Hence the VSI based DSTATCOM is a more suitable approach for harmonic compensation as compared to the CSI based DSTATCOM.

Table 1 shows comparative values of THD measurements of the source current for the VSI and CSI based DSTATCOM topologies. It is clear that before compensation the measured THD of the source current is fixed, i.e. 8.11%, but when the DSTATCOM is in operation with the distribution system, the THD of the source

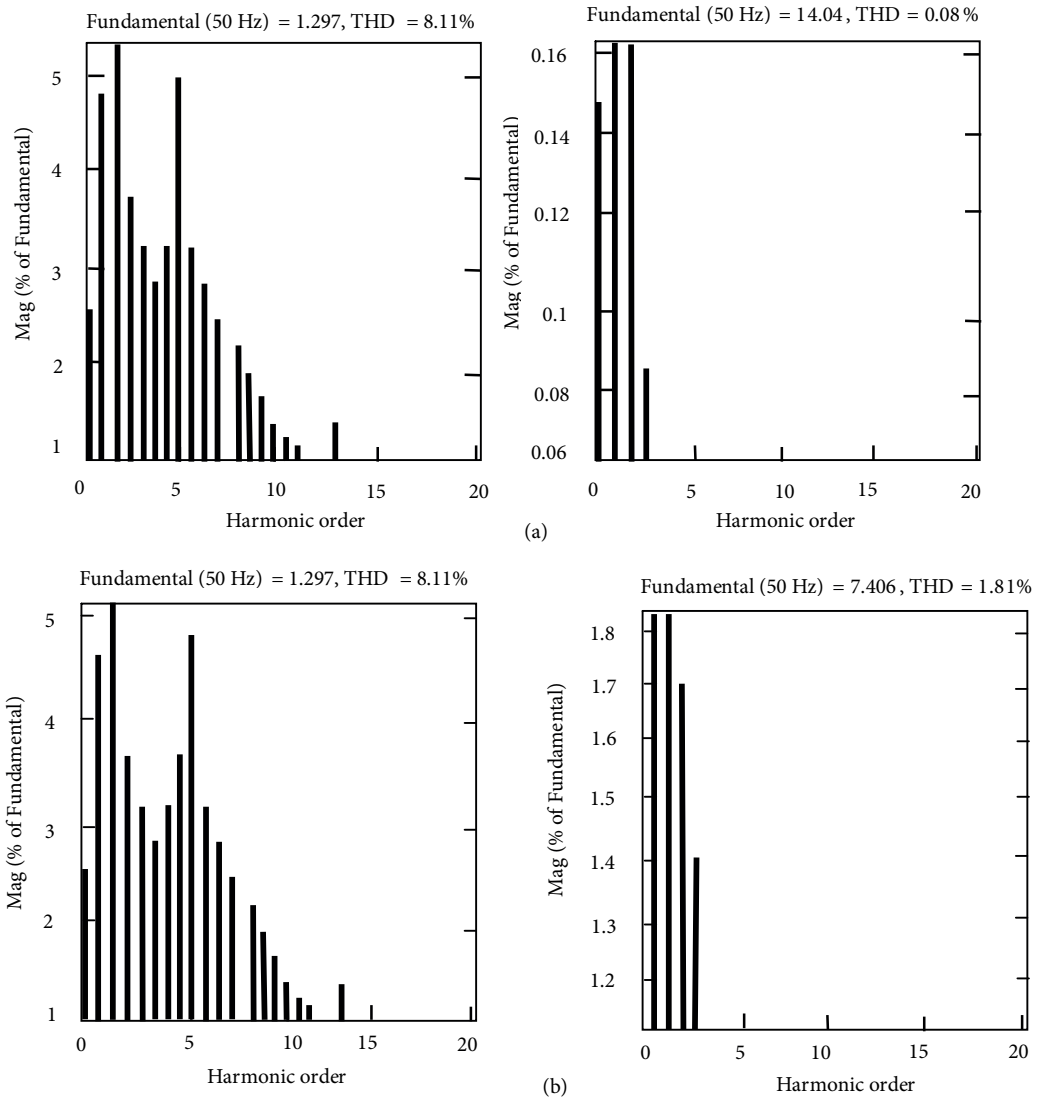

Figure 9. THD for source current spectrum of (a) VSI based DSTATCOM (b) CSI based DSTATCOM.

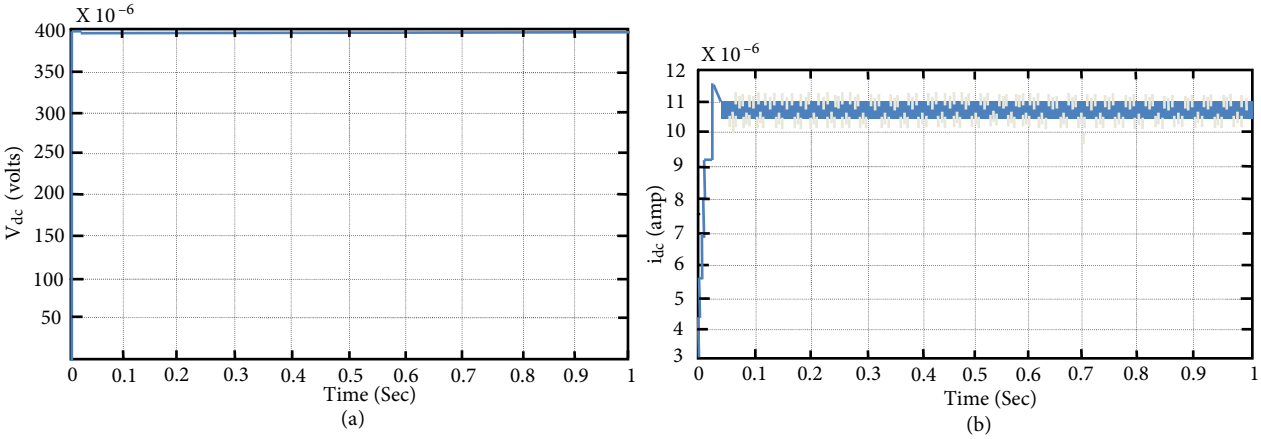

Figure 10. Voltage and current waveform on DC-side (a) DC voltage for VSI (b) DC current for CSI.

current is 0.08% for the case of conventional PI control (CPIC) and 0.06% for the case of synchronous reference frame control (SRFC) in the VSI based DSTATCOM topology but in the CSI based DSTATCOM topology the THD of the source current is 1.81% for the case of conventional PI control (CPIC) and 1.68% for the case of synchronous reference frame control (SRFC).

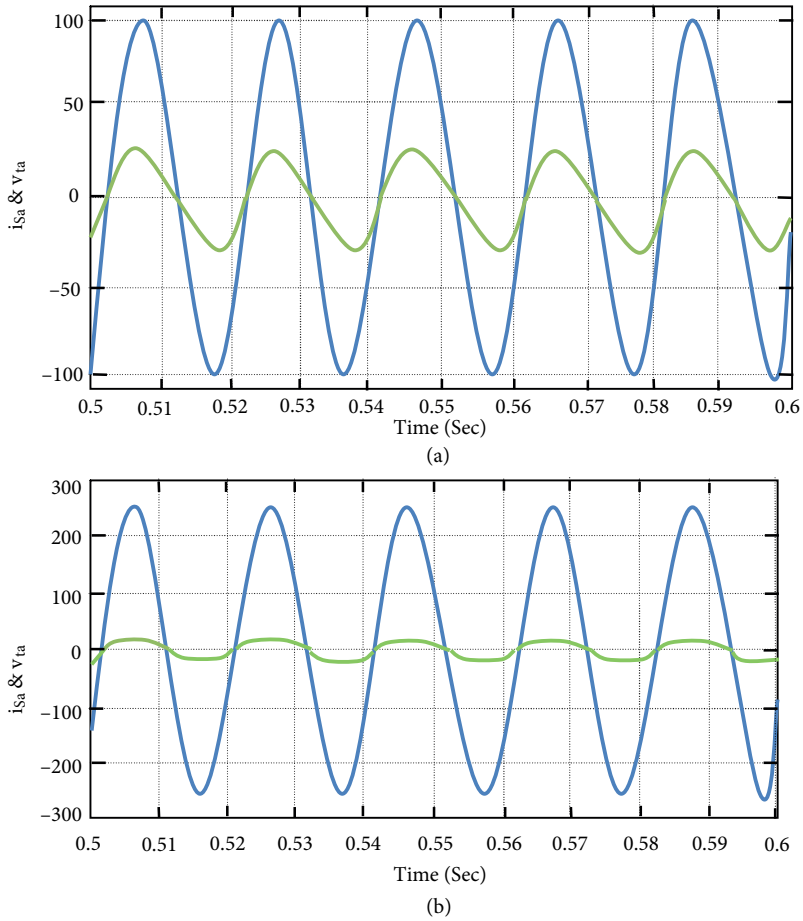

Figure 11. Power factor correction of (a) VSI based DSTATCOM (b) CSI based DSTATCOM.

Figure 13 shows a chartable representation of THD for conventional PI and synchronous reference frame control under both the VSI and CSI based DSTATCOM topology.

Table 2 gives a comparative summary of performance parameters for the VSI and CSI based DSTATCOM.

Table 2. Comparison of performance parameters for VSI and CSI based DSTATCOM.

Performance parameter	VSI based DSTATCOM	CSI based DSTATCOM
Power and control circuits Conduction losses Energy-storage element Power loss Efficiency Inrush current limiting	Simple Low DC capacitor Small Higher Inrush current limiting is required.	Complex High DC inductor Large Lower Inrush current limiting is not required.
Total harmonic distortion (THD) Power factor correction	Low (Excellent) Excellent	Comparatively high (Good) Good

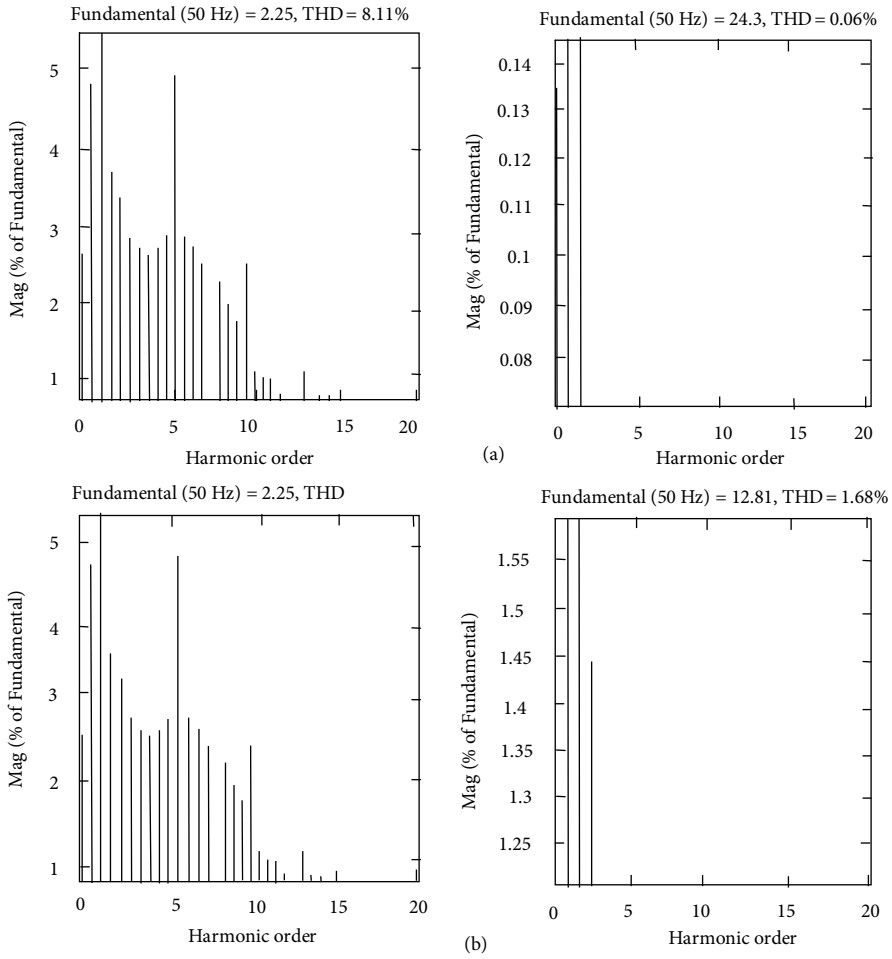

Figure 12. THD for source current spectrum of (a) VSI based DSTATCOM (b) CSI based DSTATCOM.

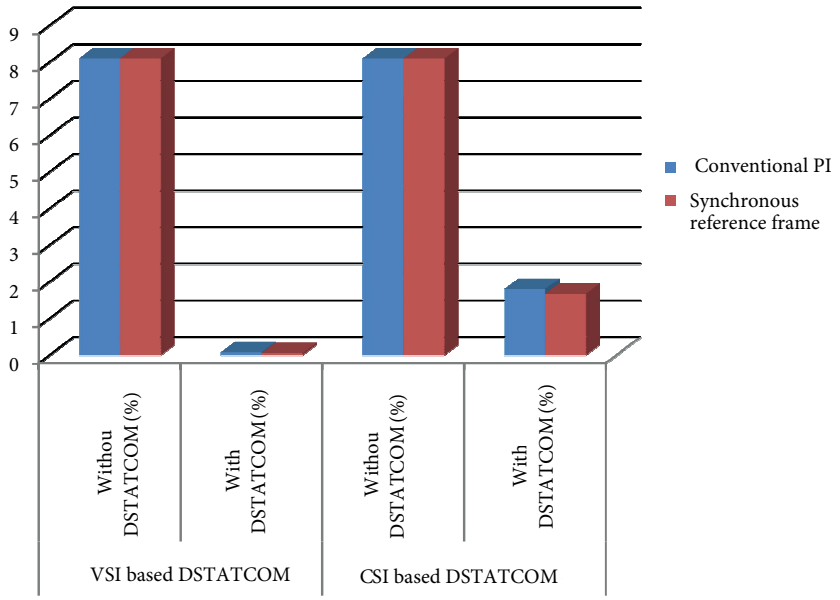

Figure 13. Chart for measured THD of source current on VSI and CSI based DSTATCOM topology.

6. Conclusion

In this paper two different topologies of DSTATCOM named VSI-DSTATCOM and CSI-DSTATCOM have been chosen for extraction of power quality disturbances in the three-phase four-wire distribution network under conventional PI and synchronous reference frame control strategies. The VSI based DSTATCOM topology is compared with the CSI based DSTATCOM topology in terms of current harmonic mitigation, power factor correction, overall cost, losses, efficiency, etc. It is observed that the VSI based DSTATCOM provided better compensation by reducing the THD of the source current than the CSI based DSTATCOM. The measured THD of the source current has successfully fulfilled for the criteria of harmonic standard as mentioned in IEEE 519.

Acknowledgment

The authors gratefully acknowledge the support provided by the National Institute of Technology, Jamshedpur, India.

References

[1] Dugan RC, McGranaghan MF, Beaty HW. Electrical Power Systems Quality. New York, NY, USA: McGraw-Hill, 1996.

[2] Sankaran C. Power Quality. Boca Raton, FL, USA: CRC Press, 2002.

[3] IEEE Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems (Standards and Reports). IEEE Standard 519; 1993; pp. 1-112.

[4] IEEE Standard for Interconnecting Distributed Resources with Electric Power Systems (Standards and Reports). IEEE Standard 1547; 2003; pp. 1-28.

[5] Hingorani NG, Gyugyi L. Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems. New York, NY, USA: IEEE Press, 2000.

[6] Sood VK. HVDC and FACTS Controllers-Applications of Static Converters in Power Systems. Boston, MA, USA: Kluwer, 2004.

[7] Ghosh A, Ledwich G. Power Quality Enhancement Using Custom Power Devices. Boston, MA, USA: Kluwer, 2002.

[8] Singh B, Jayaprakash P, Kothari DP. New control approach for capacitor supported DSTATCOM in three-phase four wire distribution system under non-ideal supply voltage conditions based on synchronous reference frame theory. Int J Elec Power 2011; 33: 1109-1117.

[9] Benhabib MC, Saadate S. New control approach for four-wire active power filter based on the use of synchronous reference frame. Electr Pow Syst Res 2005; 73: 353-362.

[10] de Morais AS, Barbi I. A Control Strategy for Four-Wire Shunt Active Filters Using Instantaneous Active and Reactive Current Method. In: Proc of 32nd Annual Conference on IEEE Industrial Electronics; 7–10 Nov 2006; Paris, France: IEEE. pp. 1846-1851.

[11] Milanés MI, Cadaval ER, González FB. Comparison of control strategies for shunt active power filters in three-phase four-wire systems. IEEE T Power Electr 2007; 22: 229-236.

[12] Zhou J, Wu XJ, Geng YW, Dai P. Simulation research on a SVPWM control algorithm for a four-leg active power filter. J China Univ Min Technol 2007; 17: 590-594.

[13] Fugita H, Akagi H. Voltage-regulation performance of a shunt active filter intended for installation on a power distribution system. IEEE T Power Electr 2007; 22: 1046-1053.

[14] Rahmani S, Hamadi A, Al-Haddad K. A Lyapunov-function-based control for a three-phase shunt hybrid active filter. IEEE T Ind Electron 2012; 59: 1418-1429.

[15] Rahmani S, Mendalek N, Al-Haddad K. Experimental design of a nonlinear control technique for three-phase shunt active power filter. IEEE T Ind Electron 2010; 57: 3364-3375.

[16] Jing X, Cheng L. An optimal-PID control algorithm for training feed-forward neural networks. IEEE T Ind Electron 2013; 60: 2273-2283.

[17] Kumar SVR, Nagaraju SS. Simulation of D-STATCOM and DVR in power systems. ARPN J Eng Appl Sci 2007; 2: 7-13.

[18] Padiyar KR. FACTS controllers in power transmission and distribution. India: New Age International Publishers, 2007.

[19] Kumar P, Kumar N, Akella AK. A simulation based case study for control of DSTATCOM. ISA T 2014; 53: 767-775.

[20] Hendershot JR, Miller TJE. Design of Brushless Permanent Magnet Motors. Oxford, UK: Magna Physics, 1994.

[21] Duffey CK, Stratford RP. Update of harmonic standard IEEE-519: IEEE recommended practices and requirements for harmonic control in electric power systems. IEEE T Ind Appl 1989; 25: 1025-1034.

Appendix

System parameters for simulation work as follows:

Three-phase supply voltage: 415 V, 50 Hz

Distribution line impedance: $L_s = 40$ mH, $R_s = 1.57\Omega$

Three phase R–L load: $R_a = 50\Omega$, $L_a = 200$ mH, $R_b = 75\Omega$, $L_b = 225$ mH, $R_c = 25\Omega$, $L_c = 175$ mH

Three-phase rectifier load: $R_d = 125\Omega$, $L_d = 30$ mH

Filter parameter: $L_f = 5.0$ mH

DC capacitance and voltage: $C_{dc} = 4000\ \mu$F, $V_{dc} = 400$ V

DC inductance: $L_{dc} = 1.0$ mH

Controller parameter (proportional and proportional + integral): $K_{p1} = 0.6$ and $K_{p2} = 0.2$, $K_i = 6.5$

PWM switching frequency: 10 kHz

Power converter: IGBTs/diodes