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Control of a ternary voltage progression based cascaded multilevel inverter using classy split multicarrier pulse width modulation

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Abstract: In this paper, a new hybrid pulse width modulation technique is proposed to enhance the performance of output voltage from a ternary progression based multilevel inverter. For high power applications, the multilevel inverter can appropriately replace the traditional converter without a transformer and the separate DC sources will be indispensable for various renewable energy sources. The classy split switching technique for the multicarrier pulse width modulation technique is adopted and the concept about new topology is presented in this paper. An arm controller has been chosen to implement the modulation due to its superior features, easy software, and hardware design. Simulation and experimental results are also presented.

Key words: Classy split modulation technique, unequal DC source, total harmonic distortion (THD), ternary voltage progression, arm controller

1. Introduction

Nowadays, the distinctive structure of multilevel inverters that reduce the harmonic content thereby decreases the filter requirement [1–3]. These are easily suited to high power applications such as utility supplies and motor drives. Due to this accomplishment, the contribution of multilevel inverters is significantly increased for high performance industrial needs. The output voltage and power can be increased without increasing the rating of individual devices [4–7]. The cascaded inverter has a disadvantage, it needs separate DC sources, but circuit layout is compact and the voltage sharing problem is absent. Application of the cascaded inverter for renewable energy systems is reviewed in [8]. Furthermore, asymmetric cascaded multilevel inverters use unequal DC sources, which increase the modularity of the circuit. Researchers have strived to introduce a new topology for multilevel converters with a reduced number of components compared to conventional multilevel converters [9].

This topology consists of series connected submultilevel converter blocks. The major disadvantage associated with a reduced number of switches is their circuit complexity due to the bulky capacitor. Additional design complications might be imposed, especially regarding the design of device heat sinks. Unfortunately, the modulation technique does not serve the purpose with the increased number of auxiliary bridges. Moreover, a large number of auxiliary bridges have to be employed and large capacitor banks need to be included. An attempt has been made to find the performance of the cascaded multilevel inverter topologies [10–12]. PWM modulation for the cascaded inverter is a well established and intensive research topic [13–16], but some modification of

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the modulation process is done to maintain the balanced DC voltage [17]. To obtain low distorted output voltage phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD) modulation techniques are used [18]. For low switching frequency applications, selective harmonic elimination and space vector control techniques are used [19,20]. In this paper, a new constant switching frequency multicarrier methodology is used to control the presented inverter. The intent of control is to compare the sinusoidal wave with various multicarrier topologies using a ternary voltage progression multilevel inverter. These control techniques are used to reduce the harmonic content in output voltage waveform and also provide customized voltage wave shaping to the specified needs. The advantage of ternary progression is compact circuit layout, less switching losses, reduced semiconductor switches, and optimized output voltage quality. Increasing the number of levels provides more steps. The output voltage will be of enhanced resolution and the reference sinusoidal output voltage can be better achieved.

A classy split modulation technique with constant switching frequency is demonstrated and the feasibility of a multilevel inverter with less total harmonic distortion is presented. The first section deals with advances in cascaded multilevel inverter topologies. In Section 2, the suggested topology is well explained in terms of working principles, voltage steps, and DC supply selection. In Section 3, the proposed configuration and the followed method for the determination of DC voltage source levels are compared with another counterpart. Section 4 explicates the simulation results. Section 5 includes brief experimental setup details.

2. Circuit description

The hybrid inverter topology with unequal DC sources is predominant [21–23]. This inverter has the advantages of reduced DC supply and semiconductor switches. Moreover, this inverter requires fewer cascaded cells to achieve the maximum output voltage [24].

2.1. Modeling of inverter

For each full bridge inverter, the output voltage is given by

$$\mathrm{V}_{0i} = \mathrm{V}_{dc}\ (\mathrm{S}_{1i} - \mathrm{S}_{3i}) \tag{1}$$

and input DC current is

$$\mathrm{I}_{dci} = \mathrm{I}_a(\mathrm{S}_{1i} - \mathrm{S}_{3i}) \tag{2}$$

$i = 1, 2, 3\ldots$ (number of full bridge inverters employed). I_a is the output current of the inverter. S_{1i} and S_{3i} are the upper switches of each full bridge inverter. The output voltage of each phase of the multilevel hybrid inverter is given by

$$V_{on} = \sum_{i=1}^{n} V_{oi} \tag{3}$$

A new constant switching strategy based ternary progression multilevel inverter is illustrated in Figure 1. Ternary configuration is based on geometric progression (GP), i.e. the succeeding source has a value equal to three times that of the preceding source. This is an unequal voltage progression with amplitude of DC voltage having a ratio of 1:3 and the maximum output voltage reaches $((3^N - 1)/2)\ V_{dc}$.

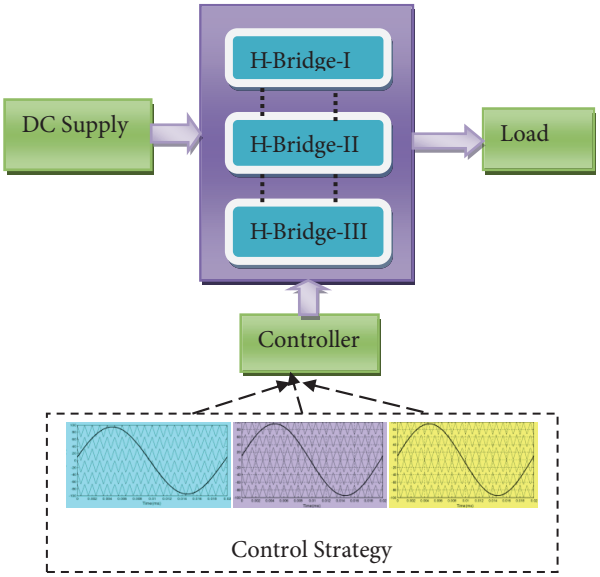


Figure 1. Schematic diagram of cascaded multilevel inverter with new control strategy.

Each subsystem connected to the inverter generates a controlled signal from the controller. H_1 bridge is connected to the phase disposition modulation scheme, H_2 bridge is connected to the alternate phase opposition disposition modulation scheme, and H_3 bridge is connected to the phase opposition disposition modulation scheme. For using ternary progression, also called order-3, DC voltages of V_{dc} = 1V then V_{dc2} = 3V ..... $V_{dcmin} = 3^N V$ are required. The ternary progression technique will have amplitude of DC voltage in the ratio 1:3:9:27: ..... 3^N. As per the switching patterns given in Table 1, driving pulses for the H-bridges were developed. The generated gate pulses are given to each switch in accordance with the developed angle of intervals as shown in Table 2.

Table 1. Operation of ternary multilevel inverter during positive cycle.

Mode level	H-Bridge-I		H-Bridge-II		H-Bridge-III		Voltage level
	ON Switch	OFF Switch	ON Switch	OFF Switch	ON Switch	OFF Switch	
I	S1, S2	S3, S4	S6, S8	S5, S7	S10, S12	S9, S11	V_{dc}
II	S3, S4	S1, S2	S5, S6	S7, S8	S10, S12	S9, S11	$2V_{dc}$
III	S2, S4	S1, S3	S5, S6	S7, S8	S10, S12	S9, S11	$3V_{dc}$
IV	S1, S2	S3, S4	S5, S6	S7, S8	S10, S12	S9, S11	$4V_{dc}$
V	S3, S4	S1, S2	S7, S8	S5, S6	S9, S10	S11, S12	$5V_{dc}$
VI	S2, S4	S1, S3	S7, S8	S5, S6	S9, S10	S11, S12	$6V_{dc}$
VII	S1, S2	S3, S4	S7, S8	S5, S6	S9, S10	S11, S12	$7V_{dc}$
VIII	S3, S4	S1, S2	S6, S8	S5, S7	S9, S10	S11, S12	$8V_{dc}$
IX	S2, S4	S1, S3	S6, S8	S5, S7	S9, S10	S11, S12	$9V_{dc}$
X	S1, S2	S3, S4	S6, S8	S5, S7	S9, S10	S11, S12	$10V_{dc}$
XI	S3, S4	S1, S2	S5, S6	S7, S8	S9, S10	S11, S12	$11V_{dc}$
XII	S2, S4	S1, S3	S5, S6	S7, S8	S9, S10	S11, S12	$12V_{dc}$
XIII	S1, S2	S3, S4	S5, S6	S7, S8	S9, S10	S11, S12	$13V_{dc}$

For N such cascaded inverters, one can achieve the following distinct voltage levels:

$$n = 3^N, \text{ if } V_{dc,j} = 3^{j-1} V_{dc}, j = 1, 2, \ldots, N \tag{4}$$

Table 2. Angles of interval up to 90°.

Angle of interval in degrees	Values
0–6.9	V
6.9–13.8	2V
13.8–20.7	3V
20.7–27.6	4V
27.6–34.5	5V
34.5–41.4	6V
41.4–48.3	7V
48.3–55.2	8V
55.2–62.1	9V
62.1–69	10V
69–75.9	11V
75.9–82.8	12V
82.8–89.7	13V

The maximum output voltage of this N cascaded multilevel inverter is

$$V_{o,MAX} = \sum_{j=1}^{N} V_{dc,j} \tag{5}$$

$$V_{o,MAX} = \left(\frac{3^N - 1}{2}\right) V_{dc} \tag{6}$$

If $V_{dc,j} = 3^{j-1}V_{dc}, j = 1, 2, \ldots, N$.

From Eq. (6), it can be seen that the asymmetrical multilevel inverter can generate higher output voltage levels with fewer switches. The power delivered for ternary configuration with 1:3:9 ratio is given as

$$P_{Load} = \sum\nolimits_{j=0}^{N} \left(V_{rms}^{f}.I_{rms}^{f}.cos\varphi\right)_{j} \tag{7}$$

$$= \left(V_{rms}^{f}.I_{rms}^{f}.cos\varphi\right)_{Aux-2} + \left(V_{rms}^{f}.I_{rms}^{f}.cos\varphi\right)_{Aux-1} + \left(V_{rms}^{f}.I_{rms}^{f}.cos\varphi\right)_{Main}, \tag{8}$$

where N is number of auxiliary bridges, $V_{rms}^{f}.I_{rms}^{f}.cos\varphi$ are the fundamental voltages, current, and the power factor, respectively, when j = 0 represents the main bridges, which consume maximum power, j = N represents the number of auxiliary bridges, when the H - bridges are scaled by power of 3, each level being $V_{dc}/3^N$.

Using Fourier series decomposition, each step is evaluated by integration.

$$(V_{max}^{f})_{load} = \frac{8}{\omega T}\frac{V_{dc}}{3^N} \times \left(\int_{\theta=0}^{\theta=\cos^{-1}\left(\frac{1}{3^{N+1}}\right)} COS\,(\theta)d\theta + \int_{\theta=0}^{\theta=\cos^{-1}\left(\frac{3}{3^{N+1}}\right)} COS\,(\theta)d\theta + \int_{\theta=0}^{\theta=\cos^{-1}\left(\frac{2N+1}{3^{N+1}}\right)} COS(\theta)d\theta \right) \tag{9}$$

$$(V_{max}^{f})_{load} = \frac{4Vdc}{3^N\pi} \sum\nolimits_{j=0}^{j=\frac{3^{N+1}-1}{2}} \int_{\theta=0}^{\theta=\cos^{-1}\left(\frac{2j+1}{3^{N+1}}\right)} COS(\theta)d\theta \tag{10}$$

From Eq. (10) when N = 2, for a 27-level inverter, the value of $(V^f_{max})_{load}$ in terms of V_{dcis}

$$(V^f_{max})_{load} \vdots^{N=2} = \frac{4Vdc}{9\pi} \sum_{j=0}^{j=13} \int_{\theta=0}^{\theta=\cos^{-1}(\frac{2j+1}{27})} COS(\theta) d\theta \tag{11}$$

3. Control strategy for multilevel inverter

The most preferable control technique available for the asymmetric cascaded multilevel inverter is the PWM technique, which produces less harmonic distortion. Modulation of the asymmetric multilevel inverter is quite challenging. A heuristic investigation is based on carrier PWM modulation string in this work. Overall performance of the multilevel inverter is compared to adopt the best modulation strategy. Mostly a carrier based strategy derived from [19] for generating driving pulses of MLI is considered. Figure 2 illustrates the generalized switching pattern of level shifted PWM modulation strategy with sinusoidal reference and triangular multicarrier signal at constant frequency. A different modulation scheme such as PD, APOD, POD, or PS was used for cascaded MLI for generating modulated driving pulses. For the N-level inverter $(N-1)$ carrier signals are required. The intention of the modulation scheme is to pursue low current harmonic distortion and reduction of switching losses with improved harmonic performance.

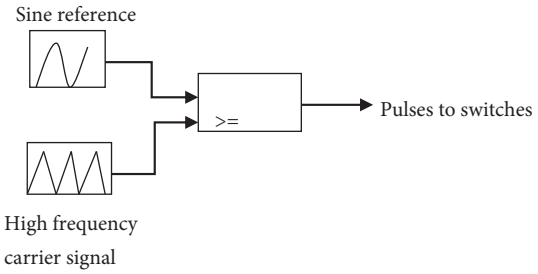


Figure 2. Pattern of gate pulse generation circuit for the switches (level shifted PWM).

3.1. Proposed modulation technique

The classy split modulation technique is the combination of PD modulation, APOD modulation, and POD modulation for an asymmetric cascaded multilevel inverter. the modulation principle differs from the conventional modulation technique in which each arm is provided with different modulation schemes so that the output voltage inherits better harmonic performance and reduced switching losses. In this modulation technique, each bridge of the asymmetric MLI is operated by different modulation schemes; H_1 bridge switches are triggered using PD modulation, H_2 bridge switches are triggered using APOD modulation, and H_3 bridge switches are triggered using POD modulation. This classy split modulation technique is introduced to obtain the best harmonic spectrum that can be used for controlling different motor drive applications. Most carrier based PWM techniques use carrier disposition PWM strategies. Commonly referred strategies; Phase Disposition (PD), where all carriers are in phase: phase opposition disposition (POD), where the carriers above the sinusoidal reference zero point are 180° out of phase with those below the zero point; and alternative phase opposition disposition (APOD), where each carrier is phase shifted by 180° from its adjacent carrier.

For the cascaded inverter, the level shifted PWM technique is the most common strategy. Improved harmonic performance is achieved when each H-bridge of the inverter is controlled by combining the three

modulation schemes. During switching, each leg must be modulated by a proper carrier to maintain the carrier signal at all times. For the classy split modulation technique, the carrier modulation is split into three sections, with each cell synthesizing a different modulation schemes as depicted in Figure 3. For one H-bridge, the positive signal is modulated and the negative signal is also modulated. They are re-modified to provide control signals under the split PWM strategy. The logic circuit for the generation of control signals using the classy split modulation technique is shown in Figure 4. High frequency of 20 kHz is logically compared with the reference sinusoidal wave. For the presented CSPWM technique, the signal from the negative s_3 and the signal from the positive s_1 are added together to generate the driving pulses for the switch S_1 signal. Similarly the driving patterns for the switches used in the other two bridges are also generated.

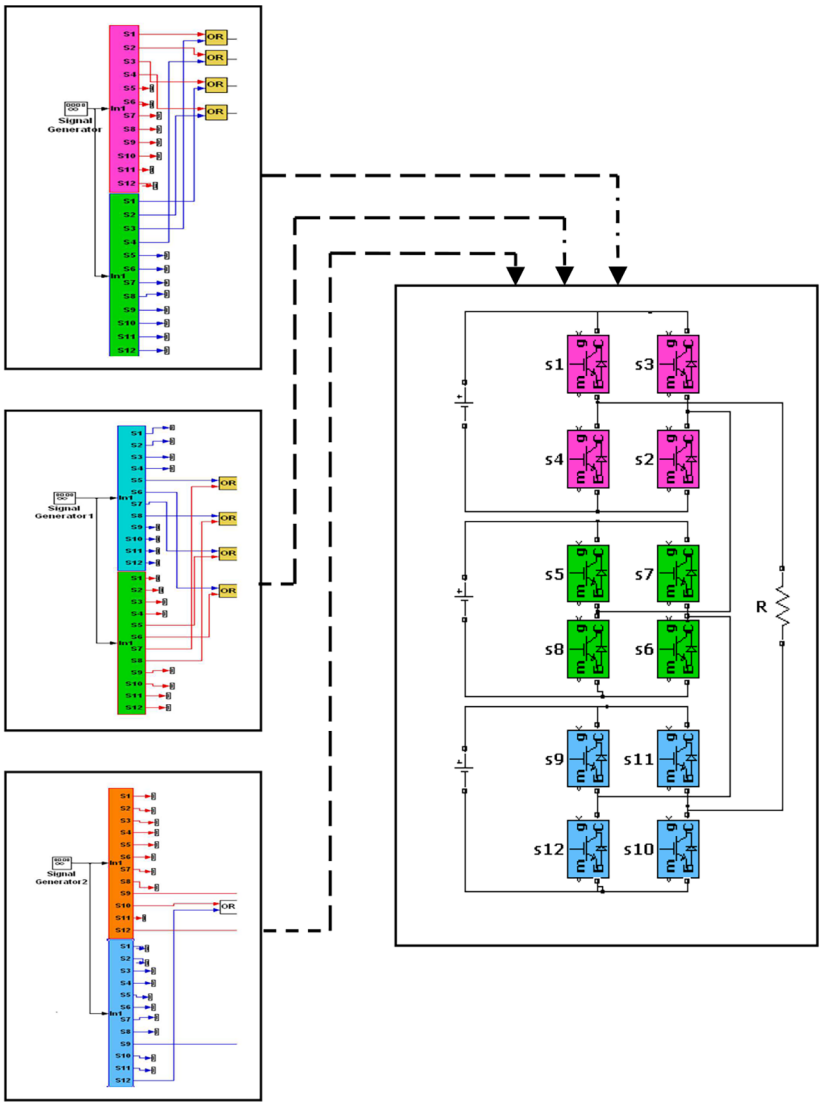


Figure 3. Simulink model of classy split modulation technique.

4. Simulation results

The ternary voltage based cascaded multilevel inverter involves the usage of only three H-bridges. In carrier based modulation, each level in the phase requires a carrier of its own. Modulation schemes are categorized into

two types: level shifted (LSPWM) and classy split modulation (CSPWM). Both of these have several variations, which differ by the allocation of carriers.

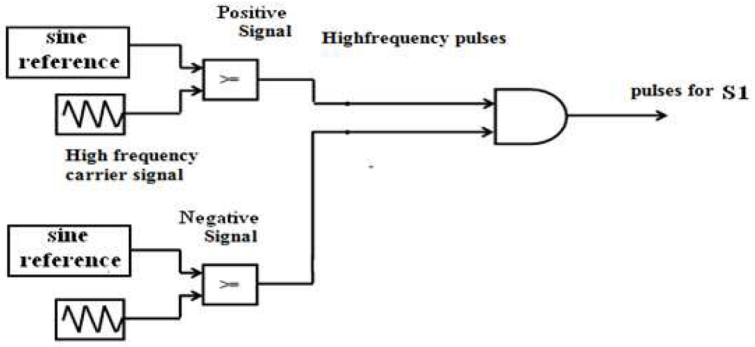


Figure 4. Pattern of gate pulse generation circuit for the switches (classy split modulation).

4.1. LSPWM modulation

In level shifted PWM methods, the carriers of the modules have the frequency of $f\mathrm{car} = 1/T_{sw}$ where the frequency of the carrier signal is inversely proportional to the switching period of the device. The LSPWM technique is the logical extension of the sine triangle PWM multilevel inverter, in which (N-1) carriers are needed for an N-level inverter. Frequency modulation ratio (m_f) is defined as the ratio of carrier frequency (f_c) and modulating frequency (f_m)

$$m_f = f_c/f_m \tag{12}$$

From the simulation work, it is seen that the PD technique produces less harmonic content on a line-to-line basis compared to the other two techniques. The carriers are arranged in vertical shifts in continuous bands defined by the levels of the inverter. An N-level inverter using level shifted multicarrier modulation requires (N-1) triangular carriers, all having same frequency and peak to peak amplitude; hence for a 27-level inverter, 26 carriers are used. The modulated output voltage waveform for a PD modulation based 27 level inverter is shown in Figure 5a and the corresponding harmonic spectrum is given in Figure 5b.

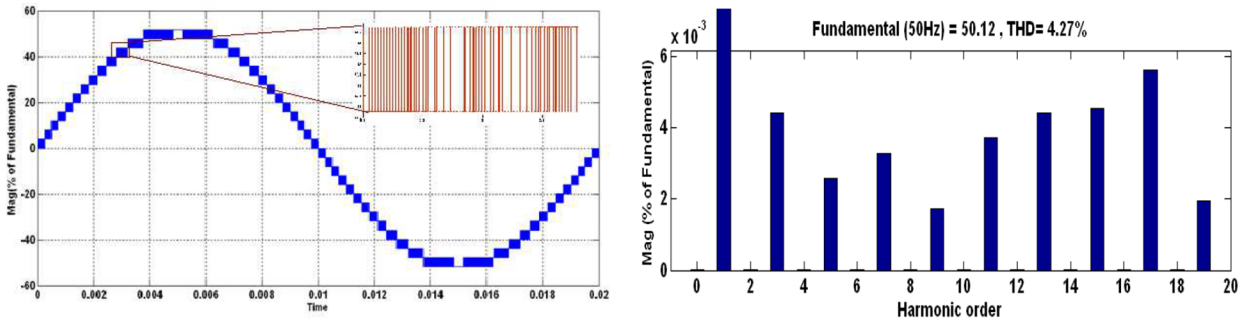


Figure 5. Simulation results: (a) Output voltage of LSPWM modulation; (b) Harmonic spectrum of output voltage.

4.2. Classy split modulation

In the ternary based cascaded multilevel inverter, different modulation schemes are available to perform the control strategy of the multilevel inverter. Modulation is generally performed in any circuit to reduce the

harmonic content at the output voltage. This section discusses the development of driving pulses for the ternary based cascaded multilevel inverter using CSPWM modulation. The operation of CSPWM involves three LSPWM modulations (PD, APOD, and POD). By properly combining these three techniques, CSPWM carrier pulses are generated as shown in Figure 6. It differs from hybrid modulation, where the frequency of the positive rail differs from the negative one and from the discontinuous modulation; the reference waveform must split into sections [9]. As discussed in section 3.1, the CSPWM pulses are generated for a 27 level ternary based multilevel inverter. To generate the switching pattern for the presented technique, efforts are taken to generate the carrier signals for H-Bridges. The generated carrier signals are split into the required fashion to develop the pattern for CSPWM.

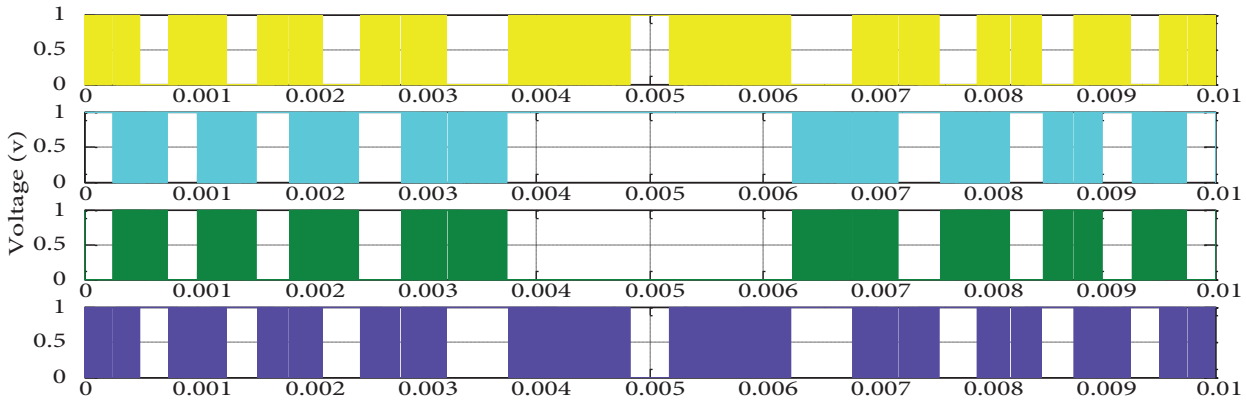


Figure 6. Generation of the CSPWM pulses for the switches S_1, S_2, S_3, and S_4.

The positive and negative carrier signals from the two adjacent subsystems of each cell are compared with the respective sinusoidal reference waveform. Generated signals are added to provide the driving pattern under the CSPWM with the constraint that the positive and negative half cycles of switches remain similar.

$$S_x = P_i + N_i \tag{13}$$

$$i \text{ integers } = 1, 2 \ldots 12$$

$$x \text{ integers } = 1, 2 \ldots .12$$

$$P_i = RS \geq CS_{kj},$$

where

RS is reference signal, CS is carrier signal, kj is amplitude of carrier signal, S is switches, s = signals, and + denotes the logical OR symbol.

Similarly the switching patterns for the remaining switches are derived according to Eq. (13), subjected to the constraint. For the positive half of the cycle, the driving signals of the switches S_1 and S_3 are considered. As the magnitude of the reference signal (RS) is greater than the magnitude of the carrier signal (CS) for the corresponding kj values, the control logic circuit generates the driving signal s_1. Similarly the control logic is given to generate the driving pulse for other switches. Symbolically, the logic for generation of the driving signal for the switch S_1 can be written as

$$S_1 = s_{1+}s_3; \tag{14}$$

$$Rs \geq Cs_1 = s_1 : Rs \geq Cs_3 = s_3$$

In a similar way,

$$S_2 = s_{2+}s_4; \tag{15}$$

$$Rs \geq Cs_2 = s_2 : Rs \geq Cs_4 = s_4$$

$$S_3 = s_{3+}s_1; \tag{16}$$

$$Rs \geq Cs_3 = s_3 : Rs \geq Cs_1 = s_1$$

$$S_4 = s_{4+}s_2; \tag{17}$$

$$Rs \geq Cs_4 = s_4 : Rs \geq Cs_2 = s_2$$

The logical representation of gate pulse generation for the switches using the proposed logic is given in Table 3. The simulation results of the classy split based multilevel inverter are illustrated in Figure 7a. Harmonic analysis is also performed to compare with the conventional multicarrier inverter topology as depicted in Figure 7b.

Table 3. Fabricated PWM signal for classy split modulation.

Switches (S_W)	Classy split PWM operation
$S_1 = s_{1+}s_3$	Rs $\geq$ Cs$_{kj}$ = s$_1$: Rs $\geq$ Cs $_{kj}$ = s$_3$
$S_2 = s_{2+}s_4$	Rs $\geq$ Cs$_{kj}$ = s$_2$: Rs $\geq$ Cs $_{kj}$ = s$_4$
$S_3 = s_{3+}s_1$	Rs $\geq$ Cs$_{kj}$ = s$_3$: Rs $\geq$ Cs$_{kj}$ = s$_1$
$S_4 = s_{4+}s_2$	Rs $\geq$ Cs$_{kj}$ = s$_4$: Rs $\geq$ Cs $_{kj}$ = s$_2$

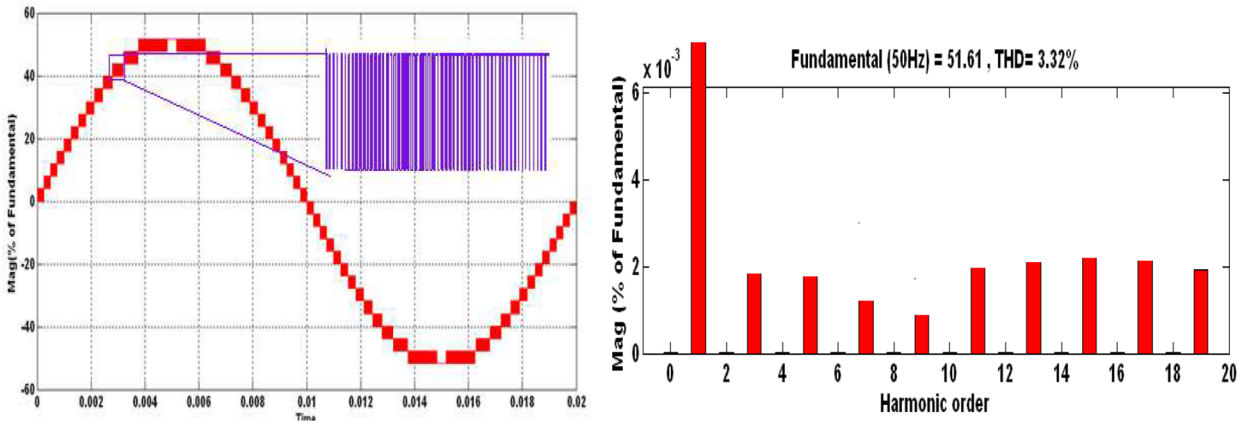


Figure 7. (a) Output voltage of CSPWM modulation; (b) Harmonic spectrum of output voltage.

In this paper, a new constant switching frequency methodology is used to control the presented inverter. The intent of control is to compare the sinusoidal wave with various multicarrier topologies using a ternary voltage progression multilevel inverter. These control techniques are used to reduce the harmonic content in output voltage waveform and also provide the customized voltage wave shaping for the specified needs. The advantage of ternary progression is its compact circuit layout, less switching losses, reduced semiconductor switches, and optimized output voltage quality. A classy split modulation technique with constant switching frequency that demonstrated the feasibility of a multilevel inverter with less total harmonic distortion is presented.

Table 4 gives the comparison of classy split modulation with and without the conventional modulation strategy. The comparison in the table is in accordance with the same number of bridges with and without modulation. From the table it is clear that the THD content of classy split modulation has less harmonic content compared to the conventional configurations. Figure 8 depicts the THD content of output voltage for various modulation index values. As the modulation index is decreased the distortion grows. In conventional topology output voltage waveform has less total harmonic distortion only for higher modulation indices. In the presented topology even with decreased modulation indices the THD content meets the IEEE standard 519. Figure 9 depicts the reduction in lower order harmonics and the presented modulation technique provides good quality voltage waveforms, having almost perfect currents, and eliminating lower order harmonic to a larger extent. From Figures 10a and 10b, it is observed that the number of drivers required and the THD content with respect to the number of levels are higher in conventional topology compared to the presented technique. It is proven that there is 75% reduction not only in bridges but also in IGBTs and 7.96% of THD reduction in conventional topology without PWM modulation and a percentage of reduction compared to conventional level shifted PD modulation technique. From Figure 11a it is found that the proposed modulation yields higher fundamental components with increasing modulation index. To prove that classy split modulation was superior to conventional modulation, the comparison was done and the same is given in Figures 11b, 11c, and 11d.

Table 4. Comparison of classy split modulation with and without conventional modulation.

Parameters	Without modulation	Level shifted modulation	Classy split modulation
Number of switches	12	12	12
Number of DC sources	3	3	3
Fundamental voltage	41.93	50.12	51.61
h3	11.18	1.17	0.22
h5	4.07	0.43	0.14
h7	2.12	0.22	0.1
h9	1.31	0.14	0.07
Distortion factor (DF_1)	0.0596	0.0213	0.016
Distortion factor (DF_2)	0.0122	0.0071	0.005
Modulation index	THD %		
0.3	13.9	6.8	4.3
0.4	13.32	6	4
0.5	11.28	4.27	3.32
0.6	9.83	4.1	3
0.7	9.28	3.8	2.8

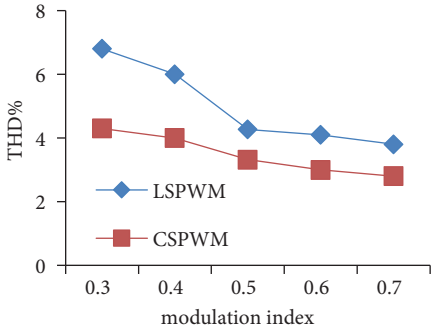


Figure 8. Output voltage THD versus modulation index.

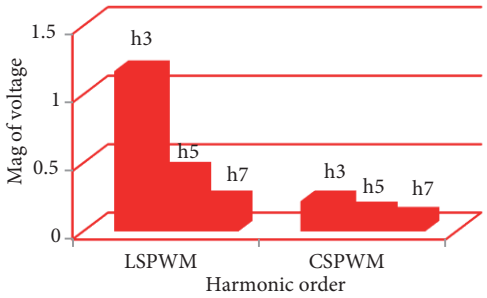


Figure 9. Magnitude of the voltage versus harmonic order.

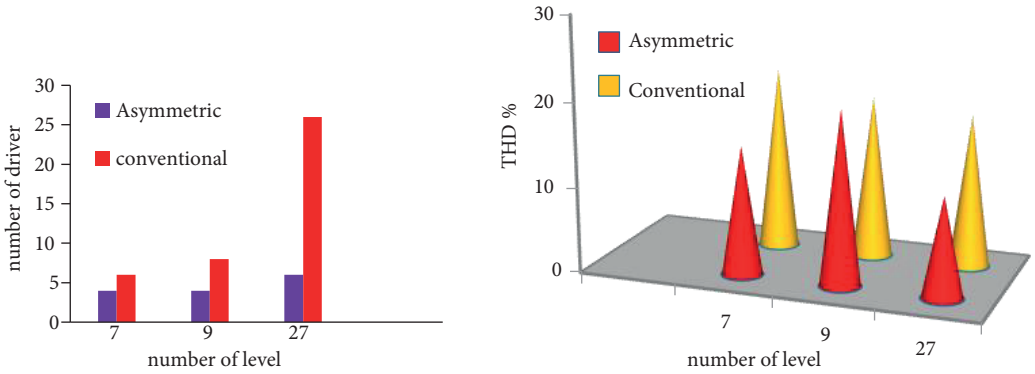


Figure 10. a. Number of drivers versus number of levels. b. THD % versus number of level

5. Experimental results

A prototype of the classy split modulation strategy is fabricated to validate the control scheme used in a ternary voltage progression based multilevel inverter. Simulation results of the control scheme are validated using experimental results. The hardware layout of the system is shown in Figure 12. The prototype of this inverter includes three DC supplies, three H-bridge power circuits, and an embedded controller (ARM Cortex-M0 Core NUC140XXCN microcontroller.

The power supply circuit comprises a step down transformer and a voltage regulator IC 7805 and 7812, which provides the DC voltage to the controller and the driver circuit. An ARM Cortex-M0 Core NUC140XXCN microcontroller is chosen to provide the driving pulses because of its superior features like

- Meeting the computing needs of the task on hand efficiently and cost effectively.
- The NuMicro NUC100 Series is a 32-bit microcontroller with embedded ARM Cortex-M0 core, the cost is equivalent to a traditional 8-bit microcontroller.
- Wide availability and reliable sources.

The control circuit decides the sequence of pulses to be given to the switches in the power circuit. The driver circuit amplifies the pulses to the required level. The driver circuit is used for an isolation of the negative current to the microcontroller, amplification of voltage, and to create a constant voltage source. The square pulse should have a constant voltage of 5 V. Isolation refers to the separation of the power circuit from the

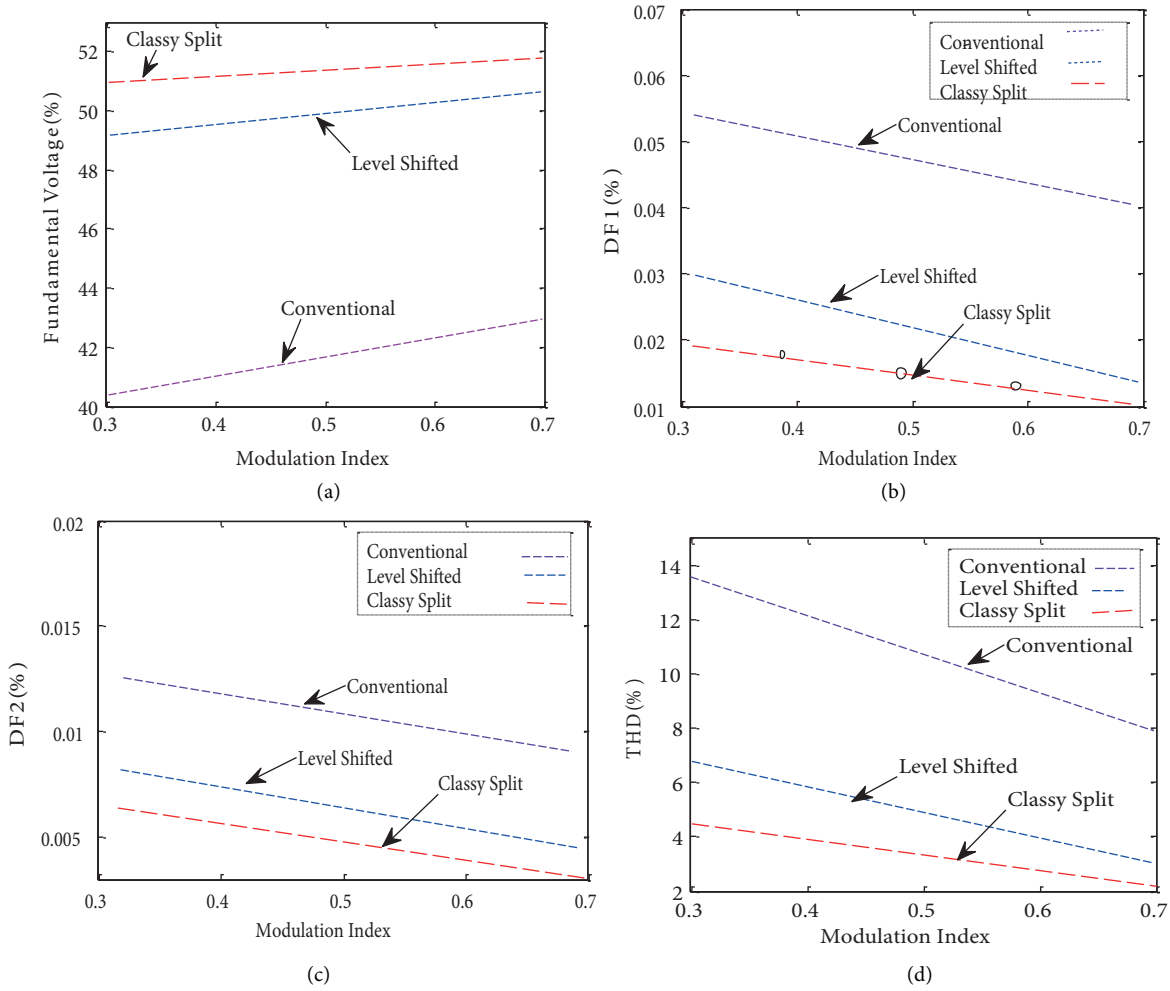


Figure 11. (a) Fundamental voltage (%) versus modulation index; (b) DF1 versus modulation index; (c) DF2 versus modulation index; (d) THD (%) versus modulation index.

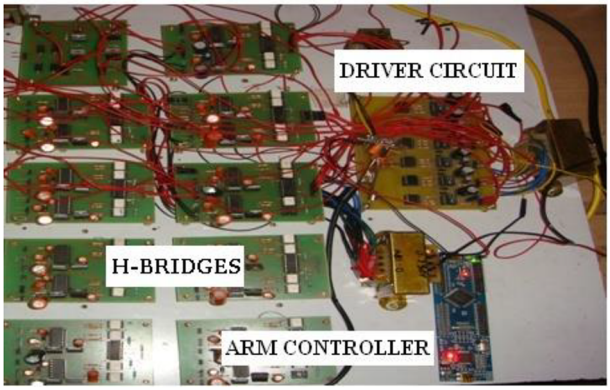
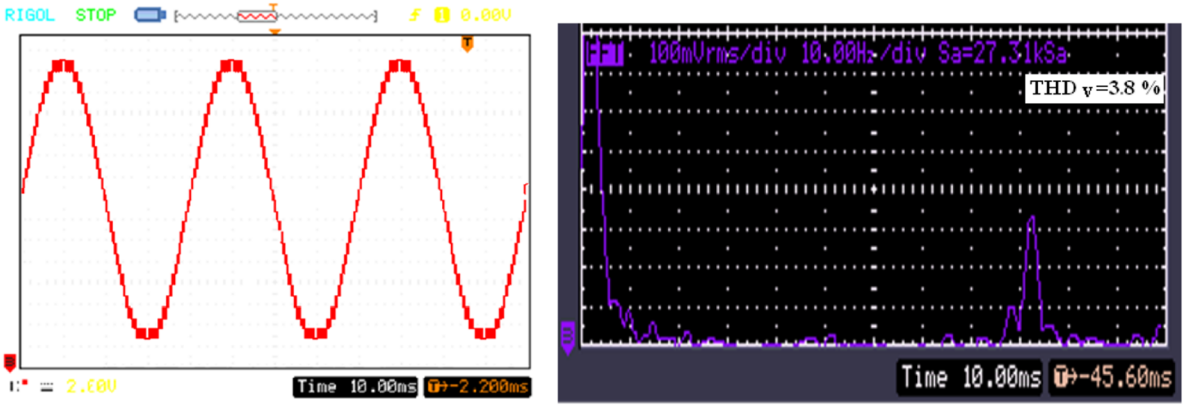


Figure 12. Hardware layout of CSPWM system.

control circuit. Output voltage from the microcontroller is given to the driver IC, and the output voltage will have an increased magnitude that will be sufficient for driving the MOSFET.

A power circuit is fabricated using 12 IRF540 type MOSFETs and it requires three individual DC sources of an asymmetric ternary ratio. During the hardware implementation, the magnitude of inverter voltage is tested for 52 V. Each inverter leg takes different voltages. During the implementation, the inverter input sources are taken as $V_{dc1} = 4$ V, $V_{dc2} = 12$ V, and $V_{dc3} = 36$ V.

Modulation is generally performed in any circuit to reduce the harmonic content at the output voltage. The control circuit for the classy split modulation strategy is implemented using a NUC140XXCN arm controller. The controller produces the CSM pulses required by the switches of the cascaded MLI. Pulses from the controller are amplified using IR2110 for the low side and IR2115 for the high side. The output voltage waveform with the modulation performed at 20 kHz switching frequency is recorded using a RIGOL DS1052E type digital oscilloscope. The output voltage and the spectrum voltage are shown in Figures 13a and 13b, respectively. It is observed that these oscillograms follow the simulation and theoretical results discussed in the previous sections.



(a) (b)

Figure 13. Hardware results: (a) Output voltage waveform of CSPWM (X axis 1 cm = 10 ms, Y axis 1 cm = 20 V); (b) Harmonic spectrum of output voltage.

6. Conclusions

In this paper, a new classy split modulation technique for a cascaded multilevel inverter operating at a higher switching frequency is proposed. The proposed technique combines with the well-known multicarrier pulse width modulation: PD, APOD, and POD. Compared to conventional modulation schemes, fewer commutations and considerable switching loss reduction are obtained with the classy split pulse width modulation strategy. The harmonic profile of the classy split harmonics scheme is analyzed and it seems there is a strong reduction in output voltage harmonics. This methodology enhances the performance of output voltage for a ternary multilevel inverter. Simulation and experimental results have been validated.

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