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Selective harmonics elimination PWM with self-balancing DC-link in photovoltaic 7-level inverter

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Abstract: In this paper, a new DC-link balancing method for a 7-level inverter fed by a photovoltaic system is proposed. The proposed redundant state technique is associated with selective harmonics elimination (SHE)-PWM instead of space vector (SV)-PWM. The switching angles related to the SHE are computed via the resultant theory method. Moreover, the study of this inverter is carried out on its equivalent matrix model. On the basis of this model, the link between the capacitor voltage, switching states, and load current is established. This allows understanding the switching redundancies' effect on the DC capacitor voltage balance. An algorithm is then developed to select the appropriate switching state, since there are 300 switching states and 720 unbalanced cases of the voltage capacitor. The proposed balancing method is tested in the case where the input DC inverter is provided by a photovoltaic generator (PVG) system and feeding an induction motor. The obtained results show that the 6 DC PVG capacitor voltages are kept balanced while cancelling the most undesirable harmonics row (5th, 7th, and 11th) in the inverter output voltage. Thus, using this cascade, photovoltaic supplying DC power can be amplified into high quality AC power.

Key words: Multilevel inverter, selective harmonics elimination pulse width modulation, photovoltaic system, switching states, balancing DC-link technique

1. Introduction

Mankind has witnessed an enormous increase in energy consumption over the last 100 years. Renewable energy sources are considered among the most promising solutions to fulfill energy requirements. Solar energy based on the photovoltaic phenomenon allows the direct conversion of solar radiation into DC electrical energy with no noise, no pollution, and no moving parts, making it robust, reliable, and long-lasting [1]. The cost still remains a challenge facing researchers.

However, this system is commonly used in large-area applications such as satellite systems, lighting, mobile applications, drives, or telecommunication systems.

The use of a PV system to supply an AC load is possible after transforming the DC power from PV arrays into utility-grade AC power via static inverters [2–4]. The simplest topology that can be used for this conversion is the 2-level inverter that consists of 4 switches. Previous works show that the traditional 2-level inverter has limitations in handling high power and voltage applications. Hence, multilevel inverters are strongly suggested as an efficient solution for high-speed semiconductor applications. The multilevel inverter offers higher efficiency and operates at low frequency. Additionally the, use of these inverters allows the generation of a high-output

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voltage waveform as compared to the 2-level inverter. Their principal advantages are decreased size of the filter, lower dv/dt ratio, lower electromagnetic interference level, and lower switching losses. Multilevel inverters have mainly been used in medium- or high-power system applications, such as static reactive power compensation and adjustable-speed drives [5,7]. They can be designed by connecting semiconductors in different ways. The most popular topologies are the flying capacitor, cascaded H-bridge, and neutral point clamped (NPC) [8–11].

When the number of inverter levels is increased, the output voltage has more steps, and this staircase-generated waveform will be closer to the desired sinusoidal waveform, reducing harmonics distortion and low voltage stresses. Nevertheless, a high level number in multilevel inverters increases the control complexity. Several pulse width modulation (PWM) strategies for multilevel inverters based on different approaches have been developed in the last decade [11–15]. The most popular ones are multilevel carrier-based PWM and space vector (SV)-PWM, which has been successfully applied in multilevel converters [12,13]. However, the power switches operate with relatively high frequency and the elimination of lower-order harmonics is not guaranteed. Selective harmonics elimination PWM (SHE-PWM) has emerged as a promising control modulation method for the multilevel inverter to achieve these objectives. Using this PWM, switches operate at a switching frequency less than 1 KHz, which is suitable for high-power applications [15,16].

The major difficulty of this PWM lies in solving its inherent nonlinear equations in order to obtain the switching angles [15–22].

Furthermore, multilevel inverters suffer from voltage unbalance of the DC link capacitors. The problem complexity increases when the number of levels is increased above 3. Several solutions have been proposed to overcome this capacitor unbalance problem: an additional power electronics circuit, isolated DC sources, and redundant states with SV-PWM [23–27].

In this paper, a 3-phase 7-level NPC inverter to transmit energy from PV modules to the 3-phase induction motor (IM) is studied. The performance of the redundant states associated with the SHE-PWM instead of the SV-PWM to balance the 6 capacitor voltages is discussed in detail. The elimination of the 5th, 7th, and 11th harmonics with self-balancing DC-link voltages is ensured without any auxiliary circuit.

2. NPC 7-level inverter structure

Figure 1 shows the configuration of a 7-level NPC inverter. It consists of 3 symmetrical legs fed by 6 DC voltages. By commutating the appropriate switches, each phase can produce 7 different voltage levels, and therefore the generated voltage leg waveform has 7 voltage levels (V_{dc}, *5/6* V_{dc}, *2/3* V_{dc}, *1/2* V_{dc}, *1/3* V_{dc}, *1/6* V_{dc}, *0*), where V_{dc} is the total input voltage. Each inverter leg can be modeled by a commutation circuit with 7 ideal switches instead of 12 (Figure 2a). Thus, the 7-level NPC inverter is equivalent to a 3 $\times$ 7 matrix inverter with ideal switches. The matrix structure generates the same waveforms as the NPC structure function of its 6 DC sources (Figure 2b).

The switch function f_{kr} (k is the leg number 1, 2, or 3; r is the sequence number in a leg) is related to the gate transistor signal (F_{kr}) as follows (Table 1):

$$\begin{cases} f_{k1} = F_{k1}F_{k2}F_{k3}\overline{F_{k4}} \\ f_{k2} = F_{k1}F_{k2}\overline{F_{k3}}\,\overline{F_{k4}} \\ f_{k3} = F_{k1}\overline{F_{k2}}\,\overline{F_{k3}}\,\overline{F_{k4}} \\ f_{k4} = \overline{F_{k1}}\,\overline{F_{k2}}F_{k3}F_{k4} \\ f_{k5} = \overline{F_{k1}}\,\overline{F_{k2}}F_{k3}F_{k4} \\ f_{k6} = \overline{F_{k1}F_{k2}F_{k3}}F_{k4} \end{cases} . \quad (1)$$

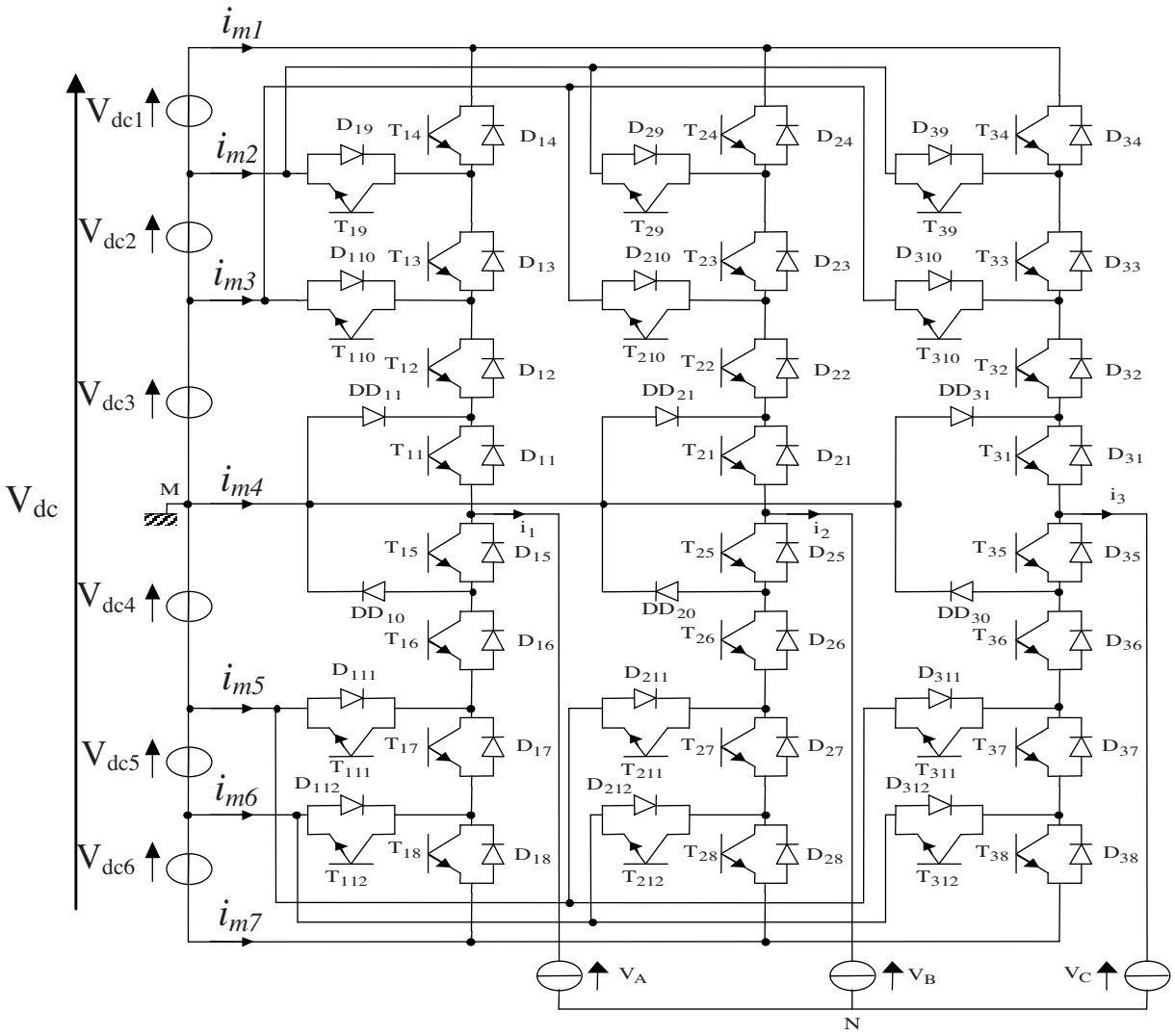

Figure 1. Structure scheme of an NPC 7-level inverter.

Table 1. Equivalent commutation circuit.

NPC structure					Matrix structure						
V_{KM}	Gate signals				Switching functions						V_{KM}
	F_{k1}	F_{k2}	F_{k3}	F_{k4}	f_{k1}	f_{k2}	f_{k3}	f_{k4}	f_{k5}	f_{k6}	
V_{dc}	1	1	1	1	1	0	0	0	0	0	U_{s1}
$5/6V_{dc}$	1	1	1	0	0	1	0	0	0	0	U_{s2}
$2/3V_{dc}$	1	1	0	0	0	0	1	0	0	0	U_{s3}
$1/2V_{dc}$	1	0	0	0	0	0	0	1	0	0	U_{s4}
$1/3V_{dc}$	0	0	1	1	0	0	0	0	1	0	U_{s5}
$1/6V_{dc}$	0	0	0	1	0	0	0	0	0	1	U_{s6}
0	0	0	0	0	0	0	0	0	0	0	U_{s7}

In the case of the 7-level inverter, there are 343 (7^3) switching states that conduct to the space vectors of voltage output, as shown in Figure 3. The space vector is defined as follows:

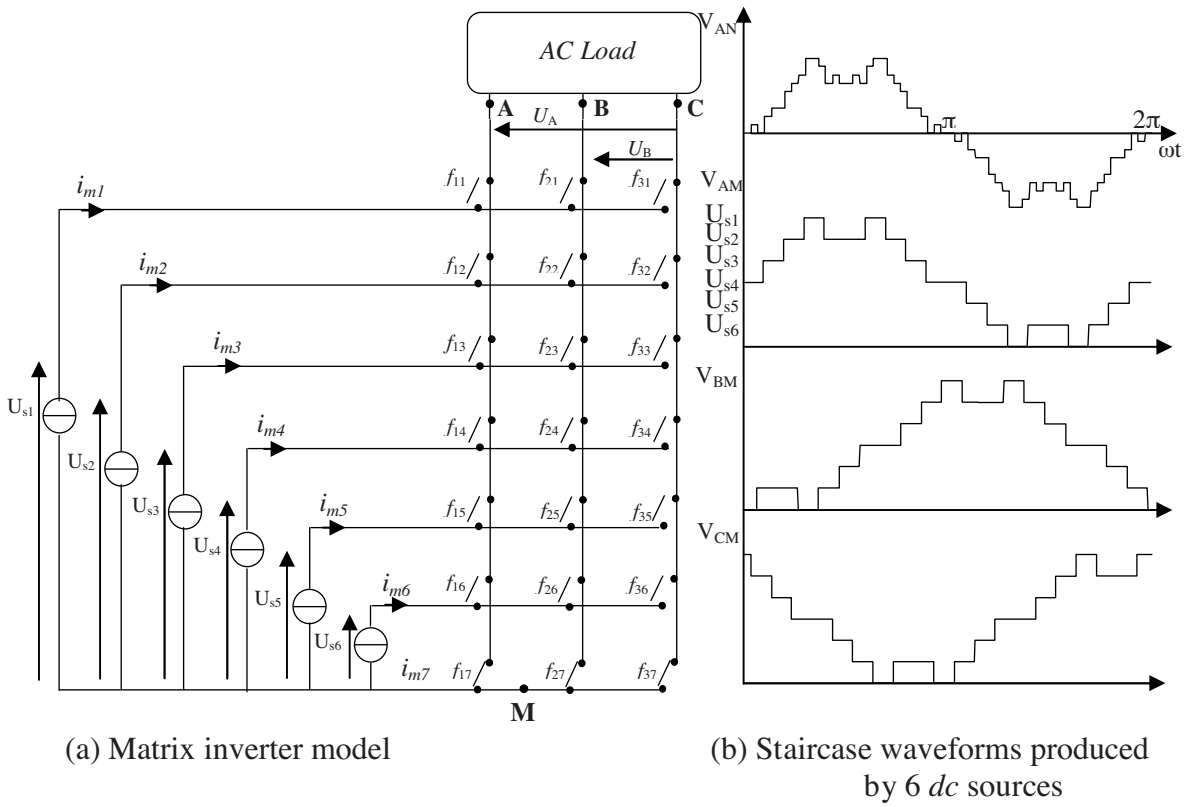

Figure 2. Equivalent model and staircase waveforms: a) matrix inverter model; b) staircase waveforms produced by 6 DC sources.

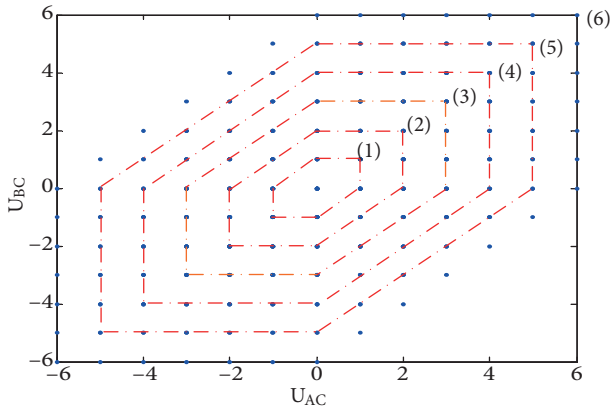

Figure 3. Positions of the output voltage vector of the 7-level inverter in the plan $(0,\ U_{AC},\ U_{BC})$.

$$Vs = \sqrt{\frac{2}{3}}\, V_{dc}[Sw_{1i} + Sw_{2i}\, e^{j\,2\pi/3} + Sw_{3i}\, e^{j\,4\pi/3}]\ , \tag{2}$$

where Sw_{ki} (k is the phase number (1, 2, or 3) and i is the switch number) stands for the leg state, and it can only be given by system of Eq. (3).

$$\begin{cases} Sw_{k1} = 6 \;\; if \;\; V_{kM} = \mathrm{V_{dc}} \\ Sw_{k2} = 5 \;\; if \;\; V_{kM} = 5/6\mathrm{V_{dc}} \\ Sw_{k3} = 4 \;\; if \;\; V_{kM} = 2/3\mathrm{V_{dc}} \\ Sw_{k4} = 3 \;\; if \;\; V_{kM} = 1/2\mathrm{V_{dc}} \end{cases} \quad and \quad \begin{cases} Sw_{k5} = 2 \;\; if \;\; V_{kM} = 1/3\mathrm{V_{dc}} \\ Sw_{k6} = 1 \;\; if \;\; V_{kM} = 1/6\mathrm{V_{dc}} \\ Sw_{k7} = 0 \;\; if \;\; V_{kM} = 0 \end{cases} \tag{3}$$

Analysis of Figure 3 shows that the connection between the DC voltages and the AC load through the 7-level inverter conducts to 90 distinct configurations (output vector states) related to the points shaping the hexagons (1, 2, 3, 4, and 5). Moreover, the center of the hexagons concerns the zero-output voltage.

The obtained modulated voltages (U_{AC}, U_{BC}) depend on the switches' functions and the levels of DC voltage as follows:

$$\begin{array}{l} U_{AC} = m_{11}U_{s1} + m_{12}U_{s2} + m_{13}U_{s3} + m_{14}U_{s4} + m_{15}U_{s5} + m_{16}U_{s6} \\ U_{BC} = m_{21}U_{s1} + m_{22}U_{s2} + m_{23}U_{s3} + m_{24}U + m_{25}U_{s5} + m_{26}U_{s6} \end{array} \quad , \tag{4}$$

with:

$$\begin{cases} m_{11} = (f_{11} - f_{31}), & m_{21} = (f_{21} - f_{31}) \\ m_{12} = (f_{12} - f_{32}), & m_{22} = (f_{22} - f_{32}) \\ m_{13} = (f_{13} - f_{33}), & m_{23} = (f_{23} - f_{33}) \\ m_{14} = (f_{14} - f_{34}), & m_{24} = (f_{24} - f_{34}) \\ m_{15} = (f_{15} - f_{35}), & m_{25} = (f_{25} - f_{35}) \\ m_{16} = (f_{16} - f_{36}), & m_{26} = (f_{26} - f_{36}) \end{cases} . \tag{5}$$

In our study, the DC voltage V_{dc} is assumed constant, so:

$$\frac{dV_{dc}}{dt} = \frac{dV_{dc1}}{dt} + \frac{dV_{dc2}}{dt} + \frac{dV_{dc3}}{dt} + \frac{dV_{dc4}}{dt} + \frac{dV_{dc5}}{dt} + \frac{dV_{dc6}}{dt}. \tag{6}$$

Therefore:

$$0 = \frac{1}{c}i_{c1} + \frac{1}{c}i_{c2} + \frac{1}{c}i_{c3} + \frac{1}{c}i_{c4} + \frac{1}{c}i_{c5} + \frac{1}{c}i_{c6}. \tag{7}$$

By using this relation, the current capacitors are:

$$\begin{cases} i_{c1} = \frac{1}{6}(5i_{m2} + 4i_{m3} + 3i_{m4} + 2i_{m5} + i_{m6}) \\ i_{c2} = -\frac{1}{6}(i_{m2} - 4i_{m3} - 3i_{m4} - 2i_{m5} - i_{m6}) \\ i_{c3} = -\frac{1}{6}(i_{m2} + 2i_{m3} - 3i_{m4} - 2i_{m5} - i_{m6}) \\ i_{c4} = -\frac{1}{6}(i_{m2} + 2i_{m3} + 3i_{m4} - 2i_{m5} - i_{m6}) \\ i_{c5} = -\frac{1}{6}(i_{m2} + 2i_{m3} + 3i_{m4} + 4i_{m5} - i_{m6}) \\ i_{c6} = -\frac{1}{6}(i_{m2} + 2i_{m3} + 3i_{m4} + 4i_{m5} + 5i_{m6}) \end{cases} . \tag{8}$$

These capacitor currents depend on the AC load currents as follows:

$$\begin{cases} i_{c1} = \frac{1}{4}(a_{11}\, i_a + a_{12} i_b) \\ i_{c2} = -\frac{1}{4}(a_{21}\, i_a + a_{22} i_b) \\ i_{c3} = -\frac{1}{4}(a_{31}\, i_a + a_{32} i_b) \\ i_{c4} = -\frac{1}{4}(a_{41}\, i_a + a_{42} i_b)\, i_b \\ i_{c5} = -\frac{1}{4}(a_{51}\, i_a + a_{52} i_b)\, i_b \\ i_{c6} = -\frac{1}{4}(a_{61}\, i_a + a_{62} i_b)\, i_b \end{cases}, \tag{9}$$

where the coefficients a_{ij} are connected to switching functions f_{kr} via the previous coefficients m_{ij} as:

$$\begin{cases} a_{11} = (5m_{21} + 4m_{31} + 3m_{41} + 2m_{51} + m_{61}) \\ a_{21} = (m_{21} - 4m_{31} - 3m_{41} - 2m_{51} - m_{61}) \\ a_{31} = (m_{21} + 2m_{31} - 3m_{41} - 2m_{51} - m_{61}) \\ a_{41} = (m_{21} + 2m_{31} + 3m_{41} - 2m_{51} - m_{61}) \\ a_{51} = (m_{21} + 2m_{31} + 3m_{41} + 4m_{51} - m_{61}) \\ a_{61} = (m_{21} + 2m_{31} + 3m_{41} + 4m_{51} + 5m_{61}) \end{cases}, \tag{10}$$

$$\begin{cases} a_{12} = (5m_{22} + 4m_{32} + 3m_{42} + 2m_{52} + m_{62}) \\ a_{22} = (m_{22} - 4m_{32} - 3m_{42} - 2m_{52} - m_{62}) \\ a_{32} = (m_{22} + 2m_{32} - 3m_{42} - 2m_{52} - m_{62}) \\ a_{42} = (m_{22} + 2m_{32} + 3m_{42} - 2m_{52} - m_{62}) \\ a_{52} = (m_{22} + 2m_{32} + 3m_{42} + 4m_{52} - m_{62}) \\ a_{62} = (m_{22} + 2m_{32} + 3m_{42} + 4m_{52} + 5m_{62}) \end{cases}. \tag{11}$$

3. Selective harmonics elimination PWM

Various modulation strategies have been developed and studied in detail, such as multicarrier PWM, SV-PWM, and SHE-PWM.

Among these strategies, only SHE-PWM allows both control of the output voltage fundamental and the elimination of some harmonics of the lower order. However, the complexity of the SHE-PWM technique increases rapidly with the number of levels of the inverter.

In this paper, the target is to cancel the 5th, 7th, and the 11th harmonics. Therefore, the multilevel staircase voltage leg must contain 4 commutations in its first quarter period. Switching angles in the remaining 3 quarter periods are referred to the first quarter, since the voltage waveform is imposed with a double symmetry as shown in Figure 4.

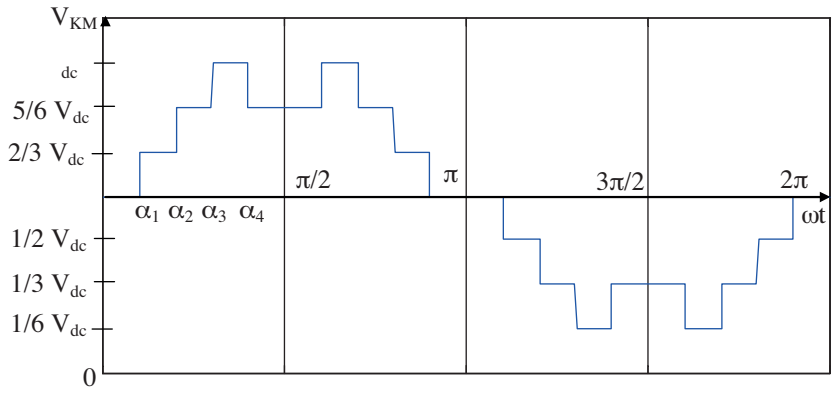

Figure 4. Assigned waveform of the leg voltage for the 7-level inverter (6 DC sources).

To proceed with 6 equal DC sources, the waveform of Figure 4 has a Fourier series expansion of the following form:

$$A_n = \frac{V_{dc}}{\pi n}[\ell_1 \cos(n\alpha_1) + \ell_2 \cos(n\alpha_2) + ... + \ell_c \cos(n\alpha_c)], \tag{12}$$

where n is the harmonic number, c the number of angles necessary to eliminate $(c - 1)$ harmonics, and ℓ_i is unitary coefficients depending on the waveform of the leg voltage (Figure 4).

In the case of Figure 4, these parameters are as follows:

$$n = 5,\ 7,\ 11, \quad c = 4, \ell_1 = 1,\ \ell_2 = 1,\ \ell_3 = 1,\ \ell_4 = -1,$$

under the following constraint:

$$0 \leq \alpha_1 \leq \alpha_2 \leq \alpha_3 \leq \alpha_4 < \frac{\pi}{2}. \tag{13}$$

While replacing these parameters in Eq. (12) and using the modulation index r ($r = \frac{2V^*_{\max}}{V_{dc}}$, where $V^*_{\max}$ is the magnitude of the desired sinusoidal voltage), the system of Eq. (14) is obtained. It contains 4 nonlinear equations with trigonometric terms and 4 unknown variables $(\alpha_1,\ \alpha_2, \alpha_3,\ \alpha_4)$.

$$\begin{cases} \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) - \cos(\alpha_4) - m = 0 \\ \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) - \cos(5\alpha_4) = 0 \\ \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) - \cos(7\alpha_4) = 0 \\ \cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) - \cos(11\alpha_4) = 0 \end{cases}, \tag{14}$$

with $m = \frac{3r\pi}{4}$.

The resolution of this class of algebraic equations is generally carried out via the Newton–Raphson iterative method [15,16,24]. Nevertheless, this method needs an initialization as close as possible to the solution. To overcome this constraint, another resolution method, based on the resultant theory and symmetric polynomials, was developed in [20]. This technique allows the determination of all possible solutions without any preliminary testing. In the case of the voltage leg imposed as the waveform of Figure 4, all possible switching angles and the THD related to the corresponding output voltage are depicted respectively in Figure 5a and Figure 5b. It appears that some range of modulation index exhibits double solutions. Therefore, the selection

of the optimal one giving the lower THD is possible (Figure 5c). In order to confirm the validity of the SHE strategy, a test is carried out for $r = 0.8$. The switching angles, resulting from Figure 5c and related to $r = 0.8$, lead to the phase voltage and their harmonics spectrum, shown respectively in Figure 6a and Figure 6b. Figure 7 gives the magnitude of the cancelled harmonics and the variation of the fundamental amplitude and its desired value according to r.

By analyzing Figures 5–7 for SHE-PWM, it is observed that:

- As opposed to the Newton–Raphson method [16,24], the resultant theory method makes it possible to obtain all the possible solutions.
- For $r < 0.57$, the system of Eq. (14) does not admit any solution (Figure 5a).
- For the modulation index r leading to multiple solutions, the inverter is controlled by those that give the weakest THD (Figure 5c).
- The elimination of harmonics 5, 7, and 11 is ensured for all values of r (Figure 7a).
- The fundamental voltage follows the desired value (Figure 7b).

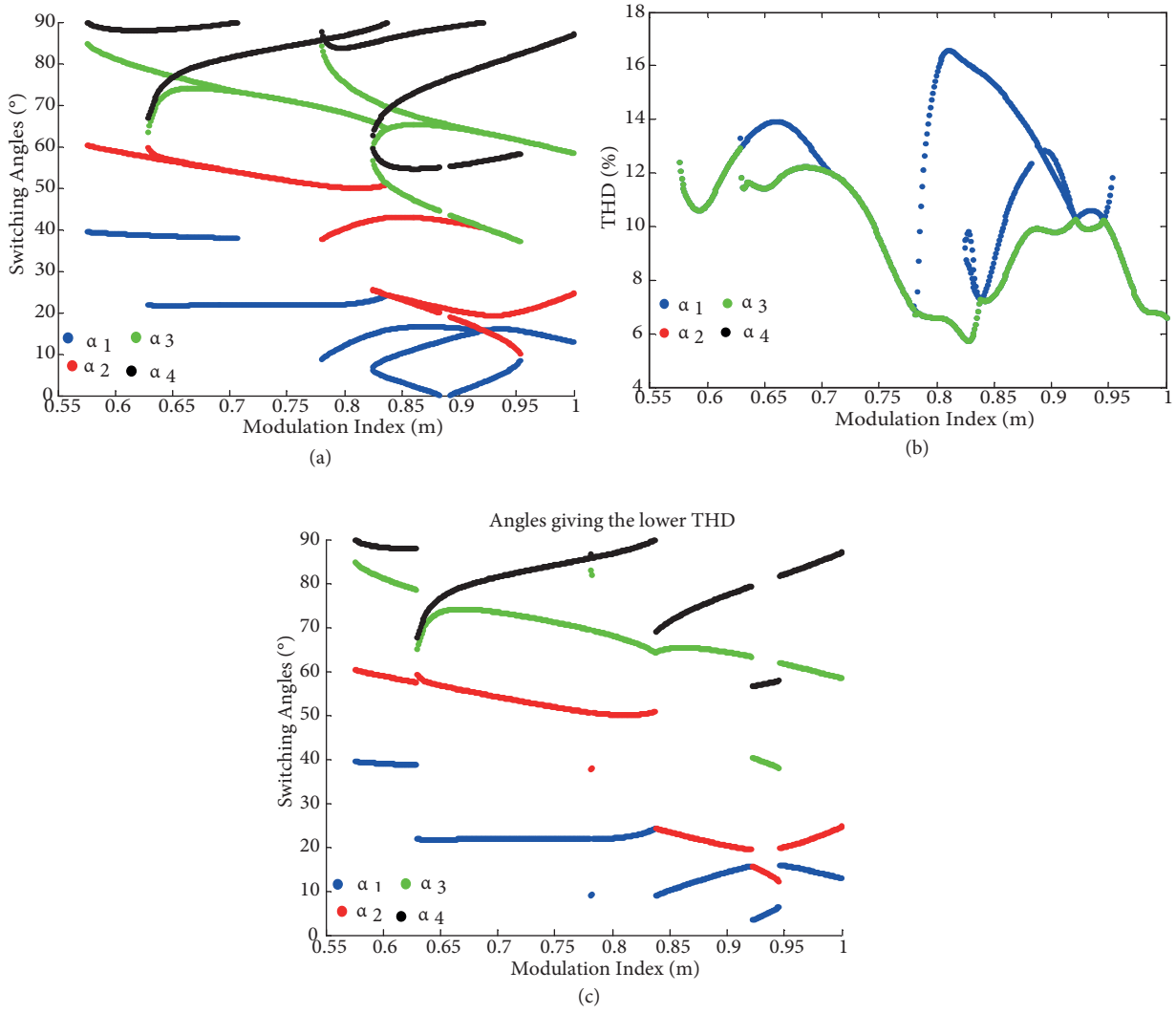

Figure 5. Switching angles and their THD for the 7-level inverter.

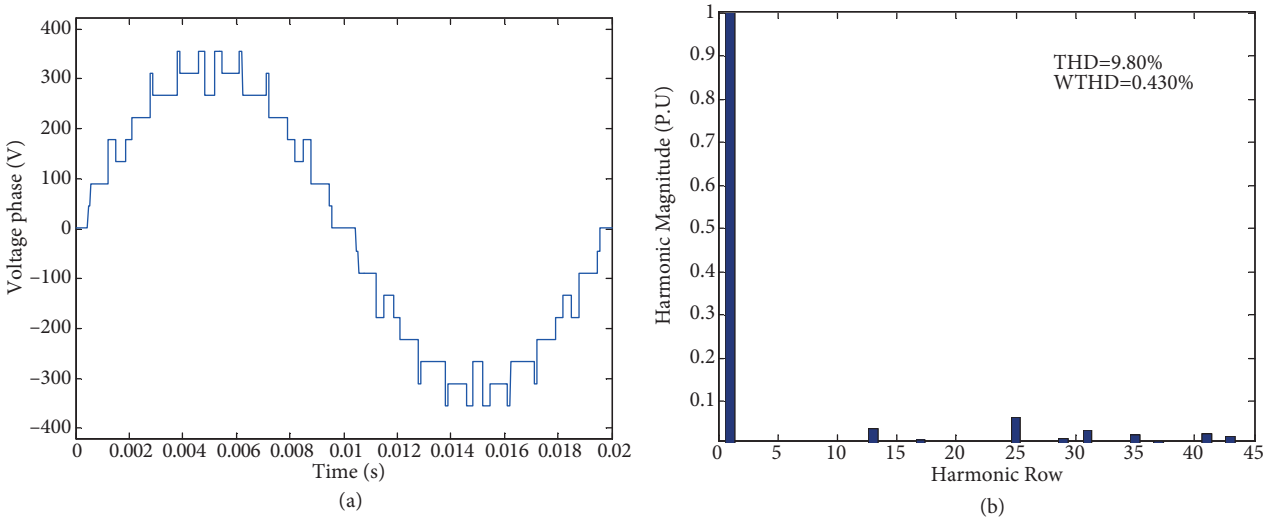

Figure 6. Output voltage waveform for a 7-level inverter controlled by the SHE-PWM and its harmonic spectrum (m = 0.8).

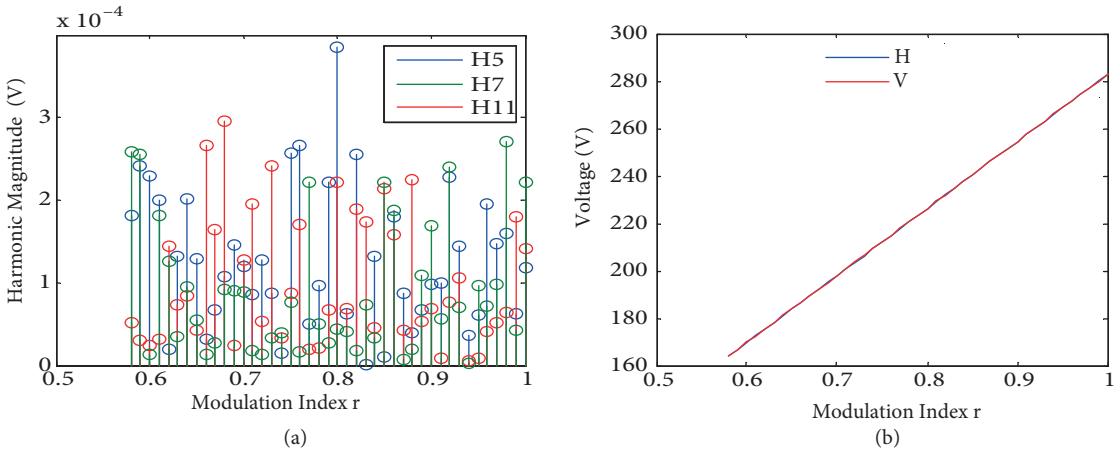

Figure 7. a) Magnitude of the cancelled harmonics range; b) magnitude of the fundamental voltage.

4. Proposed DC-link balancing technique

In the previous section, the 7-level inverter, driven by the SHE-PWM, was studied in detail. For this section, it supplies an IM. The DC input voltage inverter is generated by the PV array (Figure 8).

In order to feed the inverter by regular voltage, a buck-boost DC-DC converter is associated with the output of the PV array [28]. The maximum power point tracking is done all the time using the perturb and observe algorithm [29,30]. The electrical model of the PV cell with 5 parameters is shown in Figure 9. PV cells are regrouped in large units called PV modules, which are further interconnected in a parallel-series configuration to form a PV array or PV generator, in order to reach a high voltage at the terminals. The current I is given as in Eq. (15):

$$I = I_{ph} - I_0 \exp\left[\left[\frac{q}{A.K.T}(V + R_s I)\right] - 1\right] - \frac{V + R_s I}{R_{sh}} \tag{15}$$

Here, I_{ph} is the photocurrent depending on the solar radiation and the cell temperature, and I_0 is the cell

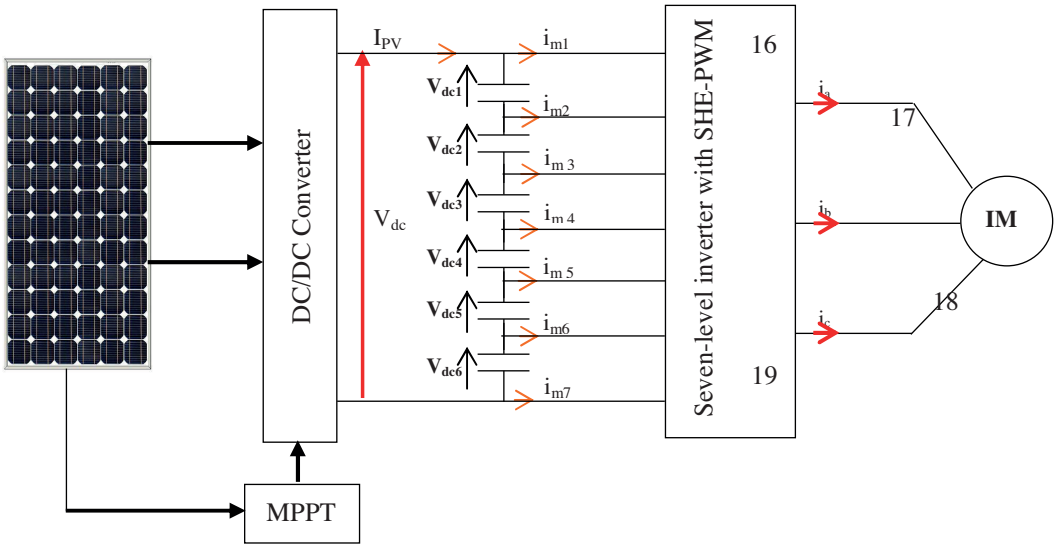

Figure 8. PVG – 7-level inverter – induction motor.

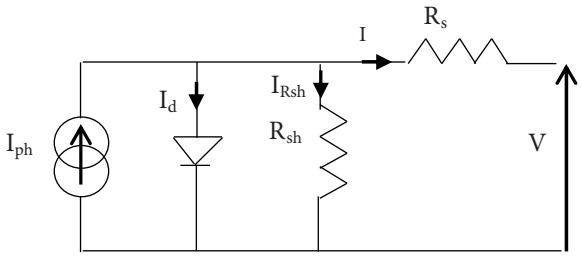

Figure 9. A PV cell equivalent circuit.

reverse saturation current varying with temperature. R_s and R_{sh} are respectively the series and the shunt parasitic resistances. K is the Boltzmann constant, q the charge of electron, A the ideality factor, and T the cell temperature.

Figures 10a–10c illustrate power–voltage and current–voltage characteristics for different values of temperature and solar irradiance.

The power produced by a PV system varies with the amount of sun shining on the module and, to a lesser extent, module temperature. The temperature is held constant, this power variation results in a variable current at a fixed voltage. Increasing temperature reduces PV module output power.

Figure 11 shows the capacitor voltages after connecting the PVG-DC-DC converter, 7-level inverter, and IM together. All capacitor voltages are unbalanced.

In order to keep the 6 capacitor voltages as equal as possible, the switching control strategy for multilevel inverter devices is used.

Among the 343 output voltage vectors of the inverter, only 90 can be obtained by different combinations of switching. Therefore, the 7-level inverter switching can be classified into 3 groups. The first one represents the last hexagon of Figure 3.

It is formed by 36 vectors that do not connect any of the 3 phases to the common capacitor's potential, and so the capacitor voltages remain unaffected.

The second one is the zero vector value obtained via 7 redundant switching states. They have no effect on the divider behavior.

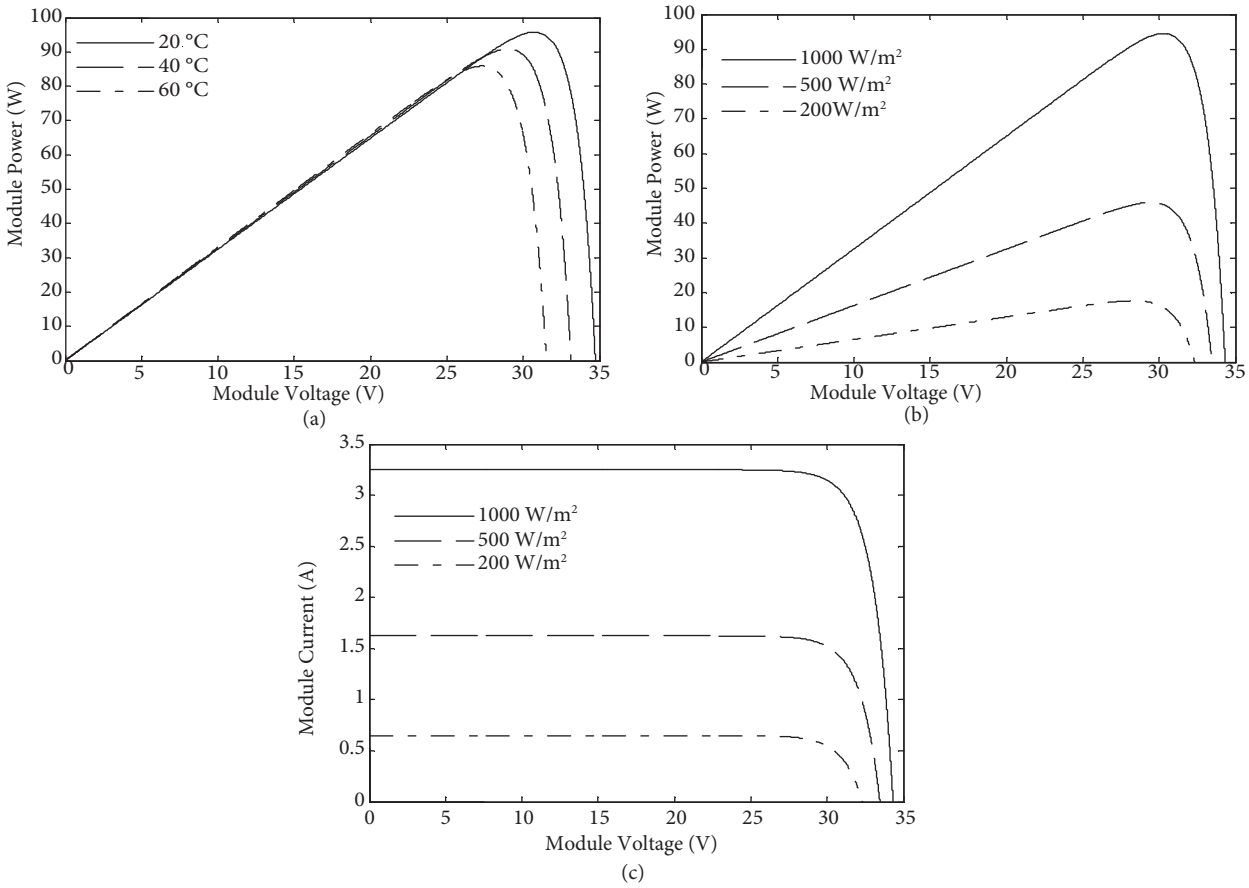

Figure 10. The 5 parameters model behavior of the PV-module.

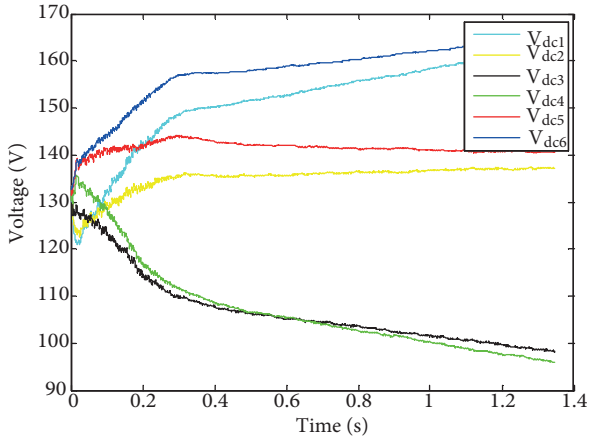

Figure 11. DC-link voltages without balancing algorithm.

On the contrary, the third group contains 90 vectors corresponding to the 5 remaining hexagons (1, 2, 3, 4, and 5) and representing 300 switching states. In this group, each vector voltage can be obtained by more than one switching combination (redundancy). Table 2 gives more information about this group. In fact the particularity of this group involves the fact that each different switching state has a different effect on the 6

capacitors' state (charge or discharge). Indeed, the different switching states of this group force the load current to flow through different paths. Thus, the direction of current through the DC-link capacitors is different, and variation among DC-link capacitors' voltages is different. Therefore, to make as effective use as possible of these 90 vectors for balancing the DC-link capacitors, it is necessary to study in detail the effect of each one. The study is more complicated than those of 3- and 5-level inverters because of the huge number of switching states to study (i.e. 300).

Table 2. Number of switching states for each group of V_s.

Hexagon	Number of vectors V_s	Number of redundancies	Number of switching states
1	6	6	36
2	12	5	60
3	18	4	74
4	24	3	72
5	30	2	60

Indeed, using the matrix model of the inverter developed in Section 1, the effect of AC load current i_a and i_b on the capacitor currents is established (Eq. (9)).

According to their sign, the states of capacitors (charge or discharge C_i) can be known relative to the 300 switching states. To explain the technique used, an example concerning the output vector (–5, –5) is explained. This vector is part of hexagon 5, and it can be obtained through 2 switching states (redundancies a and b).

Moreover, the capacitor currents (Eq. (9)) are influenced by switching states via the coefficients a_{ij}. Table 3 gives the values for the 2 redundancies through Eqs. (10) and (11). These obtained a_{ij} are then substituted into Eq. (9) of the capacitor currents. The analysis has shown that the 6 capacitor currents depend only on the variable E, which stands for $(-i_a\ -i_b)$, as shown in Table 4.

Table 3. a_{ij} values for vector (–5, –5).

V_s		U_{AC}	U_{BC}	V_{AM}	V_{BM}	V_{CM}	i_{c1}	i_{c2}	i_{c3}	i_{c4}	i_{c5}	i_{c6}
9	a	–5	–5	0	0	5	–5E	E	E	E	E	E
	b	–5	–5	1	1	6	E	E	E	E	E	–5E

Table 4. Values of capacitor current signs for vector (–5, –5).

V_s		U_{AC}	U_{BC}	a_{11}	a_{12}	a_{21}	a_{22}	a_{31}	a_{32}	a_{41}	a_{42}	a_{51}	a_{52}	a_{61}	a_{62}
9	a	–5	–5	5	5	–1	–1	–1	–1	–1	–1	–1	–1	–1	–1
	b	–5	–5	–1	–1	–1	–1	–1	–1	–1	–1	–1	–1	5	5

The analysis of 90 output vectors allows for sorting them into 15 different groups. Indeed, each group has the same effect on the capacitor voltages; it is formed by 6 different output vectors.

Based on the results of this study, an algorithm is developed in order to minimize the difference between the 6 capacitor voltages by selecting the suitable switching redundancy of the actual switching states among the switching states of the group concerned (for this example, Group 3). The switching state is selected based on the following rule: load the unloaded capacitor and unload the loaded one. Otherwise, for the DC-link 7-level inverter, 720 deviations of the 6 capacitor voltages are possible, which would further complicate the study. The developed algorithm has the capacity to find the solution for all existing unbalanced cases.

As an example, the following case of DC-link voltage unbalance is proposed:

$V_{dc1} < V_{dc2} < V_{dc3} < V_{dc4} < V_{dc5} < V_{dc6}$; the actual switching state obtained via SHE-PWM is (0 0 5), related to the voltage vector (–5, –5).

From Table 4, if $E > 0$, the actual switching state (0 0 5) is substituted with (1 1 6), which conducts charging C_1 and discharging C_6. In the opposite case, the actual switching combination is used again. The procedure is applied for all 300 switching states using the SHE-PWM signal.

At the end of the operation, another leg voltage waveform that provides the same modulated voltage waveform and the same harmonics spectrum is obtained (Figure 6b).

The proposed capacitor balancing method is tested by simulation using both MATLAB and Simulink. The PVG-DC-DC converter cascade operates a dynamic load related to the induction motor (Appendix).

The DC output voltage is kept stable at 800 V. Hence, the voltage reference of each capacitor is 133.33 V. The capacitance values are fixed at 20 mF.

Figure 12a shows the waveforms of the 6 capacitor voltages when the developed algorithm is applied with effect from time t = 0.3 s.

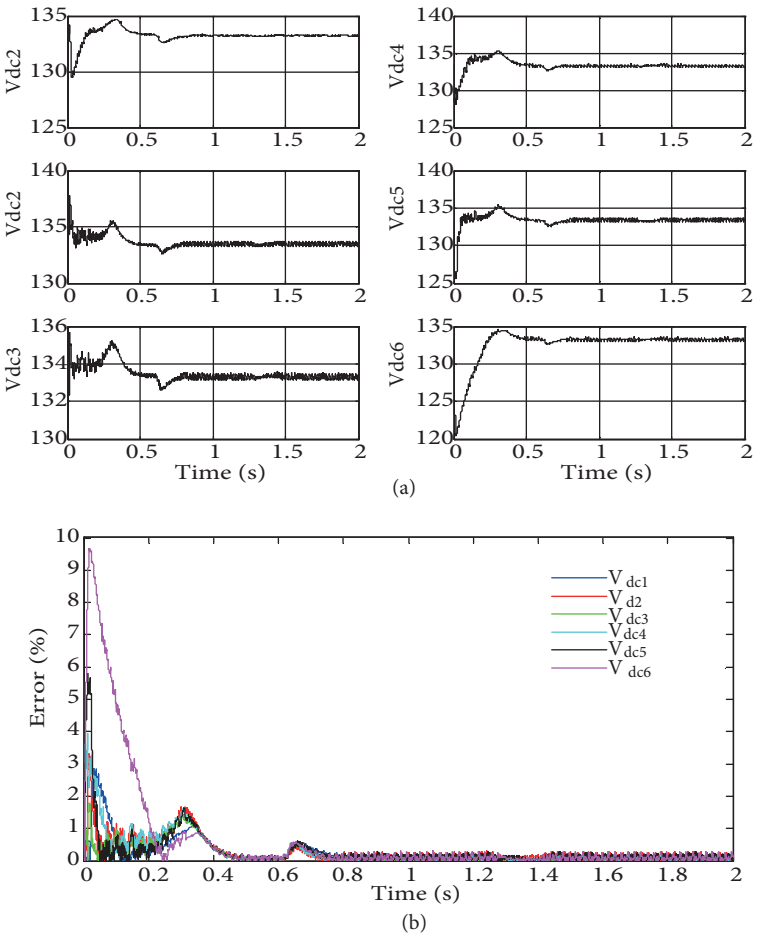

Figure 12. a) The V_{dci} voltages; b) the relative error ΔV_{dci}.

It appears clearly that the 6 voltages diverge from their reference before the balancing algorithm is applied, and they start to converge toward their desired value once the algorithm is used. The voltage deviations (ΔV_{dci})

of voltage capacitor V_{dci}, given in Figure 12b, highlight the previous observations. Indeed, the input DC-link 7-level inverter takes the form given by Figure 13a.

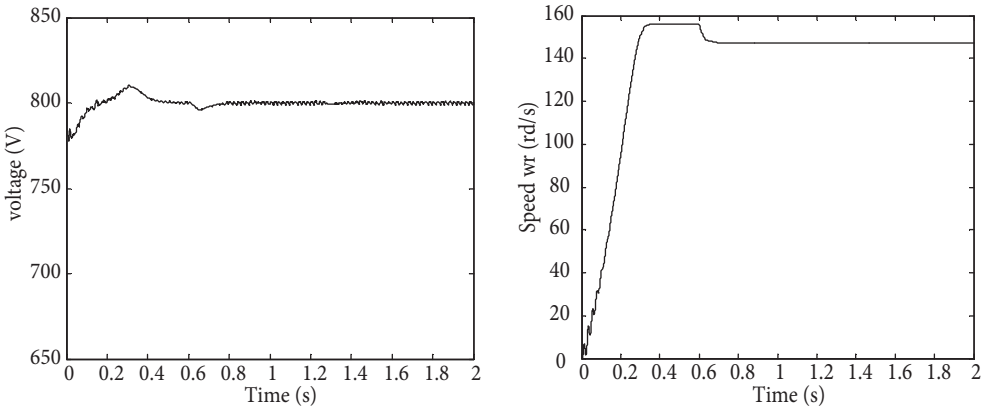

Figure 13. a) The output voltage PVG; b) induction motor speed.

The capacitor voltages are kept balanced even when the nominal load torque is applied at 0.6 s (Figure 13b). Thus, the capacitor voltages maintain balance while keeping the SHE-PWM proprieties.

5. Conclusion

Multilevel inverters suffer from capacitor voltage imbalance problems. Many techniques have been proposed to solve this problem. One of these techniques is the redundant states method generally associated with SV-PWM.

In this paper, both optimizations of switching angles of a 7-level output waveform inverter using SHE-PWM and self-DC-link voltages balance are investigated. Indeed, the programmed PWM eliminates harmonics rows 5, 7, and 11, with good control of the fundamental based on the resultant theory method. Moreover, a DC-link balancing technique is developed using the redundant switching states of the inverter. In the case of the 7-level inverter, the study can be quite laborious, since it concerns 300 switching states and 720 DC-link unbalance deviations.

In order to simplify the analysis, the inverter is represented by its equivalent matrix model. The obtained results have shown that the DC-link balancing can be involved while maintaining the SHE-PWM performance. The improvement of this technique comes from the fact that balancing the 7-level inverter DC capacitors is carried out with lower device switching frequency due to SHE-PWM, and without any auxiliary circuit. Therefore, energy losses are reduced and hardware costs are decreased for the PV system.

References

[1] Solar Energy Perspectives. Paris, France: OECD/IEA, 2011.

[2] Gow JA, Manning CD. Photovoltaic converter system suitable for use in small scale stand alone or grid connected application. IEE P-Elect Pow Appl 2000; 147: 535-543.

[3] Valan RM, Manoharan PS, Ravi A. Simulation and an experimental investigation of SVPWM technique on a multilevel voltage source inverter for photovoltaic systems. Int J Elec Power 2013; 52: 116-131.

[4] Kjær SB, Pedersen JK, Blaabjerg F. Power inverter topologies for photovoltaic modules. In: IEEE 2002 Industry Applications Society Conference; 13–18 October 2002; Pittsburgh, PA, USA. Piscataway, NJ, USA: IEEE. pp. 782-788.

[5] Hill WA, Harbourt CD. Performance of medium voltage multilevel inverters. In: IEEE 1999 Industry Applications Society Conference; 3–7 October 1999; Phoenix, AZ, USA. Piscataway, NJ, USA: IEEE. pp. 1186-1192.

[6] Tolbert LM, Peng FZ, Habetler TG. Multilevel converters for large electric drives. IEEE T Ind Appl 1999; 35: 36-44.

[7] Rodriguez J, Lai JS, Peng FZ. Multilevel inverters: a survey of topologies controls and applications. IEEE T Ind Electron 2002; 49: 724-738.

[8] Ounejjar Y, Al-Haddad K, Gregoire LA. Packed U cells multilevel converter topology: theoretical study and experimental validation. IEEE T Ind Electron 2011; 58: 1294-1306.

[9] Schweizer M, Friedli T, Kolar JW. Comparative evaluation of advanced three-phase three-level inverter/converter topologies against two-level systems. IEEE T Ind Appl 2013; 60: 5515-5527.

[10] Nabae A, Takahashi I, Akagi H. A new neutral-point-clamped PWM inverter. IEEE T Ind Appl 1981; 17: 518-523.

[11] Dixon J, Morán L. High-level multistep inverter optimization using a minimum number of power transistors. IEEE T Power Electr 2006; 21; 330-337.

[12] Rabinovici R, Baimel D, Tomasik J, Zuckerberger A. Series space vector modulation for multi-level cascaded H-bridge inverters. IET Power Electron 2010; 3: 843-857.

[13] Yao W, Hu H, Lu Z. Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter. IEEE T Power Electr 2008; 23: 45-51.

[14] Gupta KK, Jain S. Algorithm for asymmetric source configuration in a newly constructed multistring multilevel inverter topology. In: 6th IET 2012 International Conference on Power Electronics Machines and Drives; 27–29 March 2012; Bristol, UK. Stevenage, UK: IET. pp. 1-6.

[15] Patel HS, Hoft RG. Generalized technique of harmonics elimination and voltage control in thyristor inverter. IEEE T Ind Appl 1973: 310-317.

[16] Imarazene K, Chekireb H, Berkouk EM. Control of seven-level optimized voltage inverter based on selective harmonics elimination and artificial neural network. Mediterranean Journal of Measurement and Control 2007; 3: 143-150.

[17] Imarazene K, Berkouk EM, Chekireb H. Selective harmonics elimination: PWM method versus optimized total harmonic distortion. In: International Conference on Power Engineering Energy and Electrical Drives; 13–15 May 2013; İstanbul, Turkey. Piscataway, NJ, USA: IEEE. pp. 886-893.

[18] Imarazene K, Berkouk EM, Chekireb H. Selective harmonics elimination PWM with sel-balancing capacitors in three-level inverter. In: IET 6th International conference on power electronics machines and drives; 27–29 March 2012; Bristol, UK. Stevenage, UK: IET. pp. 1-6.

[19] Napoles J, Leon JI, Portillo R, Franquelo LG, Aguirre MA. Selective harmonic mitigation technique for high-power converters. IEEE T Ind Electron 2010; 57: 2315-2323.

[20] McKenzie KJ. Eliminating harmonics in a cascade H-bridges multilevel inverter using resultant theory, symmetric polynomials and, power sums. MSc, University of Tennessee, Knoxville, TN, USA, 2004.

[21] Halim WA, Rahim NA, Azri M. Selective harmonic elimination for a single-phase 13-level TCHB based cascaded multilevel inverter using FPGA. J Power Electron 2014; 14: 488-498.

[22] Dahidah MSA, Konstantinou G, Flourentzou N, Agelidis VG. On comparing the symmetrical and non-symmetrical selective harmonic elimination pulse-width modulation technique for two-level three-phase voltage source converters. IET Power Electron 2010; 3: 829-842.

[23] Shu Z, Ding N, Chen J, Zhu H, He X. Multilevel SVPWM with DC-link capacitor voltage balancing control for diode-clamped multilevel converter based STATCOM. IEEE T Ind Electron 2013; 60: 1884-1896.

[24] Imarazene K. Etude de la commande par élimination d'harmoniques des onduleurs multiniveaux avec équilibrage des tensions du bus continu. PhD, Polytechnic National School (ENP), Algiers, Algeria, 2011 (in French).

[25] Rahim NA, Elias MFM, Hew WP. Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing. IEEE T Ind Electron 2013, 60: 2943-2956.

[26] Sharifzadeh M, Vahedi H, Sheikholeslami A, Labbe PA, Al-Haddad K. Hybrid SHM-SHE modulation technique for four-leg NPC Inverter with DC capacitors self-voltage-balancing. IEEE T Ind Electron 2015; 62: 4890-4899.

[27] Strzelecki R, Benysek G, Rusiński J, Kot E. Analysis of DC link capacitor voltage balance in multilevel active power filters. In: EPE 2001 European Conference on Power Electronics and Applications; 27–28 August; Graz, Austria. Brussels: EPE, pp. 1-8.

[28] Peftitsis D, Adamidis G, Bakas P, Balouktsis A. Photovoltaic system MPPT tracker investigation and implementation using DSP engine and buck-boost DC-DC converter. In: International Conference on Power Electronics and Motion Control; 1–8 September 2008; Poznan, Poland. Piscataway, NJ, USA: IEEE. pp. 1840-1846.

[29] Ozdemir S, Altin N, Sefa I. Single stage three level grid interactive MPPT inverter for PV systems. Energ Convers Manage 2014; 80; 561-572.

[30] Altin N, Ozdemir S. Three-phase three-level grid interactive inverter with fuzzy logic based maximum power point tracking controller. Energ Convers Manage 2013; 69; 17-26.

Appendix

The squirrel-cage induction motor: 1.5 kW, 2 pairs of poles, 1420 turns/min, 50 Hz.

$R_s = 4.85\Omega$, $R_r = 3.805\ \Omega$, $L_s = 0.274$ H, $L_r = 0.274$ H, M = 0.258 H, J = 0.031 kgm^2, $f = 0.00114$ Nms.