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A generalized algorithm for space vector modulation in multilevel inverters

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Abstract: This paper proposes a new space vector pulse width modulation (SVPWM) algorithm for multilevel inverters that achieves a minimum number of switch state changes in one sampling cycle in order to reduce switching losses. The algorithm can be implemented with minimum computational burden and it does not require any look-up tables. The essence of the technique is to exploit the redundancy of switching functions in the implementation of the voltage vectors and dividing the entire vector space into three sectors in which switching functions have some common features. Careful observations showed that these common features lend themselves to be expressed as closed form analytical equations that can be readily implemented in an embedded digital platform. The concepts are developed using a three-level inverter. However, generalized equations are given so that the proposed technique can be applied to inverters with an arbitrary number of levels.

Key words: Multilevel inverter, DC/AC conversion, pulse width modulation, space vector modulation

1. Introduction

Although technical issues such as implementation complexity and dc bus voltage balancing requirements remain major problems, the reduced voltage and current harmonics at reasonably low switching frequency and the reduced voltage rating requirement for controllable switches make multilevel inverters an attractive choice for high power applications [1–4]. Space vector pulse width modulation (SVPWM) offers better utilization of the dc bus and viable implementation for embedded digital platforms. SVPWM in multilevel inverters is more complicated due to the higher number of switching functions and the redundancy among these functions. As the number of levels increases the complexity increases in parallel. Recently, many publications have appeared in the literature to address different issues of SVPWM in multilevel inverters [5–10].

This paper proposes a new algorithm that ensures a minimum number of switch state changes in one sampling cycle in order to reduce switching losses. The algorithm can be implemented with minimum computational burden and it does not require any look-up tables. Dc bus voltage level balancing has not been targeted throughout the algorithm. For this reason it would suit applications where dc bus voltage balancing is not required explicitly. These applications could be reactive power flow control or a back-to-back connected multilevel rectifier/inverter system. Switching losses strongly depend on the load power factor angle. In particular, discontinuous PWM allows switching losses to be reduced by 50% depending on the power factor of the load [9]. In addition, adaptive space vector PWM proposed in [10] allows switching loss reduction and the performance is strongly tied with the load power factor. With discontinuous PWM, the inverter has minimum switching loss at unity power factor. For lagging and leading power factor values, switching losses have a

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tendency to fluctuate by lag or lead angle and it depends on one of three PWM schemes proposed in [9]. Until 45° of lead or lag angle losses increase as the power factor angle. In adaptive space vector PWM, similar behavior is observed as reported in [10]. The only difference is the rise of switching losses continues until 75° of power factor angle.

In this work, for the sake of simplicity, a three-level inverter has been investigated. However, generalized equations have been given so that the proposed technique can be applied to inverters with an arbitrary number of levels. Section 2 gives a brief overview of SVPWM for multilevel inverters. Section 3 summarizes the proposed method. The coordinate system on which the method is based is introduced in Section 4. Section 5 gives the generalization efforts along with details about the algorithm. Verification of the algorithm is given in Section 6.

2. SVPWM for multilevel inverters

The implementation steps of a typical space vector modulation scheme for multilevel inverters are given below.

2.1. Selection of three adjacent vectors and associated duty ratios for a given reference voltage vector

This is quite straightforward for a 2-level inverter. As the number of levels increases, however, the number of vectors increases and the selection process becomes more cumbersome. An elegant method for selecting three adjacent vectors of the reference vector and calculation of the duty ratio of each vector for a given reference voltage vector was proposed in [4] through a new coordinate transformation. The same method will be adopted in this paper for this part of the problem.

2.2. Selection of the switching functions

Figure 1 shows the switching vectors for a three-level inverter. As shown in the figure, two layers of hexagons exist and a vector on the inner hexagon can be implemented with two different switching functions. On the other hand, a vector in the outer hexagon can be implemented with only one switching function. In general, as the hexagons get larger in size, the number of ways to create each vector is reduced. The vector at the origin can be created in m ways for an m-level inverter, while the outermost vectors can only be produced by one combination of switching functions. The redundancy among the switching functions adds freedom to the implementation strategy. Some researchers have exploited this freedom to reduce common mode voltage [11–13]. Some others have used it to balance dc bus voltage levels [14]. In [15], the authors analyzed the redundancy for the optimized switching sequences in terms of minimum loss and harmonics for SVPWM and carrier-based PWM schemes. In a recent work [16], researchers implemented a similar idea where algorithm simplicity is the major goal. However, the switching functions they used are still obtained by a heuristic approach, but they managed to implement the algorithm experimentally and show the effectiveness of the approach in inverter efficiency and computational load.

In this paper, our goal is to implement a minimum loss switching strategy in a computationally efficient way by exploiting redundant switching states. Our approach is general and can be applied to inverters with any number of levels. The most important contribution of the patented approach [17] comes in forming the switching functions by closed form analytical equations.

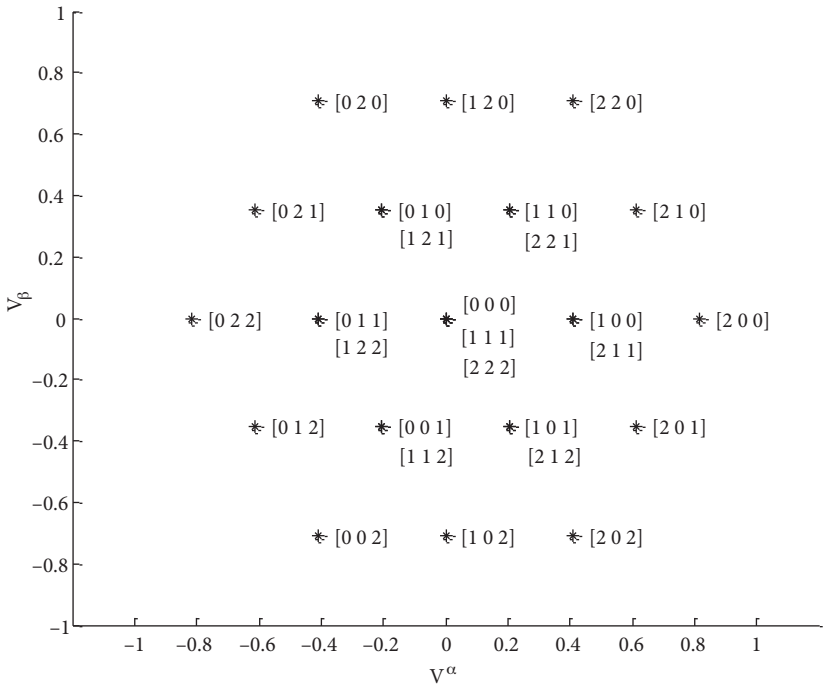


Figure 1. The voltage vectors of a three-level inverter in $\alpha\beta$ coordinates. The "*" sign indicates the tip of each vector, the bracketed numbers next to the "*" sign indicate possible switching functions to implement the associated vector.

2.3. Application of the selected vectors in a proper order

Three selected adjacent vectors are applied in a certain order by three different switching functions. If we aim for SVPWM with minimum loss, then a proper order in the application of the vectors should be maintained. A major goal in ordering three vectors is to get the lowest number of switch state changes as the implemented voltage vector moves. The proposed algorithm allows switch state changes only in one leg of the inverter when we move from one vector to the next.

3. Proposed minimum loss SVPWM strategy [17]

After close examination of the switching functions given in Figure 1, it has been observed that it is possible to make a selection among the redundant switching functions so that the entire vector space can be divided into three sectors as shown in Figure 2. The most striking feature of switching functions inside the same sector is that switch positions for one phase leg always remain constant. For instance, no switching occurs on phase A leg during sector A and no switching occurs on phase B leg during sector B and so on. Here, it should be emphasized that the number of sectors does not depend on the number of levels but it depends on the number of phase legs.

Fundamentally, space vector modulation is accomplished by using three adjacent vectors that form an equilateral triangle. The angular position and length of the reference vector dictates the triangle to be used during modulation. The minimum-loss switching scheme requires a minimum number of switch state changes when we move from one vector to another on a specific triangle. Careful examination of each triangle in Figure 2 indicates that each sector has a unique switch state change that is common to all triangles in the associated sector. This observation is shown in Figure 3.

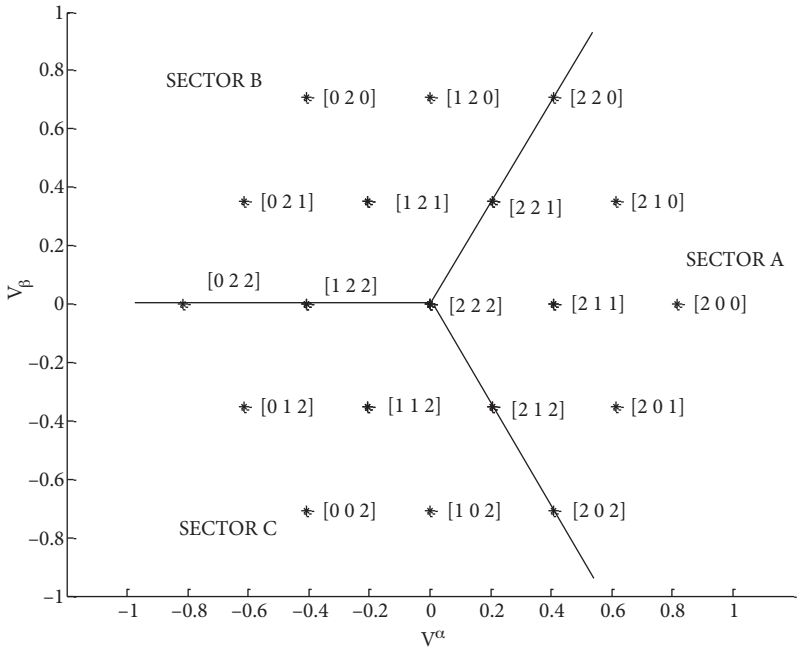


Figure 2. The sectors in the vector space after eliminating redundant switching functions for the three-level inverter.

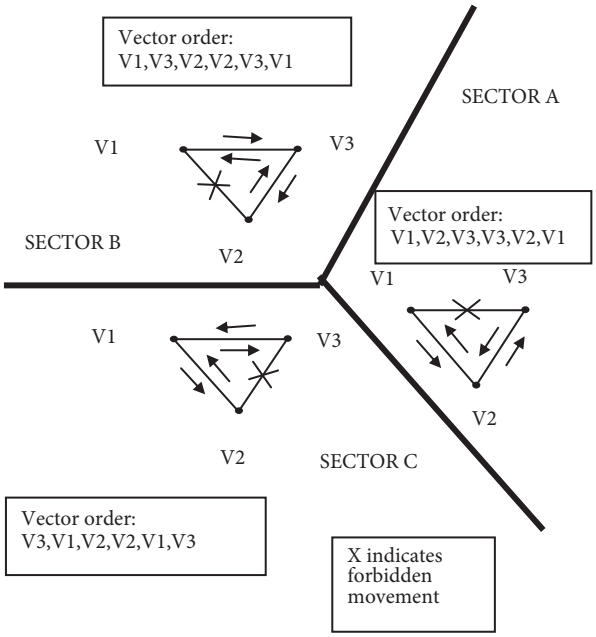


Figure 3. Common switch state changes in each sector giving minimum switching losses.

4. A nonorthogonal coordinate system

Implementing a space vector algorithm for multilevel inverters is complicated when we use a conventional orthogonal coordinate system as shown in Figures 1–3. A new coordinate system that is based on oblique basis vectors was introduced in [4]. From now on, we will refer to this coordinate system as a *gh* coordinate system on which minimum loss strategy will be based. The basis vector of the *gh* coordinate system is [4]

$$\left\{\vec{g}(v_{ab}, v_{bc}, v_{ca}), \vec{h}(v_{ab}, v_{bc}, v_{ca})\right\} = \left\{ \begin{bmatrix} V_{dc} \\ 0 \\ -V_{dc} \end{bmatrix}, \begin{bmatrix} 0 \\ V_{dc} \\ -V_{dc} \end{bmatrix} \right\}. \quad (1)$$

Figure 4 shows the space vectors tips for a three-level inverter in the *gh* coordinate system. A transformation matrix from the *abc* coordinate system to the *gh* coordinate system is

$$T_{abc-gh} = \frac{m-1}{V_{dc}} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \end{bmatrix}, \quad (2)$$

where m is the number of levels and V_{dc} is the dc bus voltage.

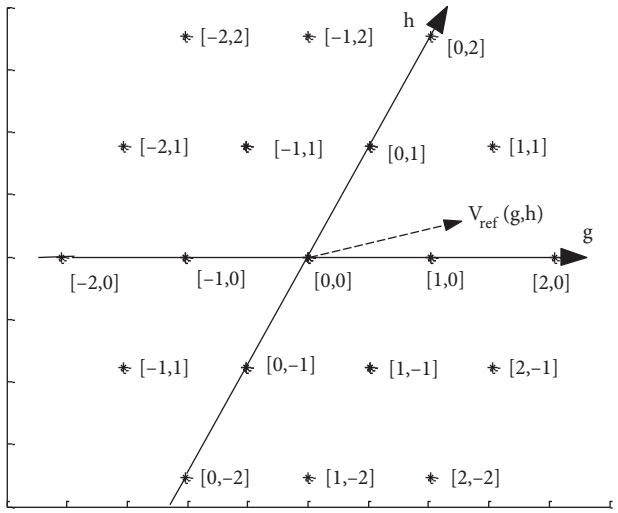


Figure 4. Illustration of voltage space vector tips in the *gh* coordinate system.

5. Generalization of the proposed method

After presenting the principles of the proposed method, generalized equations are given here for a three-phase m level inverter. As mentioned before, space vector modulation for a multilevel inverter is implemented in three major steps. The first step is to find a suitable triangle and the associated duty ratios by using reference vector information, then to make a selection among redundant switching functions, and finally to apply the selected functions in proper order.

In this step, first the reference voltage is converted from the *abc* coordinate system to the *gh* coordinate system by the transformation matrix given in (2). Then the coordinates are rounded upward and downward to the next integer number. This process defines a rhombus in which the reference vector lies. The triangle of interest is found by determining the location of the reference vector relative to the minor diagonal of the rhombus. Final selection is made between the two triangles that comprise the rhombus by comparing reference voltage vector coordinates with the coordinates of the vertices of the associated triangles. After deciding on the triangle in which the reference vector lies, duty ratios are calculated by the same approach used in the two-level SVPWM algorithm [18]. The details of finding of the appropriate triangle and the associated duty ratios are given in [4].

5.1. Making a selection among the redundant switching functions

The previous step eliminates all triangles except the one in which the reference vector resides. This step focuses on eliminating redundant switching functions by using the criteria dictated by the minimum switching loss requirement. This step and the next one are the major contributions of this investigation in terms of developing the minimum loss SVPWM algorithm. The selection of the most suitable switching function among the redundant switching functions requires the following tasks be performed.

Computing the location of the triangle in the polar coordinate system

Coordinates of the triangle vertices determined in the previous step in the gh coordinate system can be converted into the polar coordinate system where each point can be given in terms of θ, r_v. The origin of the polar coordinate system is the same as that for the gh coordinate system, with θ measured relative to the g axis. The angle is given by

$$\theta = \tan^{-1}\left(\frac{h\sin(2\pi/3)}{g + h\cos(\pi/3)}\right), \tag{3}$$

and the radius is given by

$$r_v = \left|\frac{h}{\sin\theta}\sin\left(2\pi/3\right)\right|. \tag{4}$$

5.1.1. Finding the two hexagon levels between which V_{ref} lies

The tips of the voltage space vectors in a multilevel inverter form concentric hexagons. Each new level adds a new hexagon. The vertices of the triangles determined in the first step lie on two hexagons. This step determines the associated hexagon for each vertex of the triangle. This essentially gives us two voltage levels that we use during modulation. The following logic is used for every vertex of the triangle to find its level:

Get (g,h) coordinate of the vertices.

If g=0 then level=abs(h),

Else if h=0 then level=abs(g),

Else if (g+h)=0 then level=abs(h),

Else level $=r_v$.

Application of the above algorithm to each vertex of the triangle yields three numbers indicating the level of the hexagons. The greatest one is taken as the triangle level,

$$k = Max(Level_1, Level_2, Level_3), \tag{5}$$

where k is the triangle level. $Level_1$, $Level_2$, $Level_3$ are the levels of each vertex in the triangle.

5.1.2. Determining the sector in which V_{ref} lies

The sector in which V_{ref} lies can be determined by the following logic:

Get (g,h) coordinates

If g>0 and (g+h)>0 then SECTOR A.

If g<0 and h>0 then SECTOR B.

If h<0 and (g+h)<0 then SECTOR C.

As indicated before, each vertex may have more than one switching function. Here we aim to find generalized equations that are functions of triangle level (k) and gh coordinates of the vertices.

For Sector A:

$$V_1 = \begin{bmatrix} k \\ |k-|g_1|| \\ |k-|g_1|-|h_1|| \end{bmatrix} V_2 = \begin{bmatrix} k \\ |k-|g_2|| \\ |k-|g_2|-|h_2|| \end{bmatrix} V_3 = \begin{bmatrix} k \\ |k-|g_3|| \\ |k-|g_3|-|h_3|| \end{bmatrix} \quad (6)$$

For Sector B:

$$V_1 = \begin{bmatrix} |k-|g_1|| \\ k \\ |k-|h_1|| \end{bmatrix} V_2 = \begin{bmatrix} |k-|g_2|| \\ k \\ |k-|h_2|| \end{bmatrix} V_3 = \begin{bmatrix} |k-|g_3|| \\ k \\ |k-|h_3|| \end{bmatrix} \quad (7)$$

For Sector C:

$$V_1 = \begin{bmatrix} |k-|g_1|-|h_1|| \\ |k-|h_1|| \\ k \end{bmatrix} V_2 = \begin{bmatrix} |k-|g_2|-|h_{21}|| \\ |k-|h_2|| \\ k \end{bmatrix} V_3 = \begin{bmatrix} |k-|g_3|-|h_3|| \\ |k-|h_3|| \\ k \end{bmatrix}, \quad (8)$$

where k is the triangle level and V_1, V_2, V_3 are switching functions for each vertex of the triangle. Each element of these switching functions is the switch position for each leg of the inverter. g_1, g_2, g_3 are g coordinates of triangle vertices. h_1, h_2, h_3 are h coordinates of triangle vertices. ||indicates an absolute value.

5.2. Applying the selected vector in proper order

As shown in Figure 3, each sector has a transition that should be avoided for minimum loss SVPWM. Determining the forbidden transition is quite straightforward if we make use of the gh coordinate system. This can be done as follows in each sector:

In sector A, take any two vertices and label their h coordinates as h_x and h_y. If $h_x - h_y \neq 0$ then the transition from V_x to V_y is allowed. Otherwise the transition is forbidden. Repeat this check until finding the forbidden transition. Once the forbidden transition is determined then label V_x as V_1 and V_y as V_3 and the remaining vertex as V_2. After that apply the vectors in the order of $V1 \rightarrow V_2 \rightarrow V_3 \rightarrow V_3 \rightarrow V_2 \rightarrow V_1$.

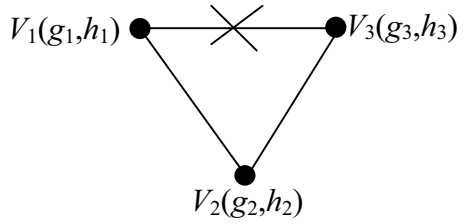
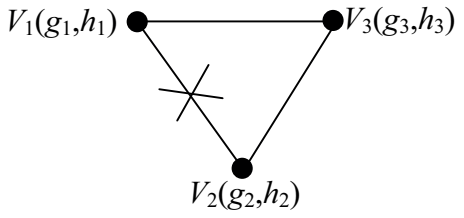
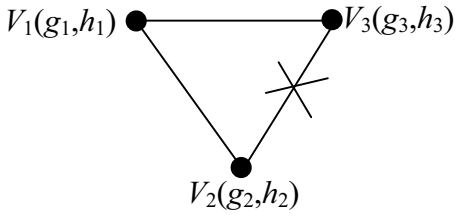
In sector B, take any two vertices and label their g coordinates as g_x and g_y and h coordinates as h_x and h_y. If $(g_x - g_y) + (h_x - h_y) \neq 0$ then the transition from V_x to V_y is allowed. Otherwise the transition is forbidden. Repeat this check until finding the forbidden transition. Once the forbidden transition is determined then label V_x as V_1 and V_y as V_2 and the remaining vertex as V_3. After that apply the vectors in the order of $V_1 \rightarrow V_3 \rightarrow V_2 \rightarrow V_2 \rightarrow V_3 \rightarrow V_1$.

In sector C, take any two vertices and label their g coordinates as g_x and g_y. If $g_x - g_y \neq 0$, then the transition from V_x to V_y is allowed. Otherwise the transition is forbidden. Repeat this check until finding the forbidden transition. Once the forbidden transition is determined then label V_x as V_2 and V_y as V_3 and the remaining vertex as V_1. After that apply the vectors in the order of $V_2 \rightarrow V_1 \rightarrow V_3 \rightarrow V_3 \rightarrow V_1 \rightarrow V_2$. The Table summarizes the switching function movements in each sector.

6. Verification of the algorithm

The proposed minimum loss SVPWM algorithm has been verified through PSPICE simulation and postprocessing. A three-phase three-level diode clamped inverter power circuit [19] has been set up by using the active and passive libraries of PSPICE. The modulator section, which hosts the SVPWM algorithm, is implemented through the Behavioral Models library. This library mainly includes controlled voltage and current sources

Table. A summary of switching function movements in each sector.

SECTOR- A	 X: Forbidden transition	$h_1 - h_2 \neq 0 \Rightarrow V_1 \rightarrow V_2$ allowed
		$h_2 - h_3 \neq 0 \Rightarrow V_2 \rightarrow V_3$ allowed
		$h_3 - h_1 = 0 \Rightarrow V_3 \rightarrow V_1$ forbidden
		Vector order in a switching cycle: $V_1 \rightarrow V_2 \rightarrow V_3 \rightarrow V_3 \rightarrow V_2 \rightarrow V_1$
		Note: if h remains unchanged from one vector to another then this movement is called a forbidden transition.
SECTOR- B	 X: Forbidden transition	$(g_1 - g_3) + (h_1 - h_3) \neq 0 \Rightarrow V_1 \rightarrow V_3$ allowed
		$(g_3 - g_2) + (h_3 - h_2) \neq 0 \Rightarrow V_3 \rightarrow V_2$ allowed
		$(g_2 - g_1) + (h_2 - h_1) = 0 \Rightarrow V_2 \rightarrow V_1$ forbidden
		Vector order in a switching cycle: $V_1 \rightarrow V_3 \rightarrow V_2 \rightarrow V_2 \rightarrow V_3 \rightarrow V_1$
		Note: if $(g_x - g_y) + (h_x - h_y)$ remains unchanged from vector V_x to vector V_y then this movement is called a forbidden transition.
SECTOR- C	 X: Forbidden transition	$g_2 - g_1 \neq 0 \Rightarrow V_2 \rightarrow V_1$ allowed
		$g_1 - g_3 \neq 0 \Rightarrow V_1 \rightarrow V_3$ allowed
		$g_3 - g_2 = 0 \Rightarrow V_3 \rightarrow V_2$ forbidden
		Vector order in a switching cycle: $V_2 \rightarrow V_1 \rightarrow V_3 \rightarrow V_3 \rightarrow V_1 \rightarrow V_2$
		Note: if g remains unchanged from one vector to another then this movement is called a forbidden transition.

such that their output values can be programmed in a flexible fashion. With behavioral modeling elements, it is possible to implement any mathematical function whose arguments are the nodes in the circuit. Figure 5 shows one line voltage output waveform generated by the three-level inverter. Figure 6 shows switching state variations of the three legs. As seen in Figure 6, only two switches are turned on and off in one switching cycle. The third leg remains inactive throughout the cycle. This indicates that the proposed algorithm is quite effective in reducing the overall switching loss of the inverter.

Figure 6 shows switching state variations of the three legs. As seen in Figure 6, one phase leg switches always remain off for 120° in one cycle of reference voltage. The controller selects another phase leg at the end of 120° and forces its switches to be inactive for another 120° . In the meantime, the switches of the active legs continue their operation. Detailed switching waveforms are given in Figure 7 by blowing up a certain section from Figure 6. As seen from the figure, phase C remains inactive while the others are switching such that only

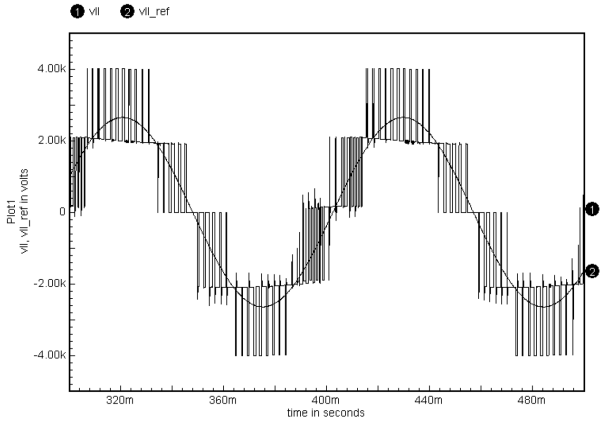


Figure 5. A line voltage waveform along with the reference voltage waveform according to the minimum loss SVPWM algorithm.

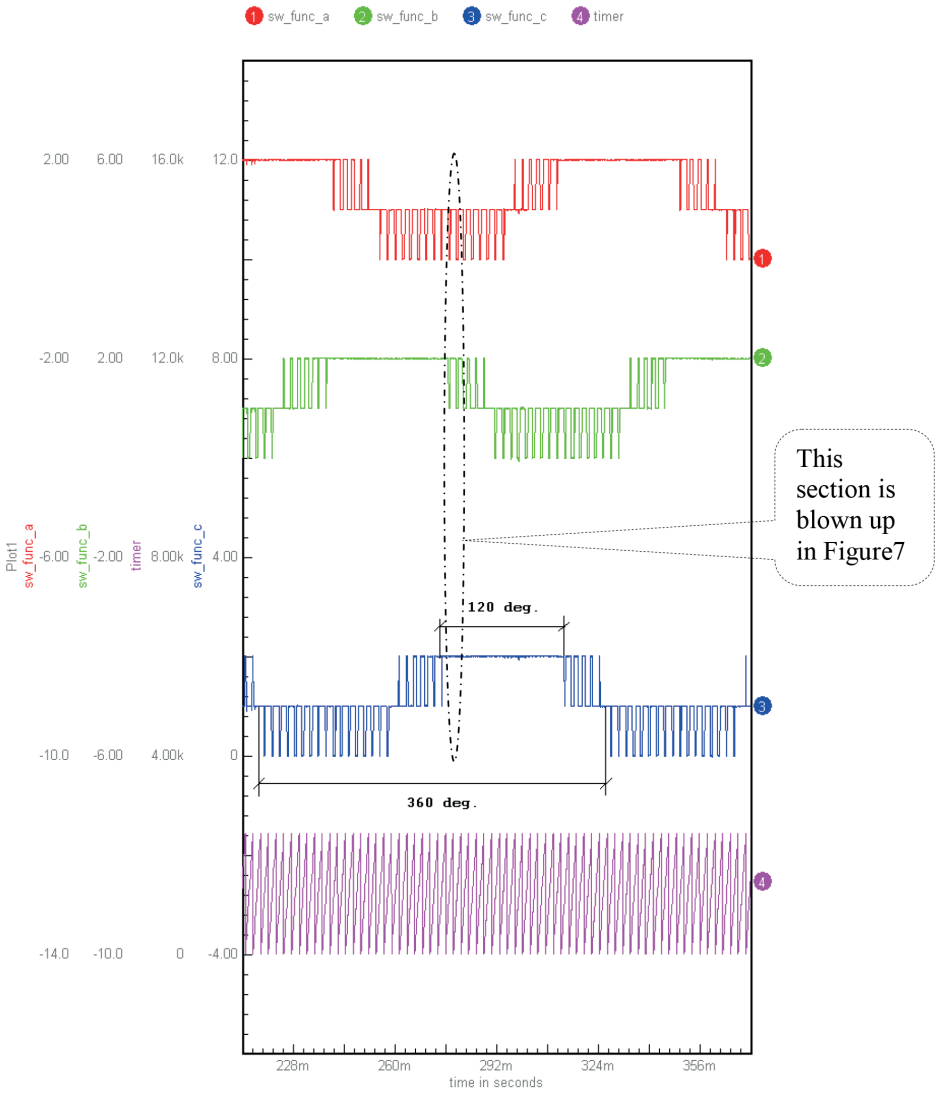


Figure 6. The switching function variation of the three phase legs along with timer count variation for the voltage waveform of Figure 5. No switching occurs in phase C for 120° while other phases perform switching.

one switch is changing its state at a time. Figures 6 and 7 show that the proposed algorithm is quite effective in reducing the overall switching loss of the inverter.

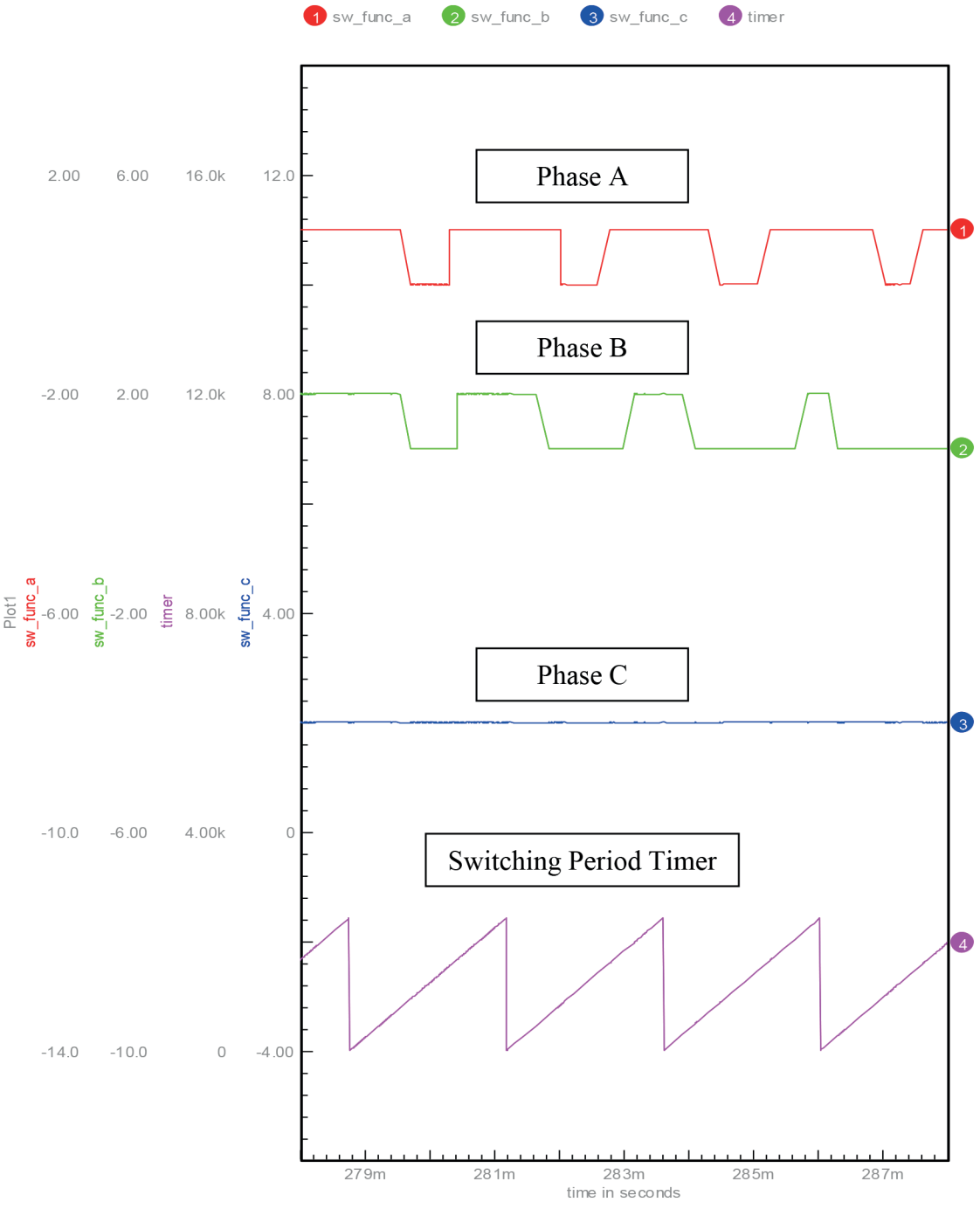


Figure 7. A close look at the switching waveforms given in Figure 6. Phase A and B switches turn on and off in proper order while phase C switch remains off.

7. Summary and conclusion

A fast minimum loss SVPWM algorithm for multilevel inverters is proposed. The algorithm has been generalized for implementing in multilevel inverters with an arbitrary number of levels. Since it has been expressed as closed-form equations by avoiding look-up tables, the algorithm is relatively compact. This would essentially yield high throughput in real-time implementation even if the number of levels increases. Sufficient details have been given in the paper to implement the algorithm in any computational platform. Simulation results illustrate the effectiveness of the algorithm to reduce the overall switching rate of the inverter.

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