

A new CMOS logarithmic current generator

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Abstract: A new CMOS current-mode controllable low-voltage and low-power logarithmic function circuit is proposed. The circuit provides good dynamic range, controllable output, and reasonable accuracy and it is insensitive to temperature variations. The circuit operates with ± 0.5 V supply, consumes $0.3 \mu\text{W}$, and has a -3 dB frequency of 2.4 MHz. The functionality of the proposed design is confirmed using Tanner T-spice with $0.35 \mu\text{m}$ CMOS process.

Key words: Logarithmic circuit, current-mode, subthreshold

1. Introduction

A logarithmic function is a nonlinear function in which the output is proportional to the logarithm of the input. The circuits performing such characteristics are widely used in many applications; these include but not limited to medical equipment, instrumentation, telecommunication, active filters, disk drives, and neural networks.

Many approaches to the design of logarithmic circuits have been reported in the literature [1–7] and the references cited therein. The authors did not find references to a CMOS current-mode logarithmic circuit in the open literature except for the one reported in [2]. However, this circuit produces the logarithmic of an input greater than unity and has a limited dynamic range. In addition, it has no gain controllability and it uses some passive elements.

All other realizations found in the literature have at least one of the following drawbacks: absence of low voltage operation capability [1,3,5], limited dynamic range [1,3,6], employment of BJT transistors [1,5,6], does not enjoy current-mode [1,3,4,6], cannot realize a true logarithmic function circuit where the ratio is larger or smaller than unity [1,6,7], temperature dependent [1,5], relatively high power consumption [6,7], no gain controllability [1,3,6], to some extent linearity error is high [3,6,7], uses passive elements, i.e. resistors [1,5,6], and finally design complexity [6,7].

The circuit given in [2] realizes a logarithmic function of the form:

$$I_{out} = \frac{I_{b4}}{\ln(N)} \ln\left(\frac{I_{in}}{I_{b2}}\right),$$

where N is the ratio between the biasing currents, I_{b2} and I_{b4} . I_{out} is the output current and I_{in} is the input current. However, since I_{out} must be positive then the condition $I_{in} \geq I_{b2}$ must be satisfied. Thus, the circuit is not capable of producing a true logarithmic function if I_{in} and I_{b2} attain arbitrary positive values and I_{out}

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could be of any positive or negative value. In [8] a current-mode CMOS logarithmic amplifier is proposed. The gain is controlled using a floating-gate trimming circuit.

In this paper, a CMOS low-voltage and low-power current-mode circuit capable of performing $\text{Log}(x)$ and $\text{Log}(1/x)$ is presented. The circuit provides high accuracy, temperature insensitivity, and controllable output. The remainder of the paper is organized as follows. Section 2 presents the design background and the proposed circuit. Simulation results and the discussion are presented in section 3. Section 4 concludes the paper.

2. Background and proposed design

2.1. Design principle

Based on Taylor's series expansion, an exponential function can be approximated by

$$e^x = 1 + x + \frac{x^2}{2!} + \frac{x^3}{3!} + \dots + \frac{x^n}{n!} + \dots \quad (1)$$

where x is the independent variable and if x is much smaller than one ($x \ll 1$) then the higher order terms in Taylors series approximation become negligible and Eq. (1) can be written as

$$e^x \approx 1 + x + \frac{x^2}{2!} \quad \text{for } x \ll 1 \quad (2)$$

According to (2), one can write e^{-x} as

$$e^{-x} \approx 1 - x + \frac{x^2}{2!} \quad (3)$$

From Eqs. (2) and (3) it can be shown that

$$e^x - e^{-x} \approx 2x \quad (4)$$

The error between " $e^x - e^{-x}$ " and " $2x$ " is plotted in Figure 1. The error can be less than 0.1% while the input $|x| < 0.2$.

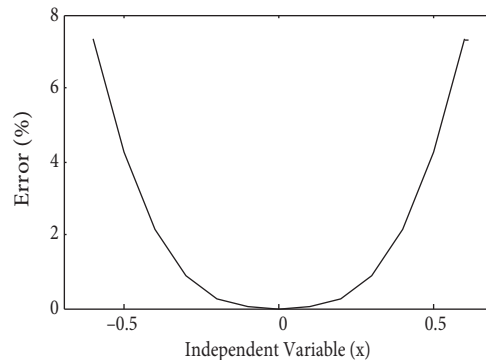


Figure 1. Error between " $e^x - e^{-x}$ " and " $2x$ ".

With reference to the exponential function generator core cell shown in Figure 2 [9], where I_b is the bias current and assuming that both M1 and M2 are matched transistors and both are biased in the subthreshold region, the current I_b and I_2 of the MOSFET in weak inversion can be expressed as [10]

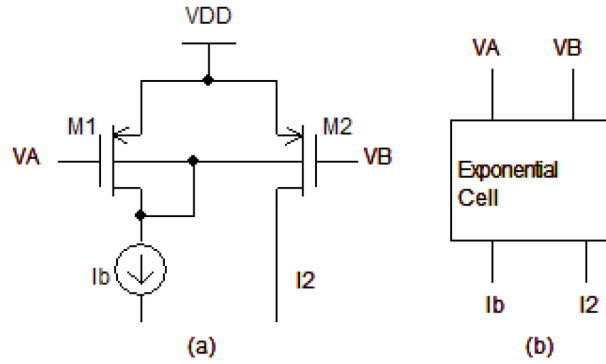


Figure 2. Basic exponential function circuit (a) circuit (b) symbol.

$$I_b = I_{D0} \cdot \exp \left[\frac{(V_{DD} - V_A) + (n - 1) V_{BS}}{n V_T} \right] \quad (5)$$

and

$$I_2 = I_{D0} \cdot \exp \left[\frac{(V_{DD} - V_B) + (n - 1) V_{BS}}{n V_T} \right], \quad (6)$$

where $I_{D0} = 2n\mu_n C_{ox} V_T^2 \frac{W}{L}$ is the leakage current, n is the weak inversion slope factor, μ_n is the mobility of charge carriers $\left(\frac{cm^2}{V.s}\right)$, C_{ox} is the normalized oxide capacitance, capacitor per unit gate area $\left(\frac{F}{m^2}\right)$, V_{BS} is the body-source voltage of M1 and M2 and $V_T = KT/q$ is the thermal voltage, K is Boltzmann constant ($1.38 \times 10^{-23} J/^\circ K$), T is temperature in degrees Kelvin, and q is charge of an electron ($1.6 \times 10^{-19} C$). Combining Eqs. (5) and (6) to get:

$$I_2 = I_b \cdot \exp \left[\frac{(V_A - V_B)}{n V_T} \right] \quad (7)$$

2.2. Proposed circuit

The proposed current mode logarithmic circuit is shown in Figure 3, where the current I_b is the bias current, I_x and I_y are the two input current signals, and I_{out} is the output current.

The drain currents of transistors M2 and M6 are given by Eqs. (8) and (9), respectively:

$$I_2 = I_b \cdot \exp \left[\frac{(V_A - V_B)}{n V_T} \right] \quad (8)$$

$$I_6 = I_b \cdot \exp \left[\frac{(V_B - V_A)}{n V_T} \right] \quad (9)$$

Eq. (9) can be rewritten as

$$I_6 = I_b \cdot \exp \left[\frac{-(V_A - V_B)}{n V_T} \right] \quad (10)$$

The drain current for transistor M8 is the same as the drain current of M6.

$$I_{out} = I_2 - I_8 = I_2 - I_6 \quad (11)$$

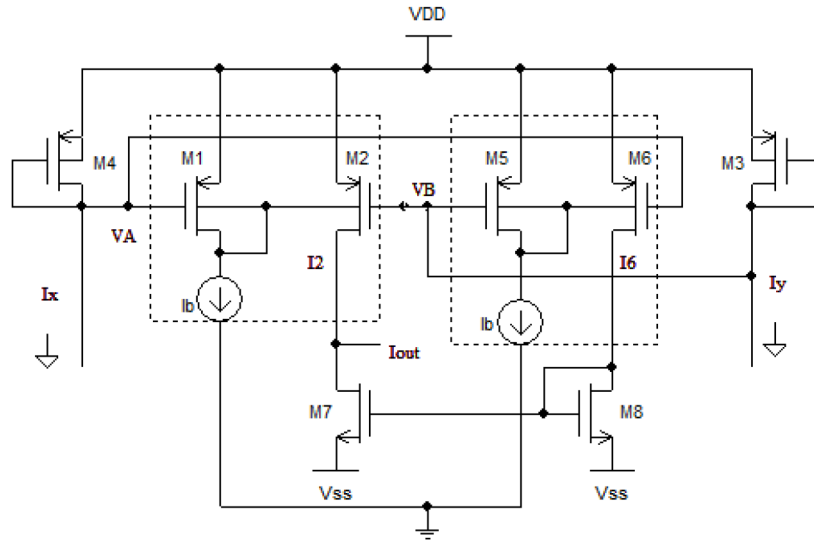


Figure 3. Proposed logarithmic circuit.

Combining Eqs. (8), (10), and (11), the output current is given by

$$I_{out} = I_b \left[\exp \left[\frac{(V_A - V_B)}{nV_T} \right] - \exp \left[\frac{-(V_A - V_B)}{nV_T} \right] \right] \quad (12)$$

Using Eq. (4) and with the quantity $\left[\frac{(V_A - V_B)}{nV_T} \right] \ll 1$, then Eq. (12) can be written as

$$I_{out} = 2I_b \cdot \left[\frac{(V_A - V_B)}{nV_T} \right] \quad (13)$$

Transistors M3 and M4 are used to convert the input currents I_Y and I_X to voltages V_B and V_A , respectively, in logarithmic form as shown in Eqs. (14) and (15):

$$V_A = V_{DD} - V_{sg4} = V_{DD} - nV_T \ln \left(\frac{I_X}{I_{Do}} \right) \quad (14)$$

$$V_B = V_{DD} - V_{sg3} = V_{DD} - nV_T \ln \left(\frac{I_Y}{I_{Do}} \right) \quad (15)$$

Combining Eqs. (15) and (14) to get:

$$\left[\frac{(V_A - V_B)}{nV_T} \right] = \ln \left(\frac{I_Y}{I_X} \right) \quad (16)$$

Combining Eqs. (13) and (16) the output current I_{out} is given by

$$I_{out} = 2I_b \cdot \ln \left(\frac{I_Y}{I_X} \right) \quad (17)$$

Eq. (17) is a current-mode logarithmic function. When the current I_x is kept constant, the output current I_{out} is proportional to the logarithm of I_y , and its gain can be controlled by the bias current I_b . $\text{Log} \left(\frac{1}{x} \right)$ is implemented when current I_y is kept constant.

To assure the MOS operates in the weak inversion forward saturation, the conditions $I_D \leq I_{D0}$ and $V_{DS} \geq 4V_T$ must be satisfied.

3. Simulation results and discussion

The layout and postlayout simulations for the proposed circuit were carried out using Tanner tool in $0.35 \mu\text{m}$ 2p4m TSMC process. The layout of the circuit is shown in Figure 4. The simulation results were obtained for $I_b = 30 \text{ nA}$, $I_x = 125 \text{ nA}$, and $V_{DD} = -V_{SS} = 0.5 \text{ V}$. The transistors' aspect ratios are listed in Table 1.

Table 1. Aspect ratios of transistors.

Transistor	Aspect ratios (W/L)
M1-M2	$1.4 \mu\text{m}/0.35 \mu\text{m}$
M3-M4	$6.3 \mu\text{m}/0.35 \mu\text{m}$
M5-M6	$1.4 \mu\text{m}/0.35 \mu\text{m}$
M7-M8	$1 \mu\text{m}/1 \mu\text{m}$

The output current was measured by forcing it through a grounded load $R_L = 1 \text{ k}\Omega$. The current I_x was set to 125 nA and the input current I_y was varied from 20 nA to 400 nA . The measured output dynamic range is around 150 nA . The simulated and calculated results are shown in Figure 5 using log scale. Figure 5 clearly shows that simulated results are in very good agreement with the theory and confirm the functionality of the developed design. As also shown in Figure 5, the output current is zero for $I_y = I_x = 125 \text{ nA}$. It was found that the maximum linearity error is 4% and the maximum power consumption is $0.3 \mu\text{W}$.

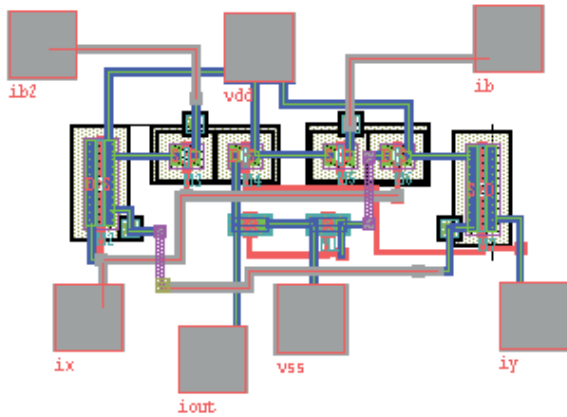


Figure 4. The layout for the proposed circuit.

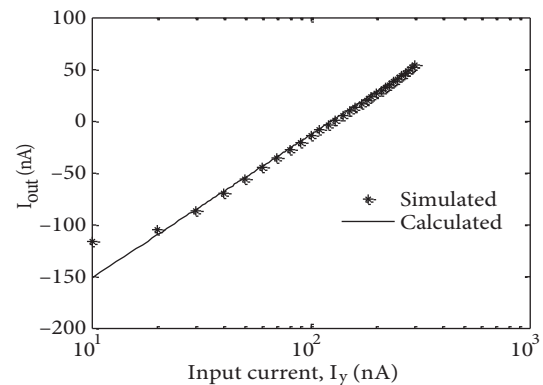


Figure 5. Simulated and calculated results of Eq. (17).

The circuit was simulated for different values of the bias current I_b and the corresponding output current is shown in Figure 6. It is evident from Figure 6 that the circuit gain is controllable.

The temperature insensitivity of the proposed design was confirmed by simulation. The temperature was varied from -25 to $+75 \text{ }^\circ\text{C}$, the output current was normalized to its value at $T = +25 \text{ }^\circ\text{C}$. Simulation results are shown in Figure 7. It is clear from Figure 7 that the output current I_{out} is insensitive to temperature.

The circuit transient response was also found for a triangular signal shifted by 40 nA DC component. The simulation results shown in Figure 8 confirm the functionality of the circuit.

The circuit was also simulated for frequency response. The -3 dB bandwidth is found to be 2.4 MHz as shown in Figure 9.

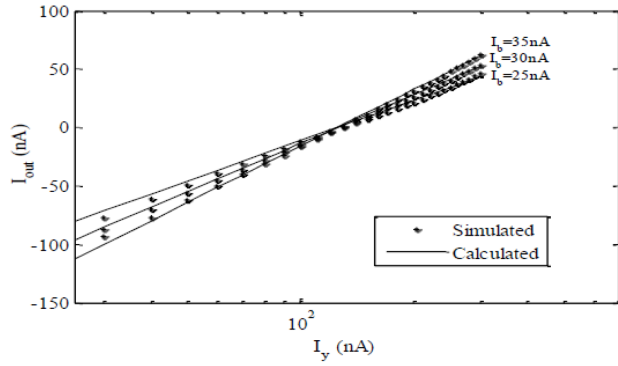


Figure 6. Varying the gain using the bias current Ib.

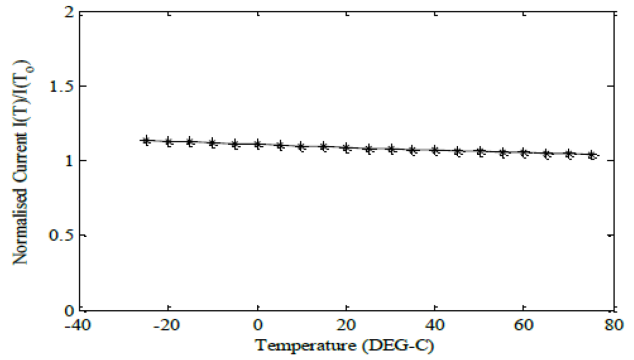


Figure 7. Temperature analysis of the proposed design.

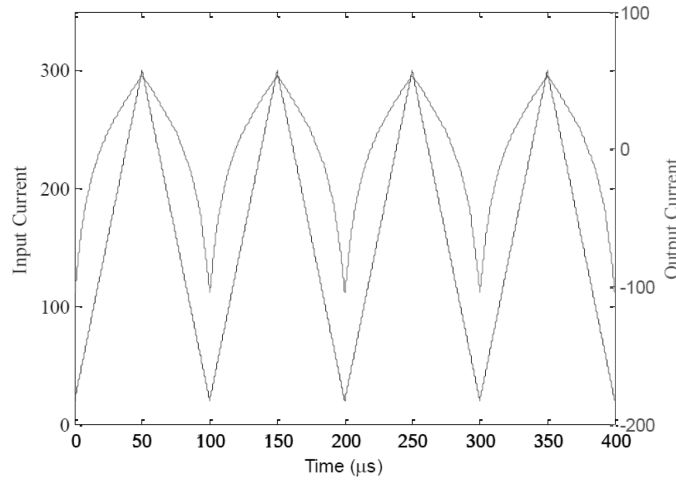


Figure 8. Transient response of the proposed design.

The circuit can be used to implement for $\text{Log} \left(\frac{1}{x} \right)$ at constant current I_y . The simulation result for this function is shown in Figure 10.

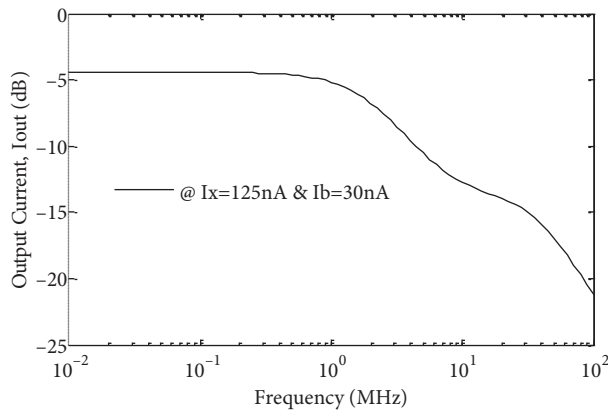


Figure 9. Frequency response of the proposed design.

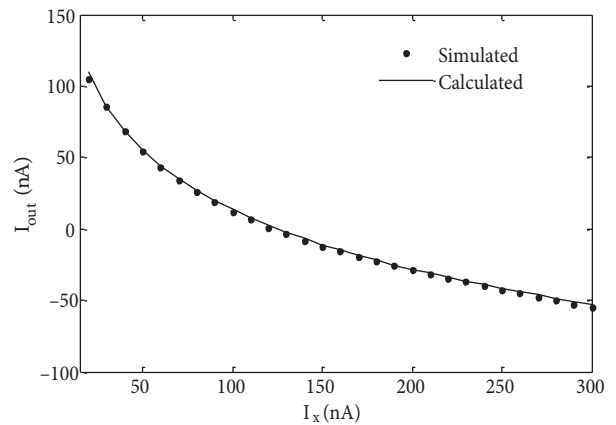


Figure 10. Simulation result for $\text{Log} \left(\frac{1}{x} \right)$ of the proposed design.

Simulation for noise analysis was carried out. The equivalent noise at the input terminal and the output one are plotted in Figure 11. The simulation was carried out with the input DC and small signals equal to 100 nA and 50 nA, respectively, and a $1 - k\Omega$ resistor was attached to the output as a load. It is clear that noise suppression is achieved by around 50%.

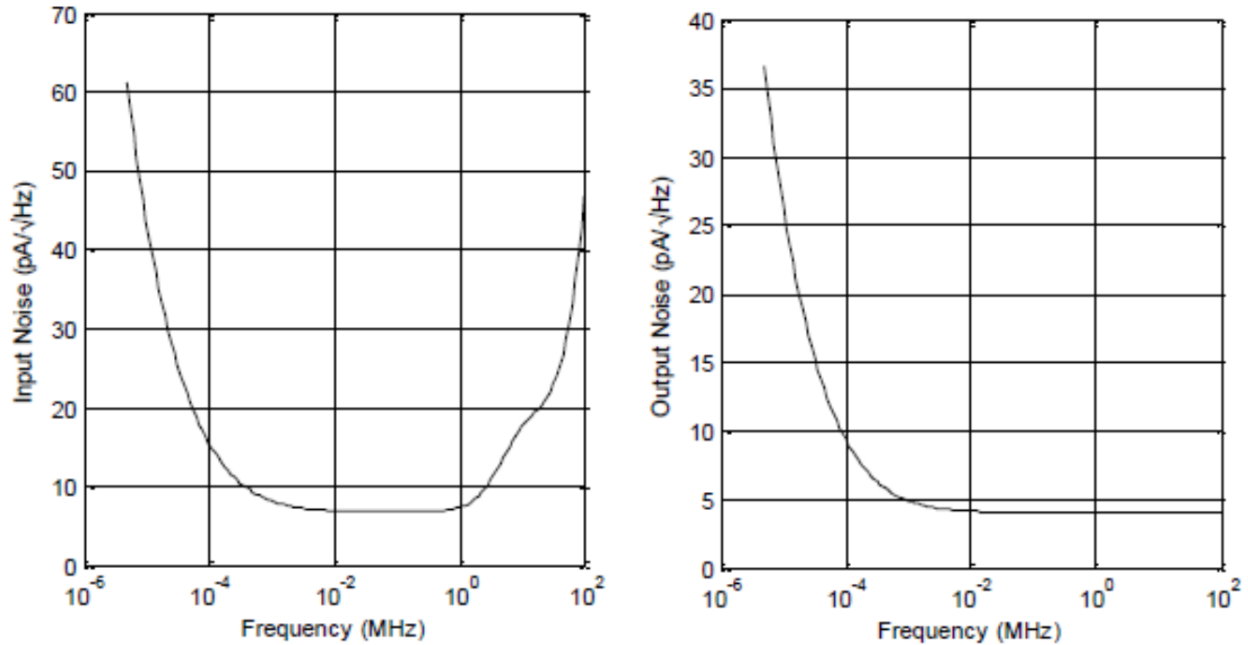


Figure 11. Equivalent input and output noise plot (I / \sqrt{Hz}): (a) input noise (b) output noise.

The performance of the proposed design was compared with previously published work [1–3]. Table 2 summarizes the comparison of the important parameters. It is clear from the table that the proposed design is superior to the reported studies in very important factors. The proposed design is small in size compared to all other designs, gain controllable using bias current, temperature insensitive without using an extra circuit for temperature compensation, and true for $x > 1$ or $x < 1$.

Table 2. Performance comparison.

Parameter	[1]	[2]	[3]	[8]	Proposed Work
Technology (Process)	0.18 μm BiCMOS	0.5 μm CMOS	0.18 μm CMOS	0.5 μm CMOS	0.35 μm CMOS
Operation region	Saturation	Sub-threshold	Sub-threshold	Sub-threshold	Sub-threshold
Voltage supply	> 1.3 V	-	1.8 V	-----	± 0.5 V
Input/output	Voltage-voltage	Current-current	Current-voltage	Current-current	Current-current
Power dissipation	17.75 mW	--	30 nW	100 nW	0.3 μW
Gain controllability	No	Yes	No	Yes	Yes
True for $x \geq 1$ or $x < 1$	Not satisfied	Not satisfied	Satisfied	Not Satisfied	Satisfied
Max. linearity error	63%	NA	5%	0.4%	4%
Temperature	Sensitive	Compensated using PTAT	Sensitive	Sensitive	Insensitive
Area	NA	NA	NA	9 mm^2	288 μm^2

4. Conclusion

In this paper, a novel CMOS current-mode logarithmic circuit is proposed. The circuit produces a highly accurate logarithmic function for any value of I_y larger or smaller than I_x . The performance of the proposed

logarithmic circuit has been verified using Tanner Tools with 0.35 μm CMOS process. The circuit consumes around 0.3 μW and has maximum linearity error of 4% and -3 dB of 2.4 MHz. The proposed circuit is expected to be a useful building block in many analogue signal processing applications.

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