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A 0.18-μm current-mode asynchronous sigma-delta modulator design

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Abstract: In this study a first-order asynchronous current-mode sigma-delta modulator has been designed and simulated. Asynchronous sigma-delta modulators eliminate the continuous time sigma-delta modulator's problem of signal-to-noise ratio degradation due to clock jitter by avoiding the use of sampling in the modulator loop. Moreover, they provide a higher signal-to-noise ratio even with low-order filters. Thus, considerably low power consumption can be achieved with fewer circuit components. The current mode enables designers to scale the circuits according to different supply voltages and operating currents. In this work, design steps for an asynchronous sigma-delta modulator have been given taking into account its ideal mathematical model. Novel current comparator architecture is proposed, which is used as a one bit-quantizer. Its working principles are explained. The comparator's operation is verified by the simulations in the asynchronous sigma-delta loop. Simulation results show that a satisfactory performance can be obtained with relatively simple designs, compared to ordinary synchronous continuous time sigma-delta modulators.

Key words: Analogue to digital converters, asynchronous sigma-delta modulator, sigma-delta modulator, current mode sigma-delta modulator

1. Introduction

Despite the fact that most electronic circuitry used is digital, there are still numerous applications, such as wireless communications, sensors, and data storage, that will stay analogue. Analogue to digital converters (ADCs) bridge the analogue world and the digital computational domain; thus their performance is crucial. The most important performance parameters of ADCs are the number of output bits and achieved signal bandwidth. Sigma-delta modulators provide medium bandwidth and high number of bits; therefore, they are demanded mostly by audio applications [1]. The sampled and coded signal by the modulator has to be fed into a digital filter to eliminate high frequency undesired signals caused by oversampling. The block diagram of the two sigma-delta converter types: continuous and discrete time [2–5], including the necessary succeeding decimation filter, are given in Figures 1a and 1b. Continuous time sigma-delta modulators consume less power compared to discrete time modulators [5].

Despite their benefits, the continuous time sigma-delta modulator's performance is limited by the jitter of the sampling clock [6].

The degradation of the signal-to-noise ratio (SNR) due to clock jitter is given in Eq. (**??**).

$$SNR_{jitter\_CT} = \frac{P_s}{P_{jitter}} = \frac{OSR \cdot A^2}{2\sigma_{\Delta y}^2 \frac{2\sigma_{\Delta t\_CT}^2}{T_s^2}} \tag{1}$$

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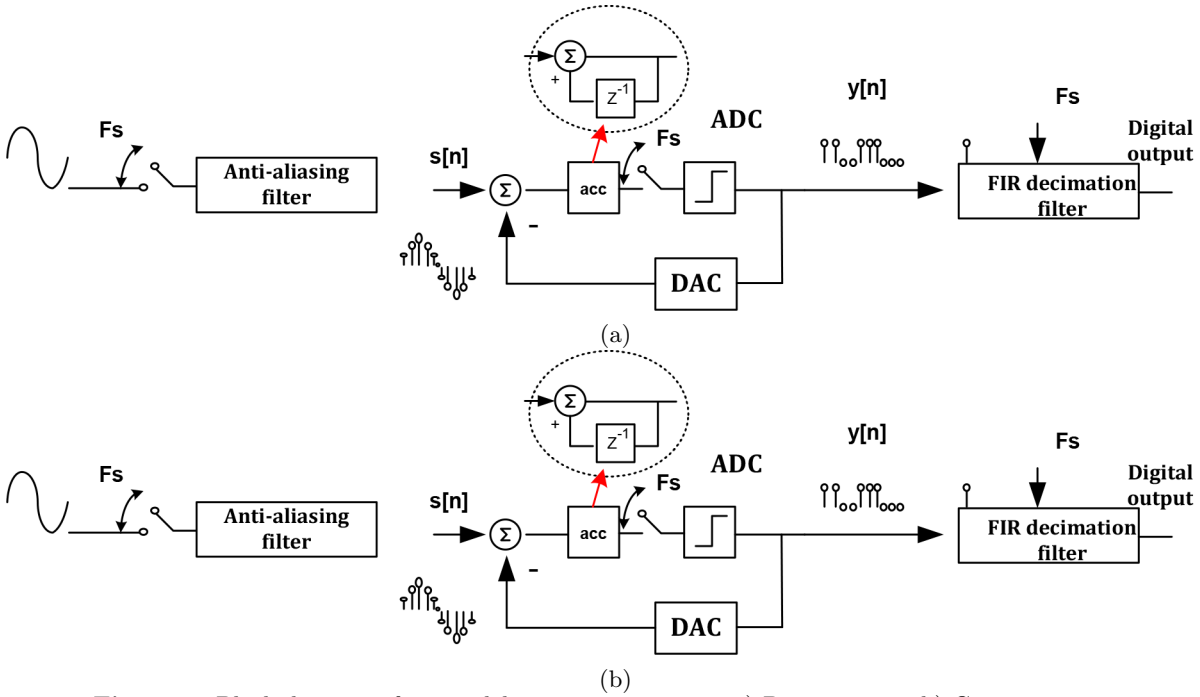

Figure 1. Block diagram of sigma-delta conversion types: a) Discrete time; b) Continuous time.

In Eq. (**??**), *OSR* denotes the oversampling ratio, *Ts* is the sampling period, and *A* is an order related parameter. The parameters $\sigma^2_{\Delta t\_CT}$ and $\sigma^2_{\Delta y}$ are the variance of the jitter in the clock signal and the jitter in the output y[n] – y[n – 1], respectively. The degradation can be further observed in Figure 2, which gives SNR values versus the amount of jitter.

All circuits including ADCs can be classified according to the signal domain they operate in as given in Figure 3. All nonsampled analogue circuits belong to 'Domain 1'. All sampled data processing analogue circuits, such as the discrete time sigma-delta ADCs, belong to 'Domain 2'. Digital circuits are classified as 'Domain 4'.

The asynchronous sigma-delta operates in 'Domain 3' and avoids the clock jitter problem by not using sampling in time. The signal will be sampled at the filtering phase, which will take place after the modulation.

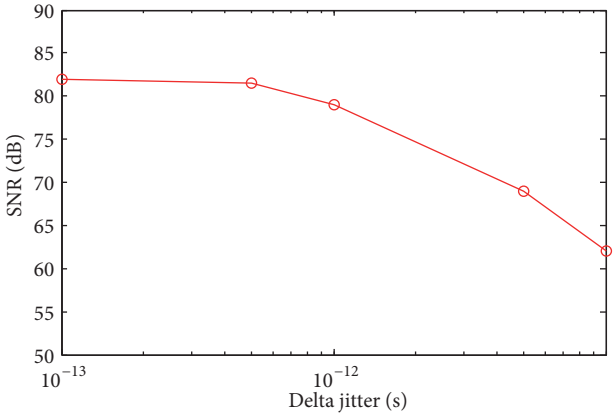

Figure 2. Influence of clock jitter on a third order continuous time (CT) sigma-delta ADC.

Amplitude	Time	
	Continuous	Sample
Continuous	Domain 1 Analogue domain	Domain 2 Discrete time domain
Sampled	Domain 3 Asynchronous	Domain 4 Digital domain

Figure 3. Signal processing circuits classified according to the domain of the signal.

A typical first-order sigma-delta modulator's block diagram, consisting of a loop filter and a quantizer, is given in Figure 4. In order to obtain digital output data, as in the synchronous counterparts, the modulator's output has to be fed to a special pulse width demodulation decoder filter.

In the next section the mathematical background of the asynchronous sigma-delta modulation is reviewed with the addition of useful observations, since it should be taken into account in the circuit design phase. The third section discusses the circuit design, followed by results and conclusion sections.

2. Mathematical background for the first-order modulator

The first-order asynchronous sigma-delta modulator (ASDM) produces a square wave output of which the duty cycle changes according to the input signal's amplitude. However, this type of modulation is a little different from original pulse width modulation (PWM), since the frequency of the signal changes also with the amplitude of the input. Considering the first-order sigma-delta circuit, if the hysteresis' thresholds of the quantizer are at $\pm\varepsilon$, the integrator's output will be a ramp function as depicted in Figure 5. Typical output of an asynchronous modulator is given in Figure 6. The ramp changes direction after reaching one of the thresholds. The total period, $T = T_1 + T_2$, is the sum of the up and down ramp times. Time spent in these regions is related by the integrator input v as follows:

$$T_1 = 2\frac{\varepsilon}{K(1+v)}$$

$$T_2 = 2\frac{\varepsilon}{K(1-v)}$$

$$T = T_1 + T_2 = \frac{4\varepsilon}{K(1-v^2)}$$

$$\alpha = (\text{the high period}) = \frac{T_1}{T} = \frac{(1+v)}{2} \tag{2}$$

In Eq. (**??**), K represents the integration constant.

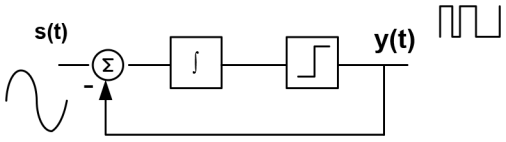

Figure 4. Block diagram of asynchronous sigma-delta modulator.

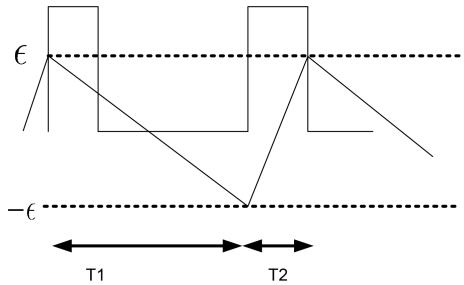

Figure 5. The output of the integrator and quantizer of the first-order modulator.

There are several methods, such as the describing function method [7,8] to obtain the frequency of oscillation for the modulator system containing the ideal relay nonlinearity with hysteresis (i.e. nonlinearity with abrupt transition between the saturation levels at hysteresis thresholds). However, in real circuit applications, the ideal relay function is not realizable since comparators' gains are always finite. The nonideal nonlinearity function is given in Figure 7.

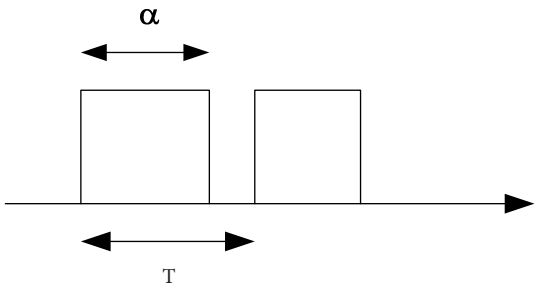

Figure 6. Duty cycle modulated wave.

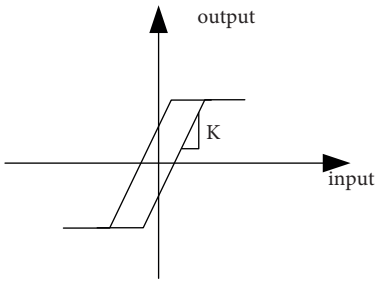

Figure 7. Transfer characteristics of a comparator with hysteresis.

The asynchronous sigma-delta modulator needs a minimum amount of loop gain for proper operation. It can be seen from the above paragraph that any system with a first-order integrator and a comparator with hysteresis will oscillate with a nonzero input. However, if the hysteresis transfer characteristics are as given in Figure 7 (finite transition slope), a minimum gain for sustaining oscillations is needed. This value can be found using the stability criteria for nonlinear systems. In this work, the following equation is used to obtain the minimum loop gain for sustaining limit cycle oscillations:

$$G(j\omega)N(A) = -1 \tag{3}$$

In Eq. (**??**), $G(j\omega)$ represents the integrator's transfer function and $N(A)$is the description function of the quantizer (comparator) nonlinearity. The describing function, which is a complex valued function, can be decomposed to in-phase and quadrature components. Since $G(j\omega)$ in Eq. (**??**) is an ideal integrator function, it is pure complex. It is seen that the oscillation condition is dependent on a minimum loop gain K. Therefore, in circuit design ensuring a high overall loop gain should be necessary for proper operation.

It is also necessary to analyze the output of a typical asynchronous modulator for designing a circuit with a desired performance. A typical duty cycle modulated waveform can be written as given in [9,10]:

$$s(t) = A_0 + \sum_{n=0}^{\infty} A_n \cos(\omega_c n + \varphi_n) \tag{4}$$

The output spectrum consists of harmonics in Bessel functions form, but the zero order and first harmonic components are especially important; they carry the input signal and noise that affects the inband noise.

$$S_0(t) = \frac{s(t)Vdc}{2}$$

$$S_1(t) = \frac{Vdc}{\pi} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} J_{2n}(\beta) J_m(\beta_M) \cdot \cos(\omega_c t + (2n+m)\omega_M t)$$

$$\beta = \frac{\omega_\Delta}{2\omega_m} = \frac{1/2M^2\omega_c}{2\omega_m}$$

$$\beta_M = M\frac{\pi}{2} \tag{5}$$

The values β and β_M denote modulation indices, which are related to limit cycle frequency ω_c, input signal frequency ω_m, and input amplitude of the sinusoidal signal M in Eq. (**??**). From Eq. (**??**), it can be

observed that the output of the asynchronous circuit is a frequency modulated PWM. The output consists of the multiplication of two Bessel functions.

The fall rate of this noise is higher than that of the low-order synchronous sigma-delta converters. Therefore, even with a first-order asynchronous modulator circuit a reasonable value of SNR can be achieved. Thus, designing a first-order modulator can result in a performance of a third- to fourth-order classical synchronous continuous time sigma-delta modulator.

3. Circuit design

Current mode circuits have been considered an alternative to voltage mode circuits when power, bandwidth, or dynamic range is important. Newer production technologies reduce voltage headrooms further and further. This forces circuits to operate in a limited dynamic range. Current mode circuits offer reduced voltage swing; therefore, they allow a much larger region to operate in [11,12]. One of the most important advantages of current mode circuits is designing the signal path is considerably easier compared to the voltage mode. When circuit blocks are designed properly, they can be put next to each other most of the time.

A prior circuit design and implementation of an asynchronous sigma-delta modulator have been done, using voltage mode circuits [13].

The proposed asynchronous sigma-delta modulator in this work consists of a current-mode integrator and a current comparator to minimize distortion caused by large voltage swings. All of the designs are done using 0.18 μm TSMC CMOS technology.

The circuit diagram of a typical first-order asynchronous sigma-delta modulator is given in Figure 8. The voltage to current converter block is shown with g_m, followed by the integrator, which consists of an amplifier A and integration capacitances; at the end is the comparator.

In this design, linearity requirements for different blocks in the modulator are analyzed by modeling circuit blocks as a combination of linear elements and an additional distortion source as given in Figure 9.

In Figure 9, the leftmost block, outside the sigma-delta loop, is the voltage to current converter. The integrator is modeled with a gain element of A_1, the comparator is modeled with a gain element of A_2, and the feedback signal circuit is modeled with a gain element of B. The output voltage's relation to the input, gains, and distortions is given in Eq. (**??**). Although the circuit will operate in current mode, since current and voltages can be converted to each other, Eq. (**??**) is written in voltage form.

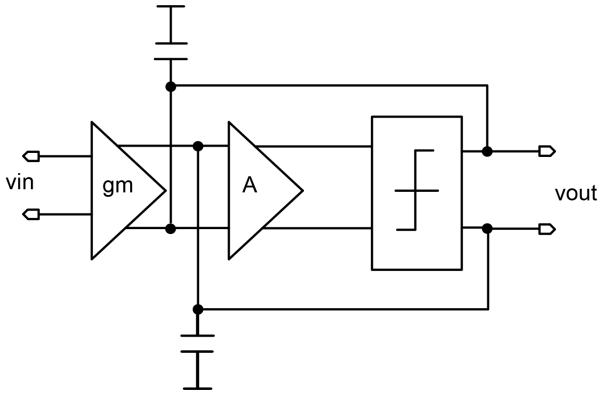

Figure 8. Circuit block diagram of first-order asynchronous sigma-delta modulator.

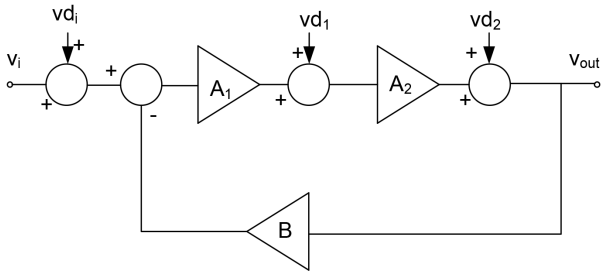

Figure 9. First order modulator blocks modeled as gain elements and distortion sources.

It can be observed from Eq. (**??**) that input distortion is not suppressed, whereas the integrator's and comparator's distortions are suppressed by the amount of their corresponding gain terms.

$$v_{out} = \frac{A_1 A_2}{1 + A_1 A_2 B}(v_i + vd_i) + \frac{A_1}{1 + A_1 A_2 B}(vd_1) + \frac{1}{1 + A_1 A_2 B}(vd_2) \tag{6}$$

The voltage to current converter is the first stage of the modulator and its linearity is crucial, since its distortion is not suppressed by the feedback. In order to get a high spurious free dynamic range (SFDR) and also high signal-to-noise and distortion ratio (SINAD), the harmonics of the converter should be greatly eliminated in the design phase. Many voltage to current converters have been presented to date [14–20].

The converters [14–17] using classical approaches achieve a maximum of 60 dB SFDR. Approaches [18–20] provide higher SFDR. The proposed converter in [19] uses both the source resistors and output current differencing methods and can eliminate the third and fifth harmonics nearly completely. In this work this converter is selected considering the simplicity of its circuitry and parameter flexibility to adjust the overall distortion of the modulator. As a second consideration, input and output impedance requirements for the voltage to current converter are taken into account. The circuit of the voltage to current converter used in the design is given in Figure 10.

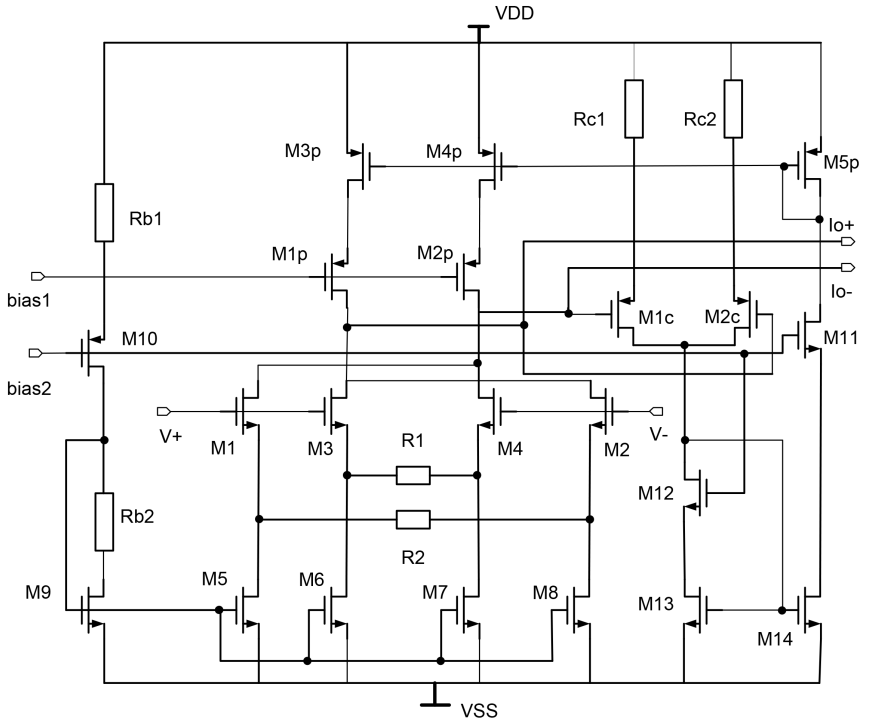

Figure 10. Voltage to current converter used in the design.

Current-mode integrators are more advantageous compared to their voltage-mode counterparts in aspects of their supply voltage reduction, power, bandwidth, and third harmonic intermodulation (IM3) distortion. The integrator proposed in [21,22] provides very good specifications like low IM3 distortion; therefore, it is an excellent candidate to use. In real circuit designs, an ideal integrator is very hard to realize because of the nonidealities. Since the circuit has finite input resistance, the realized function will be in fact a low-pass filter.

However, bringing the low-pass filter's pole near low frequencies provides an ideal-like integrator. In order to maintain a high loop gain, the integrator's gain should be maximized. Therefore, the low voltage cascode version of this integrator is used, which is given in Figure 11. The frequency response of the integrator used is given in Figure 12. The input–output transfer function and zero frequency differential gains (A_0) for the output current i_{out} and input current i_{in} are

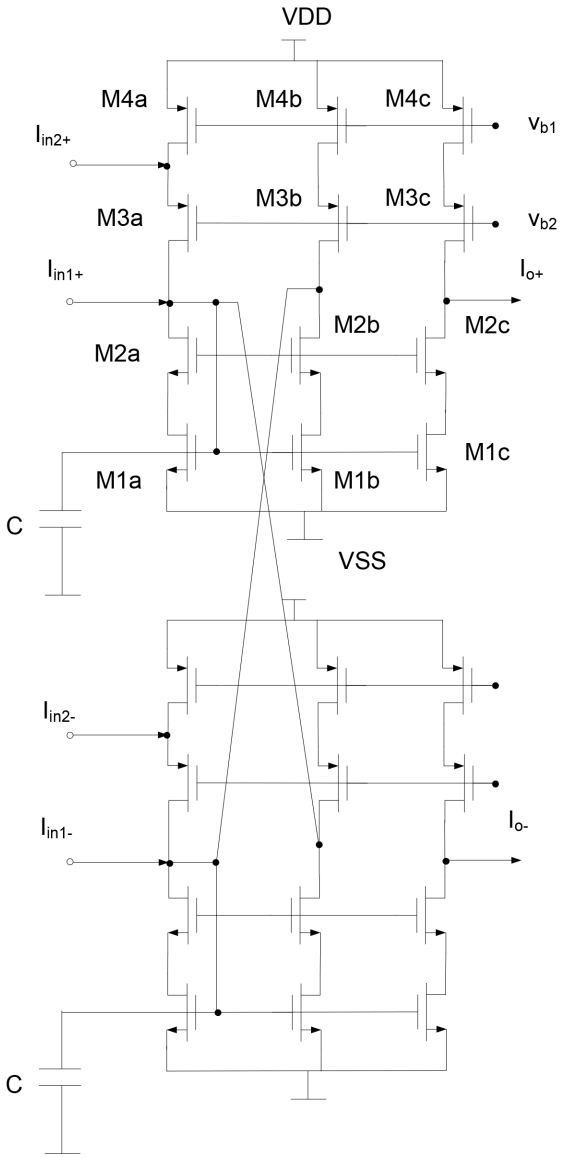

Figure 11. Current integrator used in this work.

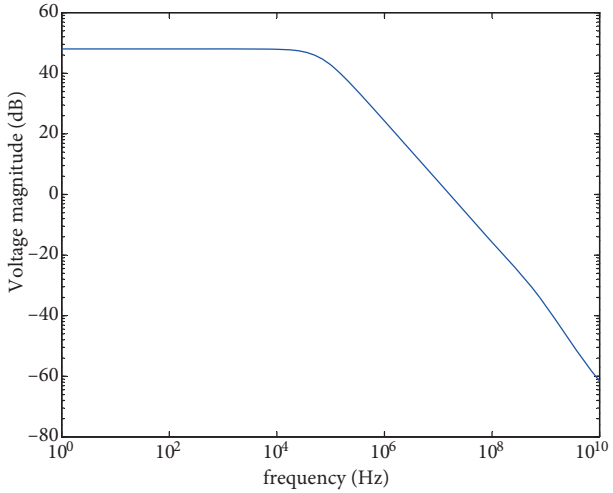

Figure 12. Frequency characteristics of current mode integrator used in the circuit.

$$\frac{i_{out}}{i_{in}} = \frac{A_0}{1 + s(2g_{ds}/(C + 4C_{gd})}$$

$$A_0 = \frac{g_m - g_{ds}}{2g_{ds}} \tag{7}$$

In Eq. (**??**), g_m and g_{ds} denote equivalent input and output conductances for the output node in the circuit, C_{gd} the input gate to drain capacitance of the input transistor, and C the integration capacitance. From the circuit diagram given in Figure 8, it can be seen that there are two input signals for the integrator. The first one is coming from the feedback path and the other from the input voltage to current converter. More linear operation is achieved when the voltage to current converter output is fed into input nodes I_{in2} and the feedback current enters via nodes I_{in1} as shown in Figure 11.

In this work, a novel current comparator topology is designed. Its circuit diagram is given in Figures 13a and 13b. Transistors M_1 and M_2 and the two resistors labeled with R constitute transimpedance amplifiers. Latching transistors M_3 and M_4 provide high gain and also provide differential operation. The transfer characteristic is a function of dimensions of M_1, M_2 and M_3, M_4 and resistance R.

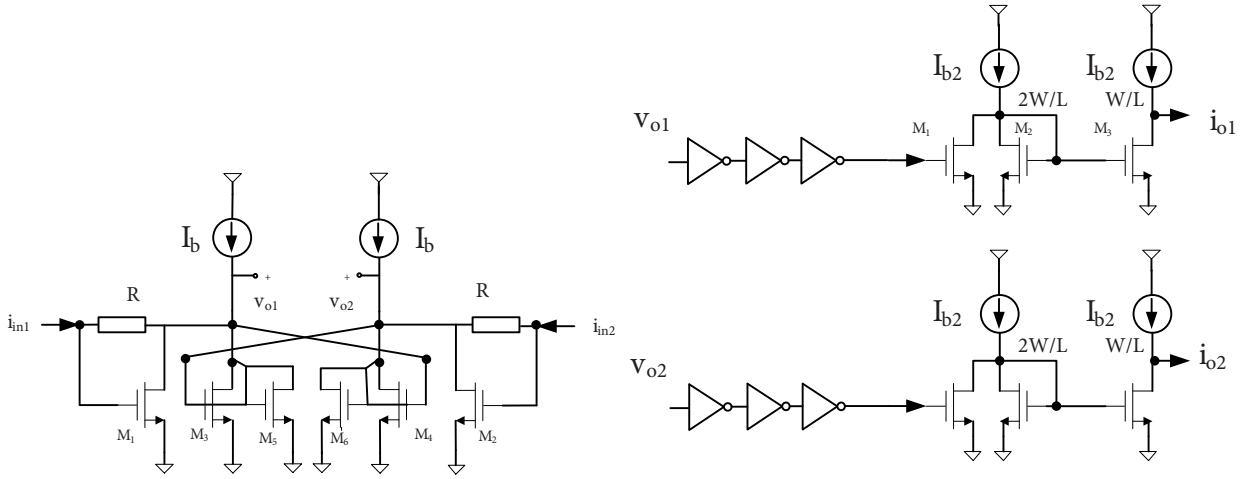

Figure 13. Current comparator designed for the circuit: a) Current comparator; b) Cascaded inverters with the voltage to current converter at the end.

The small-signal model of the circuit is given in Figure 14. It can be seen that the circuit shows a fully differential property. Transistors M_5 and M_6 can be put optionally to limit the output voltage swing and shape and smooth the response.

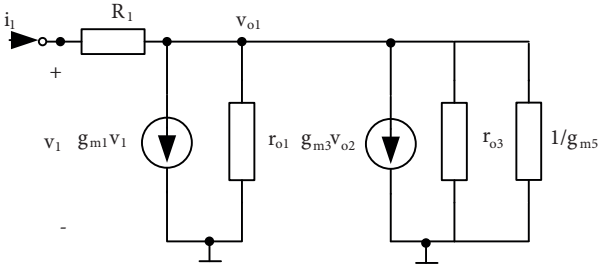

Figure 14. Small-signal model of half of the circuit in Figure 13.

The differential gain of the transresistance circuit can be written as

$$A_d = \frac{1 - gm_1 R_1}{gm_1 - gm_3 + \frac{1}{ro_1} + \frac{1}{ro_3} + \{gm_5\}} \tag{8}$$

The transconductances of M_1, M_3, and M_5 are denoted as gm_1, gm_3, and gm_5, respectively. The output resistances of M_1 and M_3 are denoted as r_{o1} and r_{o3}. High gain can be obtained when g_m values in the

numerator are canceled. If gm_3 is sufficiently large, the amplifier shows latch transfer characteristics. The gm_5 term shown in brackets is effective only when M_5 and M_6 are used and the output voltage reaches a certain level.

Synchronous sigma-delta modulators do not have extra requirements for oscillation. Every clock tick, the comparator generates a comparison result. However, asynchronous sigma-delta modulators put several constraints on circuit blocks' gains in order to maintain self oscillations. A minimum overall loop gain has to be achieved for proper operation. The comparator's transfer gain should be as high as possible and if gain is not very high, an increase in harmonic distortion and therefore degradation in the SNR value is observed. Instead of cascading several comparators, which causes chip area to be lost and also consumes high static power for obtaining high gain, gain is increased by adding cascaded inverters, which do not consume much chip area or static power.

The overall gain of the comparator section is when gains of cascaded inverters are A_1, A_2, and A_3, respectively, and A_d is the gain of the transimpedance amplifier:

$$A = A_d\, A_1\, A_2\, A_3 \tag{9}$$

The output of the comparator is a voltage signal. Because the modulator's feedback is a current signal, an additional simple voltage to current converter is used, which is shown in Figure 13b. The overall current input current output transfer curve of the comparator is given in Figure 15.

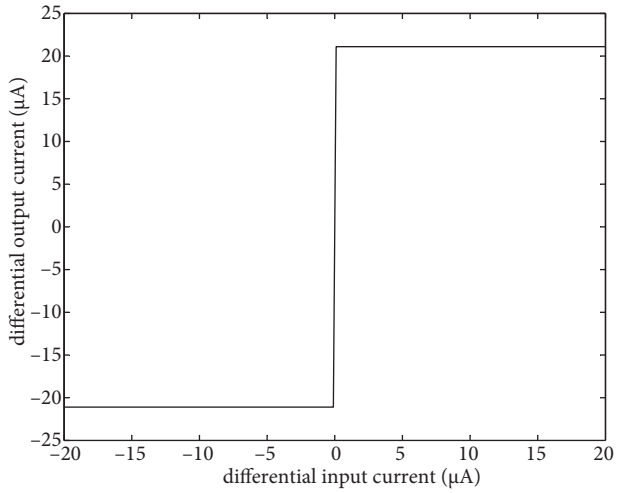

Figure 15. Input–output characteristics of the overall comparator circuit.

Since the comparator's transistors also introduce some nonlinearity and also a high value of loop gain is desired, power consumption in this stage is not minimal, which results in a total current consumption of about 350 μA. The voltage to current converter uses 32 μA current of this value.

The linearity of the sigma-delta modulator is the biggest concern, since achievable SFDR is dependent on the unwanted harmonics generated by the individual circuit components. The loop is designed carefully, so that every signal is not clipped, since any clipping is reflected as a distortion component in the spectrum. The goal set is a good SNR value in a band of 10 MHz.

To optimize the amount of the distortion, there are two main paths to follow. The first one is to minimize each block's own distortion; the second one is to design the loop with sufficient gain to suppress the apparent distortion below a certain amount, but this sometimes results in an increase in distortion since each block's

generated distortion increases as its gain increases. The upper limit of the bandwidth is determined by the amount of noise and distortion. For the desired amount of bandwidth, the limit cycle of the circuit is designed to be 100 MHz. This center frequency ensures the magnitude of the Bessel components is sufficiently low in the band of interest. The main degradation of the SNR in the band is caused by odd harmonics (i.e. first, third, fifth, and others) of the input signal caused by the nonlinearity of the circuits used. If the upper margin of the input bandwidth goal is 10 MHz, the worst case distortion occurs up to 2 MHz frequency input signals, since all the above-mentioned distortion components fall in the band of interest.

4. Simulation results

The circuit is designed with 0.18 μm TSMC technology and simulated using HSPICE. The modulator's output voltage is given in Figure 16. The pulse width of the output pulses, which corresponds to the input signals amplitude, is also drawn in the same figure to give an idea of the circuit's operation.

The output power spectral density is given in Figure 17. The achieved SNR is about 68 dB in a 10 MHz band of interest. The Bessel components, which are considered as noise, can be observed around 100 MHz center frequency. These components decrease by the amount given in Eq. (**??**). Since the signal in the band has some distortion components compared to the ideal mathematical model, the Bessel noise deviates from the equation, when they are away from center frequency. Cross distortion components arising are added to Bessel harmonics. The resulting noise decreases with the frequency when moving away from the central frequency and it finally enters the band of interest.

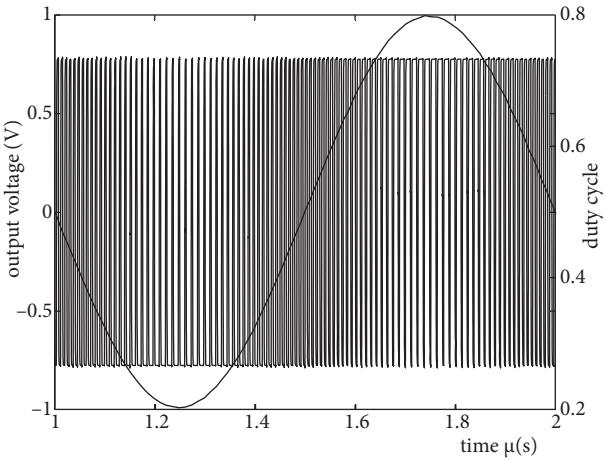

Figure 16. Output voltage of the simulated asynchronous modulator working at 100 MHz with duty cycle variation plotted.

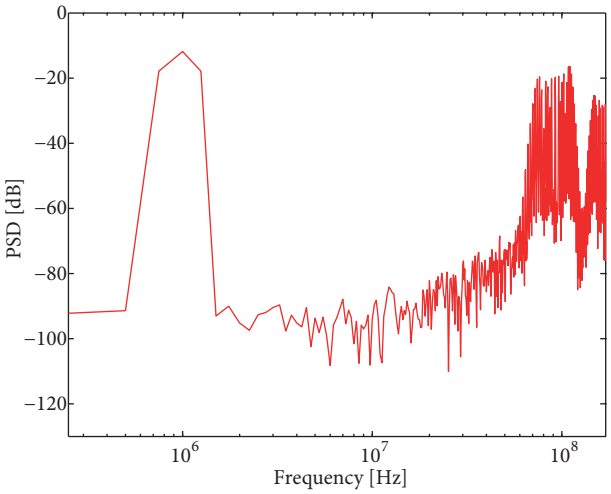

Figure 17. Power spectral density of the modulator output simulated for a 1 MHz input signal.

Since noise components in the band of interest are smaller than the input signal distortion components (third, fifth, seventh harmonics), input distortion, which is caused by the circuit's nonlinearity, is the main component of the SNR degradation. The fall rate of the noise outside the band is also dependent on the harmonic suppression of the loop and hence gain of the individual circuit blocks.

The resulting overall performance of the simulated circuit is given in Table 1. There is a tradeoff between the power consumption, circuit linearity, and limit cycle frequency. The amount of power can be reduced if

an alternative voltage to current converter with lower current consumption is used in the comparator stage. It should be noted that the achieved SNR value can be increased by increasing the limit cycle frequency. For example, a 120 MHz operating loop will result in a higher SNR value.

Table 1. Performance results of the simulated asynchronous sigma-delta modulator circuit.

Technology	0.18 μm CMOS
Supply	1.8 V
Current used	790 μA
Power	1.42 mW
Limit cycle frequency	100 MHz
SNR (1 kHz–10 MHz)	68 dB
SFDR	75 dB
ENOB	11.00 bits

The achieved SNR value gives the possibility to extract up to 11.0 bits after the succeeding filter section. A figure of merit (FOM) value can be calculated to make a comparison with other continuous sigma-delta circuits in the literature [24,27]:

$$FOM = \frac{P}{2^{ENOB} \cdot (2BW)} \tag{10}$$

In Eq. (**??**), *ENOB* corresponds to effective number of bits and BW is the width of the band in which the *ENOB* value is obtained. The resulting FOM value for this design is calculated as 0.035 picoJ/conversion-level. To reinforce the potential of the asynchronous sigma-delta modulation, a FOM comparison with two of the top performance synchronous continuous time sigma-delta modulators and SC-DT (switched capacitor discrete time) will be useful [23–26]. The results are given in Table 2.

Table 2. Performance results comparison of the designed ASDM circuit with other sigma-delta modulators.

Designs	Work in [23]	Work in [24]	Work in [25]	Work in [26]	Work in [13]	This work
Technology (μm)	0.18	0.18	0.18	0.18	0.18	0.18
SNR (dB)	82	74	82	76.3	70	68
Bandwidth of interest (Hz)	10 M	10 M	2.2 M	3.2 M	8 M	10 M
Power consumption (W)	100 m	36 m	14 m	23.8 m	1.5 m	1.42 m
FOM (pJ/conversion level)	0.485	0.176 (circuit level)	0.112	0.696	0.036	0.035
Area (mm^2)	0.7	1.1	2.32	1.7	0.026	0.030
Sampling or limit cycle frequency (MHz)	640	320	144	80	140	100
Architecture and order	CT Fifth order	CT Third order	SC-DT Second order-4 bit	SC-DT Fourth order	ASDM First order	ASDM First order

It can be seen that the FOM value is better than that of the best performance continuous sigma-delta converters. The design and this type of architecture are superior to DT-SC also. In Table 2, it is also worth mentioning that the area of the proposed circuit is considerably smaller than that in other works, since other sigma-delta architectures employ higher order (third and fourth) filters to achieve high noise suppression for

the desired bandwidth. The area value, which is given for this work in Table 2, is a value calculated using the device sizes, technology layout rules of the process used, and space needed for routing.

As a final consideration, a comparison of qualitative performance metrics of SC-DT, CT, and ASDM is given in Table 3. It can be seen that ASDM is superior especially in the metrics of area and power.

Table 3. Comparison of sigma-delta architectures.

Sigma-delta architecture	DT-SC	CT	ASDM
SNR	high	high	high
Power	high	mid	low
Area	high	mid	low

5. Conclusion

In this paper, a new current mode asynchronous sigma-delta converter topology is presented. This work also proves the low component count and high performance properties of the asynchronous sigma-delta converter, as with previous work. With the proposed design in this paper, many advantages of the current-mode circuits can be utilized, such as high bandwidth, no slew rate limitations, low power consumption, and lower supply voltage dependency.

References

[1] Aziz PM, Sorensen HV, Van der Spiegel J. An overview of sigma delta converters. IEEE Signal Processing 1996; 13: 61-86.

[2] Norsworthy SR, Schreier R, and Temes GC. Delta-Sigma Data Converters: Theory, Design, and Simulation. New York, NY, USA: IEEE, 1997.

[3] Candy JC. A use of double integration in sigma delta modulation. IEEE T Commun 1985; 3: 249-258.

[4] Candy JC, Temes GC. Oversampling Delta-Sigma Data Converters. New York, NY, USA: IEEE Press Inc., 1992.

[5] Van der Zwan EJ, Dijkmans EC. A 0.2-mW CMOS modulator for speech coding with 80 dB dynamic range. IEEE J Solid-St Circ 1996; 31: 1873-1880.

[6] Cherry JA, Snelgrove MW. Clock jitter and quantizer metastability in continuous-time delta-sigma modulators. IEEE T Circuits Syst 2 1999; 46: 661-676.

[7] Atherton DP. Nonlinear Control Engineering Design. London, UK: Van Nostrand Reinhold Co., 1975.

[8] Gelb A, Van der Velde WE. Multiple-input Describing Functions and Non-Linear System Design. New York, NY, USA: McGraw-Hill, 1968.

[9] Green TC, Williams BW. Spectra of delta-sigma modulated inverters: an analytical treatment. IEEE T Power Electron 1992; 7: 644-654.

[10] Roza E. Analog-to-digital conversion via duty-cycle modulation, IEEE T Circuits Syst. 2 Analog Digit. Signal Process 1997; 44: 907-914.

[11] Toumazou C, Lidgey FJ, Haigh D. Analogue IC Design: the Current-mode Approach. London, UK: Peter Perigrinus Ltd., 1990.

[12] Toumazou C, Hughes JB, Battersby NC. Switched-Currents: An Analogue Technique for Digital Technology. London, UK: Peter Peregrinus Ltd., 1993.

[13] Ouzounov S, Roza E, Hegt J, Van der Weide G. Analysis and design of high- performance asynchronous sigma-delta modulators with a binary quantizer. IEEE J Solid-St Circ 2006; 41: 588-596.

[14] Hung CC, Ismail M, Halonen K, Porra V. A low-voltage rail-to-rail CMOS V-I converter. IEEE T Circuits Syst 2 1999; 46: 816-820.

[15] Van Zanten AT. An accurate integrated voltage-to-current converter. IEEE J Solid-St Circ 1975; 10: 432-436.

[16] Gopinathan V, Tarsia M, Choi D. Design considerations and implementation of a high frequency continuous-time filter and variable implementation of a programmable high-frequency continuous-time filter and variable gain amplifier in submicrometer CMOS. IEEE J Solid-St Circ 1999; 34: 1698-1707.

[17] Kimura K. A linear transconductance amplifier obtained by realizing a floating resistor. IEEE T Circuits Syst 1 1998; 45: 108-113.

[18] Chang S, Liu Y. A digitally calibrated CMOS transconductor with a 100 MHz bandwidth and 75-dB SFDR. IEEE T Circuits Syst 2 Exp. Briefs 2008; 55: 1089-1093.

[19] Ouzounov S, Roza E, Hegt J, Van der Weide G, Van Roermund A. A CMOS V-I converter with 75dB SFDR and 360 μW power consumption. IEEE J Solid-St Circ 2005; 40: 1527-1532.

[20] Chilakapati U, Fiez TS, Eshraghi A. A CMOS transconductor with 80-dB SFDR up to 10 MHz. IEEE J Solid-St Circ 2002; 37: 365-370.

[21] Smith SL, Sanchez-Sinencio E. Low voltage integrators for high-frequency CMOS filters using current mode techniques. IEEE T Circuits Syst-2 1996; 43: 39-48.

[22] Zele RH, Allstot DJ. Low-power CMOS continuous-time filters. IEEE J Solid-St Circ 1996; 31: 157-168.

[23] Yang W, Schofield W, Shibata H, Korrapati S, Shaikh A, Abaskharoun N. A 100mW 10MHz-BW CT $\Sigma - \Delta$ modulator with 87dB DR and 91dBcIMD. In: IEEE 2008 International SolidState Circuits Conference Digest of Technical Papers; 3–7 February 2008; San Francisco, CA, USA: IEEE. pp. 18-23.

[24] Hong K, Chiueh H. A 36-mW 320-MHz CMOS continuous-time sigma-delta modulator with 10-MHz bandwidth and 12-bit resolution. In: 2010 IEEE International Midwest Symposium on Circuits and Systems; August 1–4 2010; Seattle, WA, USA: IEEE. pp. 725-728.

[25] Kwon S, Maloberti FA. 14mW Multi-bit Delta-Sigma Modulator with 82dB SNR and 86dB DR for ADSL2+. In: 2006 IEEE Solid-State Circuits Conference; February 6–9 2006; San Francisco, CA, USA: IEEE. pp. 161-170.

[26] An 80/100MS/s 76.3/70.1dB SNDR Delta-Sigma ADC for Digital TV Receivers. In: 2006 IEEE Solid-State Circuits Conference; February 6–9 2006; San Francisco, CA, USA: IEEE. pp. 201-210.

[27] Janssen E, Van Roermund A. Look-Ahead Based Sigma-Delta Modulation. New York, NY, USA: Springer, 2011.