Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2016) 24: 5011 – 5024

doi:10.3906/elk-1410-175

Low leakage power gating technique for subnanometer CMOS circuits

Kavitha MANICKAM[1,*], **Govindaraj THANGAVEL**[2]
[1]Department of ECE, Government College of Engineering-Bargur, Krishnagiri, India
[2]Department of EEE, VSB Engineering College, Karur, India

Received: 03.11.2014 • **Accepted/Published Online:** 15.10.2015 • **Final Version:** 06.12.2016

Abstract: Static power has become the most important factor in the fabrication of integrated circuits. Power gating techniques minimize leakage currents and help to develop ultra-low–power and high-performance digital circuits. In this paper, a power gating approach is proposed to minimize leakage for subnanometer technologies. Simulation results reveal that the proposed technique reduces maximum of 96% leakage power, 33% dynamic power, 49% drowsy power, and 16% energy as compared to conventional techniques. The proposed technique offers good leakage reduction, even under variation of different operating parameters.

Key words: Leakage power, power gating, sleep mode, drowsy mode, charge recycling

1. Introduction

In this modern era, usage of battery-powered portable devices like laptops, mobile phones, and personal digital assistants (PDAs) has been increasing rapidly. Operation time of these devices is restricted by their battery lifetime, which has become a major motivation for low-power VLSI design [1–3]. Previously, the major concern of chip designers has been dynamic power consumption, as it accounted for about 99% of the total chip power. As transistors in modern CMOS technology have been scaled, leakage power is growing immensely, and it is nearing dynamic power.

Power gating is the most commonly used circuit technique for leakage power reduction in digital integrated circuits [4]. The power gating technique cuts off power to the circuit blocks when they are idle. Transistor-based power gating is implemented by placing sleep transistors in-line between the circuit and the power network or the ground network. Mutoh et al. proposed a power gating structure [5] that supports active and sleep modes; it is a state-destructive technique where the current output value of the circuit block might be lost. To preserve the data in the circuit block during idle periods, an intermediate data retention mode is required. Many power gating techniques [6–9] have been proposed for leakage reduction and data retention. In all these techniques, the charge gets stored at the gate of the sleep transistor during active mode. The stored charge is dumped to ground and is wasted during the transition from active to sleep mode. No attempt is made to reuse the charge at the gate of the sleep transistor.

A new power gating structure is proposed in this paper to suppress power consumption and provide data retention by charge recycling. In the proposed low-power multimodal switch (LPMS) power gating structure, the drowsy and sleep transistors form a stack pair to minimize power consumption. Virtual ground node voltage is boosted by charge recycling to support a data retention mode. Reduced power consumption reveals that the

*Correspondence: kavithaengr@gmail.com

proposed structure is effective in minimizing energy to a great extent. The rest of the paper is organized as follows: section 2 discusses previous power gating approaches. Section 3 describes the proposed technique, and section 4 presents the simulation methodology. Section 5 explains the results, and section 6 concludes the paper.

2. Previous work

Various power gating techniques exist in the literature with low leakage and data retention capability. In [10], Tada et al. presented the sleep buffer (SB) approach shown in Figure 1, which retains the data in drowsy mode by reusing the charge stored at the sleep transistor gate during active mode. Sleep mode is lost in the sleep buffer approach; it is suitable only when the circuit block switches between active and drowsy modes frequently. The charge recycling (CR) technique [11] shown in Figure 2 supports active, drowsy, and sleep modes. The layout area of the charge recycling process is smaller, but drowsy mode power consumption is very high. The trimodal switch technique (TMS) [12,13] shown in Figure 3 puts the circuit block in active, sleep, and drowsy modes depending on the control signals *sleep* and *drowsy.* The area requirement of the trimodal switch technique is high and leakage is also high, as there exists a sneak path from supply to ground through the drowsy transistors.

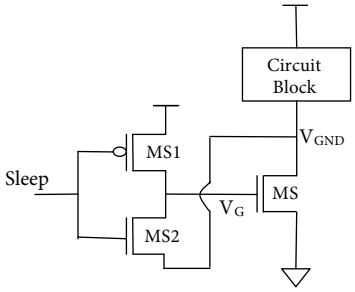

Figure 1. Sleep buffer (SB) approach.

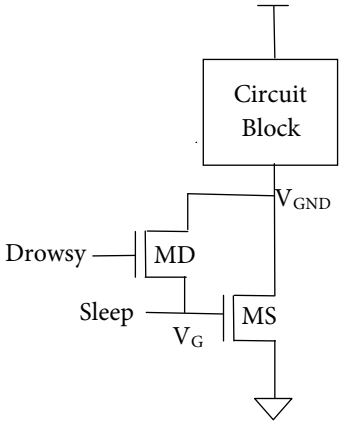

Figure 2. Charge recycling (CR) approach.

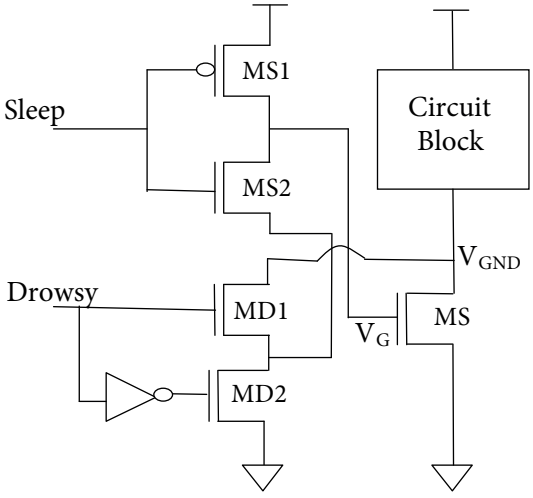

Figure 3. Trimodal switch (TMS) approach.

A low-power multimodal switch is proposed in this paper to support sleep mode and minimize power with minimum area overhead. By utilizing a drowsy transistor, LPMS technique supports sleep mode. By connecting the sleep buffer (*MS1* and *MS2*) to real ground through stacked pair transistors, the sneak path is eliminated in the LPMS technique. The power consumption, delay, power delay product (PDP), and area overhead of different power gating techniques are characterized in this paper. The impacts of sleep transistor width, sleep transistor threshold voltage, and temperature on power consumption are evaluated. The simulation results of the existing techniques show the potential benefits of the proposed LPMS technique in terms of power and performance.

3. Proposed technique

This section presents the circuit configuration and functionality of the proposed power gating technique. The circuit configuration of the low-power multimodal switch is shown in Figure 4, and its functionality is provided in Table 1. In LPMS, *MS1* and *MS2* transistors form the sleep buffer, *MD* is the drowsy transistor, and *MS* is the sleep transistor. The proposed technique has 2 control signals named *sleep* and *drowsy*. Based on the values of these control signals, the LPMS technique enables the circuit to operate in 3 modes, namely *Active*, *Sleep*, and *Drowsy*.

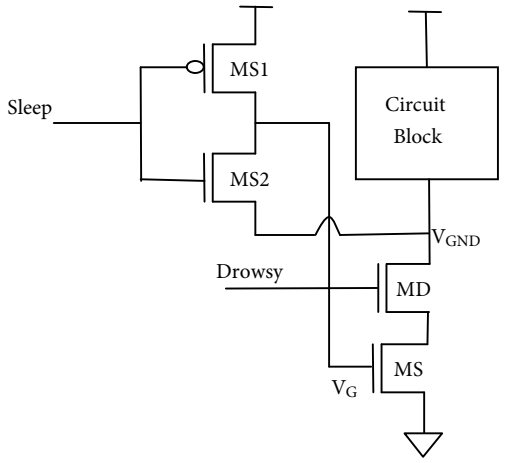

Figure 4. Low power multimodal switch (LPMS) approach.

Table 1. LPMS technique functionality.

Sleep	Drowsy	Circuit mode
0	1	Active
1	0	Sleep
1	1	Drowsy

The LPMS technique combines both the concept of power gating and the stack effect. The LPMS structure connects the circuit block with the ground rail during active mode and disconnects the ground rail in sleep mode. Transistors *MD* and *MS* are connected such that they form a stack pair to minimize power. Considering *MD* and *MS* along with the pulldown network of the circuit block, it is clear that the stack length results in higher power reduction.

Active mode: Active mode is also termed dynamic mode. In active mode, sleep signal is low and drowsy signal is high. Transistors *MS1*, *MD*, and *MS* are *on* and electrical charge gets stored at V_G. Voltage across

the circuit block is approximately V_{DD} which enables its normal operation. In active mode, virtual ground (V_{GND}) voltage level is approximately 0.

Drowsy mode: Drowsy mode is an intermediate power-saving mode and is meant for retaining data. Virtual ground voltage should be increased to maintain sufficient voltage across the circuit block for data retention. In LPMS, virtual ground voltage is raised by reusing the charge stored at V_G through *MS2*. Charge recycling takes place until the voltages of V_{GND} and V_G are equalized to V_{CR} ($0 < V_{CR} < V_{DD}$). The voltage across circuit block turns out to be ($V_{DD} - V_{CR}$), and this significant voltage helps to retain the data in it. In this paper, only estimation of drowsy power is considered. Power consumption in drowsy mode is less than in active mode.

Sleep mode: When the sleep signal is high and drowsy signal is low, transistors *MD* and *MS* are in the *off* state. *MD* and *MS* form a transistor stack; due to this, *Vgs* of *MD* and *Vds* of *MS* are affected. *Vgs* of *MD* is minimized due to body effect, making *MD* enter strongly into the cutoff region. Because of the stack effect, drain voltage of *MS* is lowered, thereby minimizing *Vds* of *MS*. As leakage current depends on the values of *Vgs* and *Vds*, a reduction in these voltages leads to leakage power reduction in LPMS.

4. Experimental methodology

LPMS technique is applied to various generic logic circuits to show that it is applicable to generic logic design. Three benchmark circuits—(i) a 4-bit adder, (ii) a 4:1 multiplexer, and (iii) a chain of 3 inverters—were considered for experimentation. In order to compare the results of the proposed approach with existing leakage reduction approaches, experiments include the techniques discussed in section 2, namely, sleep buffer, charge recycling, and trimodal switch approaches.

Schematics and layouts are designed in 90 nm technology for all considered techniques using digital schematic editor and simulator (DSCH) and Microwind tool. The net lists generated from layouts are modified to fit into all targeted silicon technologies using the predictive technology models (PTM) [14] for 32, 45, 65, 90, and 130 nm processes. Synopsys HSPICE simulation is used to estimate delay and power consumption. The simulation procedure is summarized in Figure 5.

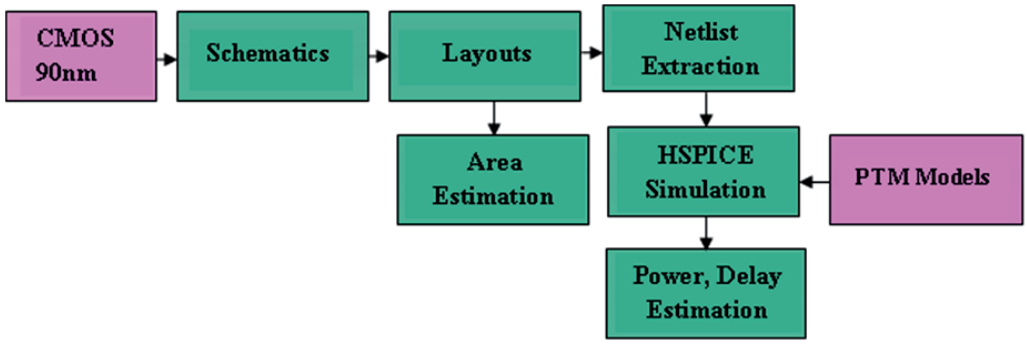

Figure 5. Experimental methodology.

5. Experimental results

Leakage, dynamic, and drowsy power analyses are presented in sections 5.1, 5.2, and 5.3, respectively. Propagation delay analysis is done in section 5.4. Energy consumption of different power gating techniques is discussed in section 5.5. Impact of sleep transistor width, threshold voltage, and temperature on leakage and drowsy

power is estimated for the 4-bit adder designed in 65-nm technology, and the results are analyzed in sections 5.6, 5.7, and 5.8, respectively. Layout of generic circuits and area comparison are presented in section 5.9.

5.1. Leakage power analysis

As leakage power varies according to input state, a subset of possible input combinations are considered to estimate static power. All 8 possible input vectors of a full adder are considered for leakage power measurement. Out of 128 possible input combinations, 8 random input vectors are considered for the 4:1 multiplexer, as shown in Table 2. For the chain of 3 inverters, 2 input vectors, '1' and '0', are considered. When an input vector is asserted, power consumption is measured after the signal becomes stable (e.g., after 50 ns). Leakage power consumption of each circuit is derived by averaging power consumption for all input combinations.

Table 2. Input sets for a 4:1 multiplexer leakage power measurement.

I_0	I_1	I_2	I_3	S_0	S_1	E
0	0	0	0	0	0	0
1	0	0	0	0	0	0
1	0	0	0	0	0	1
1	0	0	0	0	0	1
1	1	0	1	0	1	1
1	1	0	1	1	1	1
1	1	0	1	1	1	0
1	1	1	1	1	1	1

Leakage power consumption of the 4:1 multiplexer is shown in Figure 6. Leakage of TMS and CR is high compared to the LPMS technique. The proposed LPMS technique offers high leakage reduction compared to other power gating techniques; this is due to the stacked pair of transistors, *MD* and *MS*. Stack effect: 2 series connected MOS devices that are *off* have significantly reduced leakage compared to a single *off* device [1]. The leakage reduction due to the stack effect can be illustrated mathematically by solving for the stack effect factor, which is defined as the ratio of leakage in a single *off* transistor to the leakage in a stack of 2 *off* transistors [15].

Consider the LPMS stack pair shown in Figure 7, and let I_{off} be the leakage of a single MOS transistor of unit width in the *off* state, with its $V_{gs} = V_{bs} = 0$ and $V_{ds} = V_{dd}$. If the gate drive, body bias, and drain to source voltages are minimized by $\Delta V_g, \Delta V_b$, and ΔV_d respectively, then assuming $V_{ds} > 3kT / q$, the leakage reduces to

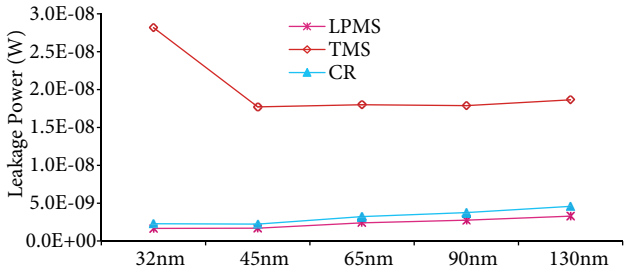

Figure 6. 4:1 multiplexer leakage power.

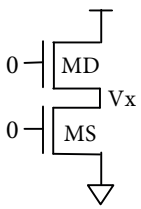

Figure 7. Stack effect in LPMS technique.

$$I_1^{'} = I_1 10^{-\frac{1}{S}[\Delta V_g + \lambda_d \Delta V_d + k_\gamma \Delta V_b]}, \tag{1}$$

where S is the subthreshold swing, λ_d is the drain induced barrier lowering (DIBL) factor, and k_γ is the body effect coefficient. In Figure 7, intermediate node voltage V_x attains a steady state condition when the leakage currents in the transistors *MD* and *MS* are equal. Under these conditions, the leakage currents in *MD* and *MS* are given by

$$I_{stack-MD} = W_{MD} I_1 10^{\frac{-(1+\lambda_d+k_\gamma)V_x}{S}} \tag{2}$$

$$I_{stack-MS} = W_{MS} I_1 10^{\frac{-\lambda_d(V_{dd}-V_x)}{S}}, \tag{3}$$

and the intermediate node voltage is

$$V_x = \frac{\lambda_d V_{dd} + S \log \frac{W_{MD}}{W_{MS}}}{1 + k_\gamma + 2\lambda_d} \tag{4}$$

For short channel devices, k_γ ¡¡ $1 + 2\,\lambda_d$; hence V_x of the intermediate node voltage is approximately given by

$$V_x \approx \frac{\lambda_d V_{dd} + S \log \frac{W_{MD}}{W_{MS}}}{1 + 2\lambda_d}. \tag{5}$$

Substituting V_x in either Eq. (3) or Eq. (4) will yield leakage in 2 stacked transistors.

$$I_{stack} = W_{MD}^{\alpha} W_{MS}^{1-\alpha} I_1 10^{\frac{-\lambda_d V_{dd}}{S}(1-\alpha)} \tag{6}$$

where $\alpha = \frac{\lambda_d}{1+2\lambda_d}$.

The leakage reduction that can be obtained in a 2-transistor stack with widths W_{MD} and W_{MS} compared to a single transistor with width W is given by

$$X = \frac{I_{device}}{I_{stack}} = \frac{W}{W_{MD}^{\alpha} W_{MS}^{1-\alpha}} 10^{\frac{\lambda_d V_{dd}}{S}(1-\alpha)} \tag{7}$$

When $W_{MD} = W_{MS} = W$, the stack factor X can be rewritten as

$$X = 10^{\frac{\lambda_d V_{dd}}{S}(1-\alpha)}, \tag{8}$$

or

$$X = 10^{\frac{\lambda_d V_{dd}}{S}\left(\frac{1+\lambda_d}{1+2\lambda_d}\right)} = 10^{U}, \tag{9}$$

where U is the universal 2-stack exponent, which depends on the parameters λ_d, S, and V_{dd}. From Eq. (9), it can be observed that leakage is highly alleviated in a stacked pair of MOS devices in comparison to a single device. No sneak path exists in the LPMS structure as the source of *MS2* is connected to ground through the stacked transistors, resulting in further leakage reduction. The sleep buffer approach is not included in the leakage power estimation, as sleep mode is not supported by it.

5.2. Dynamic power analysis

Active power is estimated by asserting semirandom input signals and calculating the average power dissipation during this time. Inputs are chosen so that a large number of possible input combinations are included in the set. The average power dissipation reported by HSPICE is taken as the estimate of active power consumption.

For the 4-bit adder, the input vectors are asserted, covering every possible input. For the 4:1 multiplexer, the input vectors are chosen to represent a sample of possible inputs, with at least 4 of the 7 input bits at every clock cycle change. The active power of the chain of 3 inverters is measured by asserting a pulse signal of 25-MHz frequency.

The dynamic power consumption of different power gating techniques for a 4:1 multiplexer is shown in Figure 8, which reveals that power reduction is high in LPMS as compared to other power gating techniques. The dynamic power of sleep buffer, charge recycling, and TMS approaches is the same. LPMS virtual ground voltage is influenced by the *on* resistance of 2 transistors (*MD* and *MS*), whereas in other power gating techniques, virtual ground voltage is influenced by the *on* resistance of a single sleep transistor. Hence, the LPMS technique offers higher dynamic power reduction, as the voltage across the logic circuit blocks is lower due to higher virtual ground voltage.

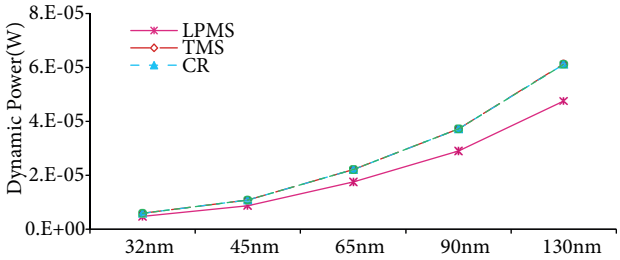

Figure 8. 4:1 multiplexer dynamic power

5.3. Drowsy power analysis

Drowsy mode is an intermediate power-saving mode introduced to retain data if the circuit block remains idle for a short duration. A subset of possible input combinations that are used for estimating leakage power is considered for measuring drowsy power. The circuit block is made to switch from active to drowsy mode, and the drowsy power is estimated for 50 ns.

When the circuit switches to drowsy mode, charge recycling takes place between V_{GND} and V_G nodes, making the sleep transistor partially *on*; current flows from virtual ground node to real ground node. V_{GND} voltage reaches equilibrium at a balance point of the leakage current of the internal circuits and the current through the transistors between virtual ground and real ground nodes. Due to the stack effect, equilibrium virtual ground voltage of LPMS technique is higher than other techniques; hence, drowsy power is decreased to a greater extent.

Figure 9 shows the results for 4:1 multiplexer drowsy power as the technology scales from 130 nm to 32 nm. Drowsy power of the CR technique is higher than that of other techniques, and drowsy power of the trimodal switch is higher in the sleep buffer and LPMS techniques. It is evident from Figure 9 that the LPMS technique is suitable for minimizing drowsy power compared to sleep buffer, charge recycling, and trimodal switch approaches.

5.4. Delay analysis

The propagation delay is estimated as the time between the input edge reaching 50% of supply voltage to the circuit output edge reaching 50% of supply voltage. Figure 10 reveals that the delay of the 4:1 multiplexer decreases as technology scales down. The delay of SB, CR, and TMS is less than that of the LPMS technique.

Propagation delay of the LPMS technique is higher than other techniques as it employs a stacked pair of transistors.

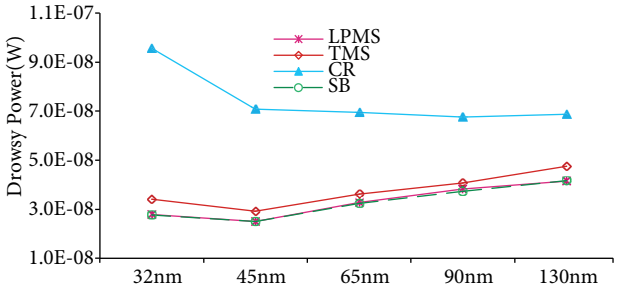

Figure 9. 4:1 multiplexer drowsy power.

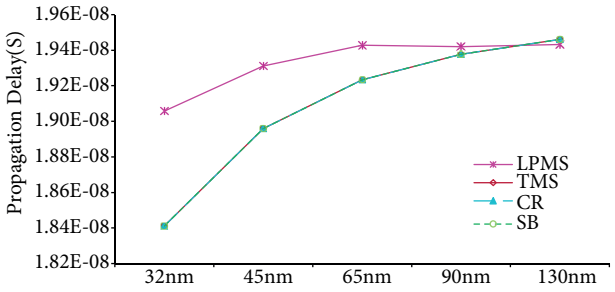

Figure 10. 4:1 multiplexer propagation delay.

The analytical delay model of a stacked inverter can be compared with the conventional inverter to show that the stack effect increases delay. Figure 11 shows the conventional inverter and its RC equivalent circuit, where C_L is the load capacitance, R_t is the transistor resistance, and C_{in} indicates the input capacitance. Generally, transistor delay of the conventional inverter [16] is given by

$$T_d = R_t C_L. \tag{10}$$

The stacked inverter can be realized by replacing the single MOS device with 2 MOS devices. Figure 12 shows the stacked inverter and its RC equivalent circuit. C_x represents the internal node capacitance between the 2 pulldown transistors. Using the Elmore equation, the delay of stacked inverter is

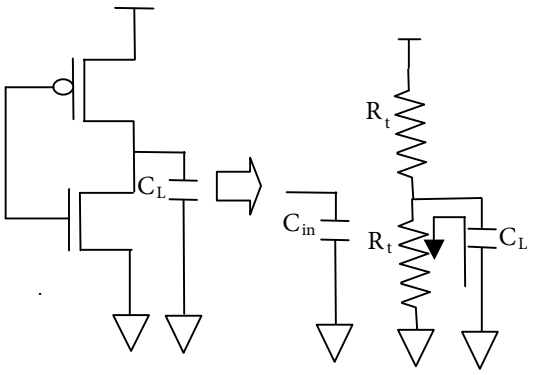

Figure 11. Inverter and its RC equivalent circuit.

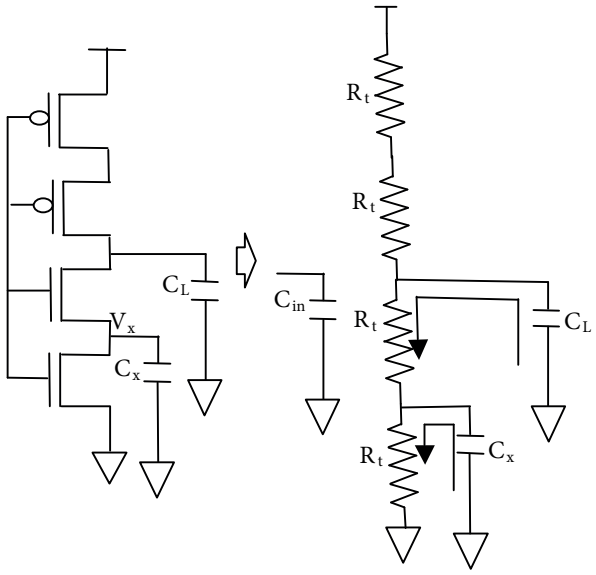

Figure 12. Stacked inverter and its RC equivalent circuit.

$$T_{d-stack} = (R_t + R_t)C_L + R_t C_x, \tag{11}$$

$$T_{d-stack} = 2R_t C_L + R_t C_x. \tag{12}$$

It can be observed from Eqs. (10) and (12) that the delay of a circuit increases due to the stack effect.

5.5. Power delay product analysis

Power delay product (PDP) defines the energy consumed by the circuit block, and it is necessary to minimize the energy overhead. PDP is estimated by multiplying the propagation delay with the dynamic power. Figure 13 shows the impact of technology scaling on the energy consumption of the 4:1 multiplexer. The energy overhead decreases as the device size shrinks. The PDP of TMS, sleep buffer, and charge recycling techniques is the same; the power delay product of the LPMS technique is less due to its low power consumption compared to other power gating techniques.

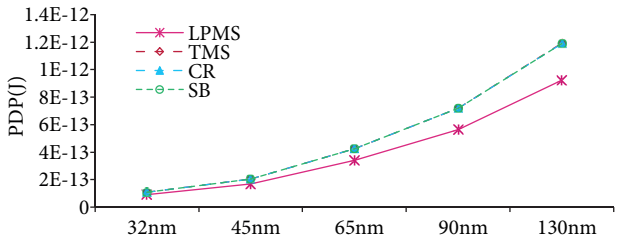

Figure 13. 4:1 multiplexer PDP.

Table 3 lists the results for 32 nm technology implementation of each benchmark circuit. It is evident from Table 3 that the proposed LPMS technique minimizes dynamic, drowsy, and leakage power significantly as compared to other power gating techniques for all of the generic logic circuits, like a chain of 3 inverters, the 4-bit adder, and the 4:1 multiplexer. For instance, considering the results of a chain of 3 inverters implemented in 32 nm technology, the LPMS approach provides a reduction of up to 2% drowsy power, 33% dynamic power, and 15% energy compared to the sleep buffer technique. As compared to the CR technique, LPMS provides 9% reduction in leakage, 49% reduction in drowsy power, 33% reduction in dynamic power, and 16% reduction in energy. Compared to the TMS technique, a reduction of about 96% leakage, 47% drowsy power, 33% dynamic power, and 15% energy is obtained in LPMS. The delay of the LPMS approach is 26.8%, 25.7%, and 26.1% higher than TMS, CR, and SB techniques, respectively.

5.6. Impact of sleep transistor width scaling

Transistor width scaling increases power consumption. In this section, leakage and drowsy power of different power gating techniques are characterized, with varying sleep transistor width. Figure 14 shows that leakage power increases as sleep transistor width is varied from 1 μ m to 10 μ m. Leakage power of the LPMS technique is significantly less than charge recycling and the trimodal switch approach for all sleep transistor sizes. As sleep transistor width changes from 1 μ m to 10 μ m, leakage power minimization of LPMS varies from 87% to 90% and 78.5% to 88% compared to TMS and CR techniques, respectively. Figure 15 shows the simulation results of 4-bit adder drowsy power with varying sleep transistor width. Due to the stack effect of *MD* and *MS*, the LPMS technique consumes less drowsy power than sleep buffer, charge recycling, and trimodal switch techniques. LPMS technique minimizes drowsy power by approximately 49% more than the TMS technique and 10% more than sleep buffer and charge recycling techniques for all sleep transistor sizes ranging from 1 μ m to 10 μ m.

Table 3. Power, delay, and PDP estimation (32 nm).

A chain of 3 inverters	Static power (W)	Drowsy power (W)	Dynamic power (W)	Propagation delay (S)	PDP (J)
LPMS	1.11E–09	1.49E–08	6.49E–08	4.39E–11	2.85E–18
TMS	2.72E–08	2.81E–08	9.73E–08	3.46E–11	3.37E–18
CR	1.23E–09	2.93E–08	9.72E–08	3.49E–11	3.38E–18
SB	_	1.53E–08	9.73E–08	3.48E–11	3.37E–18
4:1 multiplexer	Static power (W)	Drowsy power (W)	Dynamic power (W)	Propagation delay (S)	PDP (J)
LPMS	1.66E–09	2.73E–08	4.75E–06	1.91E–08	9.07E–14
TMS	2.82E–08	3.41E–08	5.89E–06	1.84E–08	1.09E–13
CR	2.25E–09	9.16E–08	5.88E–06	1.84E–08	1.08E–13
SB	_	2.77E–08	5.88E–06	1.84E–08	1.08E–13
4-bit adder	Static power (W)	Drowsy power (W)	Dynamic power (W)	Propagation delay (S)	PDP (J)
LPMS	3.03E–09	8.56E–08	1.75E–06	1.93E–09	3.38E–15
TMS	3.07E–08	9.27E–08	2.16E–06	1.62E–09	3.49E–15
CR	4.75E–09	3.56E–07	2.15E–06	1.62E–09	3.48E–15
SB	_	8.59E–08	2.15E–06	1.97E–09	4.24E–15

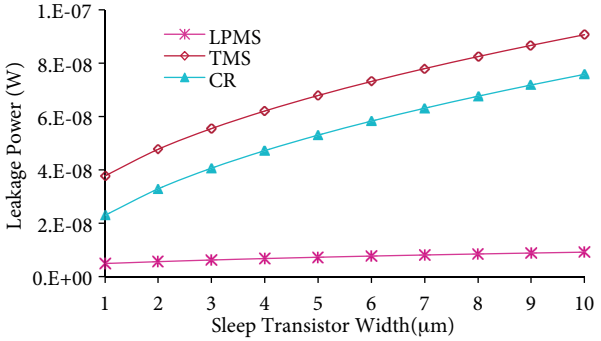

Figure 14. Effect of transistor width on 4-bit adder leakage power.

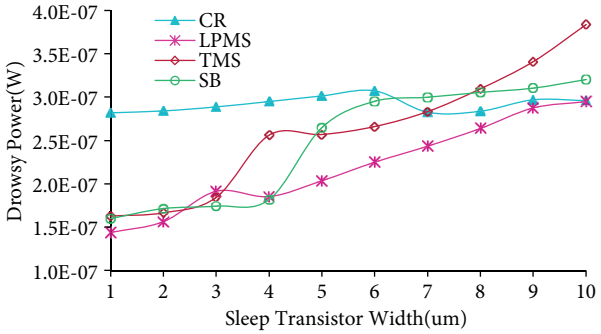

Figure 15. Effect of transistor width on 4-bit adder drowsy power.

5.7. Impact of sleep transistor threshold voltage

Choosing the right threshold value for the sleep transistor is very important in terms of power consumption. In this section, leakage and drowsy power of different power gating techniques are compared by varying the threshold voltage of sleep transistors. Figure 16 shows the measured leakage power results of the 4-bit adder while varying *Vth*. As the sleep transistor threshold voltage is increased from 0.3 to 0.5 V, leakage power decreases. The leakage power of charge recycling and the TMS approach reduces drastically as the sleep transistor threshold voltage increases, but the leakage is still higher than that of LPMS technique. At a threshold value of 0.3 V, LPMS leakage consumption is approximately 95% less than the CR and TMS approaches. At *Vth* of 0.5 V, leakage of LPMS is 49% and 80% less than CR and TMS techniques, respectively. Figure 17 shows the estimated drowsy power results with varying sleep transistor threshold voltage. The drowsy power of the charge recycling technique is higher than that of other power gating techniques. The drowsy power of sleep buffer and trimodal switch is the same. When the transistor threshold voltage is 0.5 V, the LPMS technique offers a maximum drowsy power reduction of about 13% to 16% compared to SB and TMS techniques, respectively.

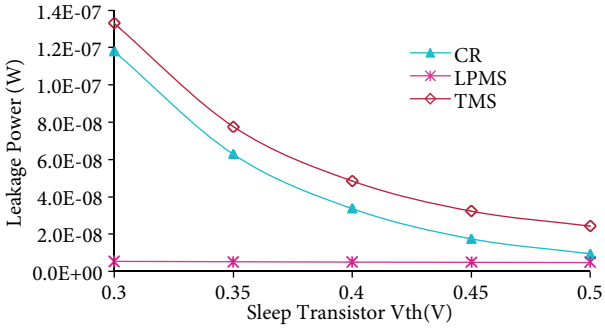

Figure 16. Effect of Vth on 4-bit adder leakage power.

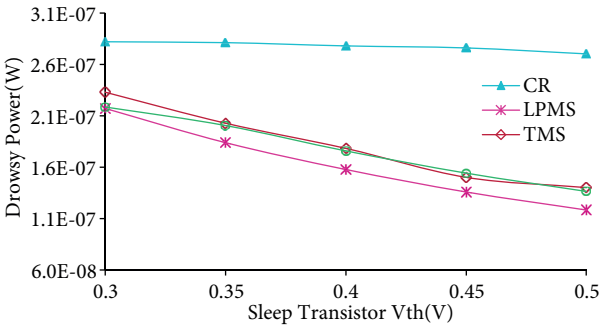

Figure 17. Effect of Vth on 4-bit adder drowsy power.

5.8. Impact of temperature

The impact of temperature on leakage and drowsy power of the 4-bit adder is presented in this section. Temperature affects the leakage power of digital circuits adversely, as subthreshold leakage increases with temperature. Figure 18 shows the effect of temperature on leakage power. The leakage power consumption of TMS is approximately 80% more than that of LPMS technique at 100 °C. Leakage power reduction of LPMS varies from 32% to 79.6% compared to charge recycling technique as the temperature changes from

0 °C to 100 °C. Figure 19 shows the impact of temperature on 4-bit adder drowsy power. Charge recycling technique has the highest drowsy power consumption compared to other power gating techniques. At 100 °C, TMS technique's drowsy power is 5% more than that of LPMS technique. Sleep buffer and LPMS techniques consume approximately the same amount of drowsy power.

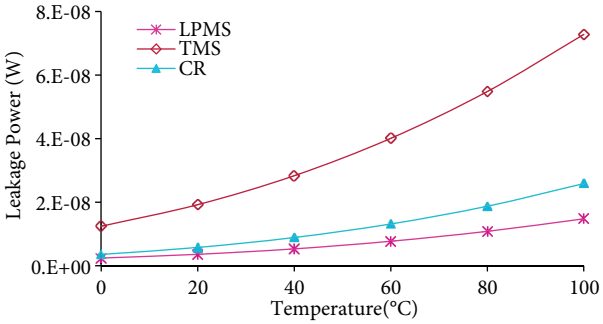

Figure 18. Impact of temperature on 4-bit adder leakage power.

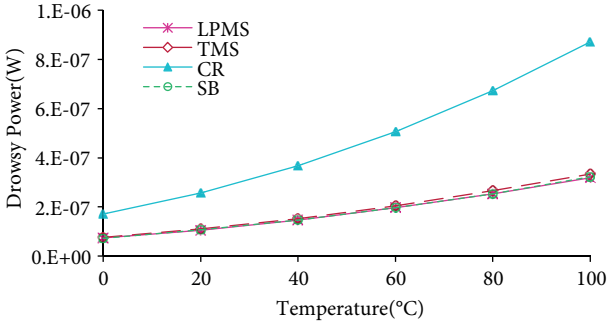

Figure 19. Impact of temperature on 4-bit adder drowsy power.

Results and analysis in sections 5.6, 5.7, and 5.8 show that the proposed LPMS technique's performance is better in terms of leakage and drowsy power reduction than other power gating techniques, even if the operating parameters changes.

5.9. Layout area comparison

Comparison of the layout area of logic circuits with different power gating techniques is presented in this section. The layouts are drawn with Microwind layout tool using 90 nm technology. Figure 20 represents the layout of the 4:1 multiplexer and 4-bit adder using LPMS technique, respectively. The layout areas of the chain of 3 inverters, 4-bit adder, and 4:1 multiplexer with different power gating techniques are listed in Table 4. Considering the chain of 3 inverters, the charge recycling technique has the smallest layout area among all the power gating techniques that are evaluated in this paper. Sleep buffer technique has an area overhead of about 20.6% compared to charge recycling technique. As the TMS approach uses 4 transistors in its drowsy section, its area overhead is 48.6% and 23% higher than sleep buffer and charge recycling techniques, respectively. Although the LPMS technique suffers from greater area overhead of about 36% and 13% than CR and SB techniques, respectively, the area requirement of LPMS is 8% less than that of the TMS technique.

Table 4. Transistor count and area comparison (90 nm).

Tech.	Chain of 3 inverters			4:1 multiplexer			4 bit adder		
	NMOS	PMOS	Area (μ m^2)	NMOS	PMOS	Area (μ m^2)	NMOS	PMOS	Area (μ m^2)
LPMS	6	4	166.5	35	33	326.9	45	43	392.4
TMS	8	5	181.3	37	34	341.7	47	44	407.2
CR	5	3	122.1	34	33	282.4	44	42	347.9
SB	5	4	147.2	34	33	307.6	44	43	373.1

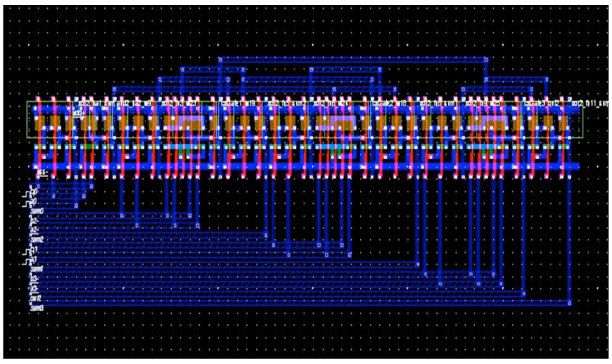

Figure 20. Layout of 4:1 multiplexer.

6. Conclusion

In this paper, an effective power gating technique to reduce leakage, drowsy and dynamic power in generic logic circuits is proposed. It is apparent from the power characteristics that the LPMS approach is better than conventional techniques. The LPMS technique also minimizes energy consumption to a maximum of about 16% over other approaches. The proposed LPMS technique provides excellent leakage and drowsy power reduction even when sleep transistor width, threshold voltage, and temperature change. LPMS technique can be used in applications like wireless sensor nodes, SoC, and microprocessors to extend the battery life of these devices.

References

[1] Keating M, Flynn D, Aitken R, Gibbons A, Shi K. Low Power Methodology Manual for System on Chip Design. New York, NY, USA: Springer, 2007.

[2] Taur Y. CMOS design near the limit of scaling. IBM J Res Dev 2002; 46: 213-222.

[3] Lorenzo R, Chaudhary S. A novel all NMOS leakage feedback with data retention technique. In: IEEE 2013 International Conference on Control, Automation, Robotics and Embedded Systems; 16–18 December 2013; Jabalpur, India. Piscataway, NJ, USA: IEEE. pp. 1-5.

[4] Khoshavi N, Ashraf RA, DeMara RF. Applicability of power-gating strategies for aging mitigation of CMOS logic paths. In: IEEE 2014 57th International Midwest Symposium on Circuits and Systems; 3–6 August 2014; College Station, Texas. Piscataway, NJ, USA: IEEE. pp. 929-932.

[5] Mutoh S, Douseki T, Matsuya Y, Aoki T, Shigemitsu S, Yamada J. 1-V power supply high-speed digital circuit technology with multi threshold-voltage CMOS. IEEE J Solid-St Circ 1995; 30: 847-854.

[6] Kim S, Kosonocky SV, Knebel DR, Stawiasz K, Papaefthymiou MC. A multi-mode power gating structure for low-voltage deep-submicron CMOS ICs. IEEE T Circuits-II 2007; 54: 586-590.

[7] Jiao H, Kursun V. Ground bouncing noise suppression techniques for data preserving sequential MTCMOS Circuits. IEEE T VLSI Syst 2011; 19: 763-773.

[8] Chowdhury MH, Gjanci J, Khaled P. Controlling ground bounce noise in power gating scheme for system-on-a-chip. In: 2008 IEEE Computer Society Annual Symposium on VLSI; 7–9 April 2008; Montpellier, France. Los Alamitos, CA, USA: IEEE. pp. 437-440.

[9] Abdollahi A, Fallah F, Pedram M. An effective power mode transition technique in MTCMOS. In: IEEE 2005 42nd Design Automation Conference; 13–17 June 2005; Anaheim, CA. New York, NY, USA: IEEE. pp. 37-42.

[10] Tada H, Notani, Numa M. A novel power gating scheme with charge recycling. IEICE Electron Expr 2006; 12: 281-286.

[11] Liu Z, Kursun V. Low energy MTCMOS with sleep transistor charge recycling. In: IEEE 2007 50^{th} Midwest Symposium on Circuits and Systems; 5–8 August 2007; Montreal, Quebec. Piscataway, NJ, USA: IEEE. pp. 891-894.

[12] Pakbaznia E, Pedram M. Design and application of multi modal power gating structures. In: IEEE 2009 International Symposium on Quality Electronic Design; 16–18 March 2009; San Jose, CA. Piscataway, NJ, USA: IEEE. pp. 120-126.

[13] Pakbaznia E, Pedram M. Design of a tri-modal multi-threshold CMOS switch with application to data retentive power gating. IEEE T VLSI Syst 2012; 20: 380-385.

[14] Zhao W, Cao Y. New generation of predictive technology model for sub-45 nm early design exploration .IEEE T Electron Dev 2006; 53: 2816-2823.

[15] Narendran S, Borkar S, De V, Antoniadis D, Chandrakasan A. Scaling of stack effect and its application for leakage reduction. In: IEEE 2001 International Symposium on Low Power Electronics and Design; 6–7 August 2001; Huntington Beach, CA, USA. New York, NY, USA: IEEE. pp. 195-200.

[16] Park J. Sleepy stack: a new approach to low power VLSI and memory. PhD, Georgia Institute of Technology, Atlanta, GA, USA, 2005.