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Research Article

FPGA implementations of scale-invariant models of neural networks

Zeinulla ZHANABAEV, Yeldos KOZHAGULOV, Dauren ZHEXEBAY*

Department of Solid State Physics and Nonlinear Physics, Faculty of Physics and Technology, al-Farabi Kazakh National University, Almaty, Kazakhstan

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Abstract: Integrated circuit implementations of new models of neural networks with scale-invariant properties are presented. The specifics of such models are necessary in analysis of discrete mappings containing fractional power. We suggest an algorithm for increasing the power of a physical value by using a field-programmable gate array (FPGA). Comparisons between FPGA implementations and numerical results are demonstrated.

Key words: Neural networks, field-programmable gate array, digital scheme, scale invariance

1. Introduction

Neural networks are the most common type of intelligent system implementations. However, an actual problem is to study models of neural networks by using modern digital devices such as the field-programmable gate array (FPGA). This approach lets us simplify the structural realization and increases computational efficiency. Some works [1–7] were devoted to the modeling of neuronal dynamics based on digital technology of the FPGA. Qualitative and quantitative comparison of the FPGA with alternatives (for example, XC5VLX330T compared with Core2/3GHz and GT200/1.2GHz) were given in [1–4]. In the case of solving complex problems we have a clear superiority of the approach in time and productivity. Thus, the implementation of neural networks on the Xilinx Virtex-5 FPGA demonstrates computational speed 24.3 times higher than that of the corresponding software [5]. A number of new properties of neuron oscillations, including existence of their hierarchical levels, were established in [8]. For example, in contrast to the equations used in recent papers [6,7], the dynamic system suggested in [8] contains a fractional power of variables. As is known, the FPGA does not include the operation of raising a random fractional power. The presented research is focused on the possibilities of integrated-circuit engineering realizations of scale-invariant models of neural networks, which takes into account fractional power. Notice that scaling means the self-similarity of the structural elements of the object of large and small scales.

2. Models of neural network elements and algorithms for their circuit realizations

The well-known models of neural oscillations [6,7] (FitzHugh–Nagumo, Hindmarsh–Rose) and a scale-invariant model of neural networks [8] have been chosen as testing models of neural networks. The hardware part has been realized on the basis of the evaluation board ANVYL FPGA with an integrated circuit made by the XILINX company (set Spartan 6). The digital output signal has been obtained in the form of FPGA 8 bit code data. We used the toolbox Simulink (MATLAB) for output of numerical and graphical data.

^{*}Correspondence: zhexebay92@mail.ru

Equations for the description of oscillations of neurons according to the FitzHugh–Nagumo model [6] can be written as:

$$\dot{v} = v - \frac{v^3}{3} - w + I_{ext} \tau * \dot{w} = v + a - b * w,$$
(1)

where v is membrane potential; w is the variable of recovery; I_{ext} is the current value of stimulus; parameters $a, b, \tau > 0$; and \dot{v} is a derivative of the potential at time t.

Equations describing the Hindmarsh–Rose model [7] have the following form:

$$\begin{aligned} \dot{x} &= y - a * x^3 + b * x^2 - z + I \\ \dot{y} &= c - d * x^2 - y \\ \dot{z} &= r * [s * (x - x_R) - z], \end{aligned} \tag{2}$$

where I simulates the value of input current to membranes of biological neurons; b allows switching between bursting and spiking behaviors and controls the frequency of spikes; r controls the rate of variation of the slow variable z (i.e. efficiency of slow channels in exchanging of ions); parameters a, b, c, and d control the rate of change of variables x and y; s governs adaptation; x_R establishes resting potential of the system; and \dot{x} , \dot{y} , \dot{z} are derivatives at time t.

First we obtained experimental results based on the FPGA (Figures 1 and 2) for the systems in Eqs. (1) and (2), and we compared them with the corresponding numerical realizations of dynamic systems (Figures 3 and 4). We noticed that the experimental results corresponded to numerical results.



Figure 1. Block diagram FitzHugh–Nagumo model with parameters $I_{ext} = 0.5$, $\tau = 12.5$, a = 0.7, b = 0.8.

Equations for scale invariance models of neural networks include the basic properties of neurons [8]. Three methods for simulation of neural networks have been considered. In the first case an external field affects every object under study as a modulation-periodic signal:

$$V_{i+1}^{(k)} = V_0^{(k)} \left(\left| 1 - F^{(k)}(t) \middle/ \sum_{k=1}^N V_i^{(k)} \right| \right) - \gamma^k$$
(3)



Figure 2. Block diagram of Hindmarsh-Rose model with parameters a = 1, b = 3, c = 1, d = 5, s = 4, $x_R = -8/5$, $r = 10^{-3}$, I = 2.



Figure 3. The numerical implementation (a) and experimental results (b) of the FitzHugh–Nagumo model.

where V_i is the action potential of neurons, V_0 is the threshold excitation potentials, k is the ordinal number of a neuron, and i is the number of iterations necessary to determine value $V^{(k)}$. The external field is taken as a modulation-periodic signal:

$$F(t) = A(1 + B\sin(\Omega t)), \tag{4}$$

where A, B, and Ω are amplitude, coefficient of depth, and frequency modulation of neural oscillations, respectively, and $\gamma_k = D_k - d_k$ are fractional values. Here D_k and d_k are fractal and topological dimensions for the description of the geometry of a neuron with number k.



Figure 4. Numerical implementation (a) and experimental results (b) of the Hindmarsh–Rose model.

If $\gamma_k = 0$, then $V_{i+1}^{(k)}(t)$ will be a nonfractal, regular measure. If $\gamma_k \neq 0$, then $V_{i+1}^{(k)}(t)$ will be a onedimensional fractal curve with fractal dimension $D_t > 1$, $d_t = 1$, i.e. $\gamma = D_t - d_t$, that is not necessarily equal to γ_k .

In the second method we have taken into account that action potential of a neuron depends on a boundary neuron, and a modulation-periodic external field acts only on the first neuron $(V^{(1)} = F, k \ge 2)$:

$$V_{i+1}^{(k)} = V_0^{(k)} \left(\left| 1 - V_i^{(k-1)} \middle/ \sum_{k=1}^N V_i^{(k)} \right| \right) - \gamma^k.$$
(5)

The third method takes into account the multilayer structure of neural networks with a hierarchical structure with $\operatorname{order} n$:

$$V_n = f\left(\dots f\left(\frac{V_0}{n}, V_n\right) \dots\right), \ f(V_0, V) = V_0\left(\left|1 - \frac{F(t)}{V}\right|\right)^{-\gamma}, \ n = 1, 2, \dots,$$
(6)

where the number of brackets equal to $n, V_{n,i+1}^{(k)}$ is given by Eq. (3).

A block diagram of circuit implementation according to Eq. (3) is shown in Figure 5. The model consists of three interconnected neurons (dotted line). A modulation-periodic external field is applied on the neurons.

Figure 6 shows the block diagram for a signal raised in arbitrary fractional power on digital logic elements. There are no blocks for exponentiation to an arbitrary fractional power in the FPGA, just properties of exact roots. An algorithm for computing the fractional power γ on the FPGA can be written as

$$\gamma = \sum_{k=1}^{m} a_k * (2)^{-k}, \tag{7}$$

where kk is the number of iterations and $a_k a_k$ is equal to $\{0,1\}$. If the values of elements $a_k a_k$ are defined, we can obtain any fractional power of signal x with the desired accuracy:

$$x^{\gamma} = \prod_{k} x^{\gamma_{k}} = \prod_{k=1}^{m} x^{a_{k} * (2)^{-k}}.$$
(8)

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Figure 5. Block diagram of the implementation on FPGA scale-invariant model of neural networks for the systems of Eq. (3).



Figure 6. Block diagram of the valuator of a fractional power.

We can distinguish different types of physical phenomena with accuracy until 1% by using only one parameter, which is γ . Neural oscillations in certain ranges of parameters can be considered as chaotic processes with

scaling regularities. Such processes can be classified by the following values of $\gamma: \gamma_1 = 0.567, 1 - \gamma_1; \gamma_2 = 0.806, 1 - \gamma_2; \gamma_3 = 0.618, 1 - \gamma_3$ [9,10].

Numbers γ_1 , γ_2 are the normalized values of fixed information and entropy, respectively. These values can be used as criteria of self-organization. The well-known Fibonacci number (γ_3) is the 'golden mean' of a dynamic measure and it follows from the theory for γ_1 and γ_2 .

Table 1 shows that for the description of the various types of neural oscillations (signals from neural networks) it is sufficient to use nine iterations in Eq. (8).

γ m	γ_1	$1 - \gamma_1$	γ_2	$1 - \gamma_2$	γ_3	$1-\gamma_3$
9	0.567 ± 0.001	0.433 ± 0.001	0.806 ± 0.001	0.194 ± 0.001	0.618 ± 0.001	0.382 ± 0.001

Table 1. Values γ according to Eq. (8) for =9.

A block diagram of a digital implementation of the scale-invariant model of neural networks according to Eq. (5) is shown in Figure 7.



Figure 7. Block diagram of a digital implementation of the scale-invariant model of neural networks according to Eq. (5).

3. Results and discussion

Numerical and circuitry analysis of Eq. (3) are given below.

Figure 8 shows the possibility of a sufficiently accurate implementation of the dynamic system of Eq. (3) via the digital technology FPGA. The number of oscillations and amplitudes of peaks are the same in digital and circuit implementations. We have expressed voltage in millivolts and time in milliseconds. The curves in Figure 8 are fractal curves. Fractal dimensions of Hausdorff D_t , calculated by the standard algorithm [11]. are equal to $D_t = 1.22 \pm 0.01$ for cases of numerical and circuit implementation.

Another type of oscillation described by Eq. (5) is also adequately implemented by our proposed digital technology (Figure 9).



Figure 8. Numerical realization (a) and experimental results (b) for Eq. (3) at A = 0.8, B = 0.4, $\Omega = 88.8\pi$, V₀ = 0.1, k = 3, $\gamma = 0.433$.

Implementation of a hierarchical three-layer neural network described by Eq. (6) is shown in Figure 10. The network has three hierarchical layers with three neurons at each layer. Problems of this type of modeling of multilayer neural networks require a large memory capacity of the FPGA, so we used the integrated circuit family Spartan 6. It allows us to realize hierarchical levels of orders to n = 3 and degree of granularity in variations m = 1, 2.



Figure 9. Numerical realization (a, c, e) and experimental results (b, d, f) of the scale-invariant model of neural networks according to Eq. (5) at A = 0.8, B = 0.4, $\Omega = 8\pi$; $\gamma = 0.5$, V₀ = 0.1, k = 3.



Figure 10. Numerical realization (a) and experimental results (b) of the hierarchical model of neural networks (Eq. (6)) at A = 0.45, B = 0.5, $\Omega = 4\pi$, $\gamma = 0.5$, $V_0 = 0.1$, k = 3, n = 3.

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1 1.5 Time (t)

(a)

0 -0.01 -0.02

0.5

The experiment was done by calculating the duration of a quantitative comparison of the FPGA and

Ch1 10.0mV

Ch2

0f

(b)

M 200ms

software environment MATLAB R2012a in Intel Core i7-3770 CPU 3.40GHz RAM 8,00GB. The realization of Eq. (3) with N=1.5 \times 10⁶ points is chosen. With a computer we obtain results after 1.15 s and with FPGA Spartan 6 after 0.48 s. This is shown in Figure 11, where the FPGA gives results 2.4 times faster. For implementations with more than 10⁷ points, with a MATLAB score after 7.91 s and the FPGA after 1.0 s, it is about 8,0 times faster. Compilation results are given in Table 2.



Figure 11. Numerical realization (a) and experimental results (b) for Eq. (3) at $N = 1.5 \times 10^6$ points.

 Table 2. Device utilization summary.

Slice logic utilization	Used	Available	Utilization
Number of slice registers	151	54,576	1%
Number used as flip flops	53		
Number used as AND/OR logics	98		
Number of slice LUTs	10,405	27,288	38%
Number used as logic	10,341	27,288	37%
Number using O6 output only	7558		
Number using O5 output only	926		
Number using O5 and O6	1857		
Number used exclusively as route-through	64		
Number with same-slice carry load	64		
Number of occupied slices	3145	6822	46%
Number of MUXCYs used	9212	13,644	67%
Number of LUT flip flop pairs used	10,405		
Number with an unused flip flop	10,269	10,405	98%
Number with an unused LUT	0	10,405	0%
Number of fully used LUT-FF pairs	136	10,405	1%
Number of unique control sets	3		
Number of slice register sites lost to control set restrictions	3	54,576	1%
Number of bonded IOBs	9	320	2%
Number of LOCed IOBs	9	9	100%
Number of BUFG/BUFGMUXs	2	16	12%
Number used as BUFGs	2		
Number of DSP48A1s	35	58	60%
Average fanout of nonclock nets	2.77		

4. Conclusions

In this work we have shown the results of electronic digital implementation of different models of the dynamics of neurons. By using the proposed digital technology we can generate signals of the neural network with different structures, spiking (single regular and irregular spikes by time), bursting (regular and irregular alternations of single and multiple bursts), according to the terms accepted in the literature, for example in [12].

General models of neural networks have been considered by using the integrated FPGA circuitry in real time. The possibility of circuit simulation of neural networks described by fractional degrees of signals has been demonstrated. The structural element in the block for calculation of fractional power has also been developed. Using integrated circuit design is a simple way to implement complex tasks. Realization of neurodynamic models via the FPGA provides effectiveness in time, construction simplicity of devices, and a small size. Such implementation of neural network models can be used for creation of artificial neural networks different from existing analog systems. These models are maximally close to a system of biological neurons, which is a perspective problem in this direction.

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