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A 2-D analytical model for cylindrical gate tunnel FET (CG-TFET) based on center potential

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Abstract: In this paper, a 2-D cylindrical gate tunnel FET (CG-TFET) model is developed based on the potential at the center of cylinder. The center potential is obtained by Laplace solution in the cylindrical coordinate system and the accuracy is validated using a 2-D TCAD device simulator. The tunneling of charge carriers in the CG-TFET is analyzed using the center potential and the results are compared to the surface potential-based model. The drain current is formulated using the initial tunneling point and tunneling path, which further helps to obtain the threshold voltage of this model. The effect of gate engineering and band-gap engineering on the drain current are investigated. The device scaling capability of the model is discussed extensively.

Key words: CG-TFET, center potential, tunneling path, drain current, threshold voltage

1. Introduction

As the bulk metal oxide semiconductor FET (MOSFET) dimensions are downscaled continuously to improve the packing density, the devices suffer from short channel effects (SCEs) such as threshold voltage roll-off and drain-induced barrier lowering (DIBL). The SCEs arise due to the reduction of gate control on the channel and the physical limits of the structure [1,2]. Many researchers adapted a number of multiple-gate devices such as the cylindrical gate MOS (CG-MOS), which provides excellent electrostatic control of the channel due to its physical structure [3–5]. The cylindrical GAA (gate all around) MOS provides better ON-state current and threshold stability compared to single-gate, dual-gate, and tri-gate structures [6,7]. However, there is an exponential increase of leakage current (I_{OFF}) and thermally limited 60 mV/decade subthreshold swing (SS) in CG-MOS. This leads to higher power consumption and low-speed switching behavior [7].

The tunnel field effect transistor (TFET) has emerged as a potential alternative to bulk MOS in low power applications due to its steep switching behavior (sub-60 mV/decade SS) and low I_{OFF} [8–10]. As the drain current of the TFET is obtained by a nonlocal direct band-to-band tunneling (BTBT) model at the source–channel interface, SS is not limited to 60 mV/decade, unlike MOSFETs [11]. The TFET also produces minimal leakage current I_{OFF} as compared to MOS because of the reduced electric field along the channel in the OFF-state. In recent times quite a few compact analytical models for the TFET have been reported to improve the ON-current performance and device scaling [12–23]. A number of single-gate [13–16], double-gate

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[17–20], and cylindrical-gate [21–23] TFET models have been developed using BTBT phenomena. Compared to other models, the cylindrical-gate TFET (CG-TFET) exhibits the maximum scaling capability due to its physical structure and provides SS below 60 mV/decade. All of the above discussed TFET models employ a 2-D analytical solution of the Poisson equation based on surface potential. However, Dubey et al. [24] developed an analytical model for CG-MOS based on potential at the center of the cylindrical body. They reported that the characteristic length of the center potential model is smaller compared to the conventional surface potential-based model. Hence, this improves the device scaling capability and reduces the threshold voltage of the CG-MOS.

In this paper, we develop a CG-TFET analytical model based on center potential. The center potential has been derived using parabolic approximation in the Laplace equation and validated using a TCAD device simulator from Synopsis. The resultant center potential is further used to study the tunneling behavior of charge carriers. The drain current is calculated through the tunneling path in the lateral direction. Furthermore, the threshold voltage is extracted using the peak transconductance change (TC) method. The effect of scaling of the device dimensions such as cylindrical pillar diameter and gate oxide thickness on drain current performance has been investigated for a channel length of 50 nm. Various SCEs like DIBL and punch-through have been studied for the present model. The drain current analysis is further extended for different work functions and various band-gap materials. The results have been compared with the conventional surface potential CG-TFET model.

2. Analytical modeling

The schematic of the CG-TFET is shown in Figures 1a and 1b. The source and drain regions of the model are uniformly doped with doping concentration of $N_d = 10^{20}$ and $N_a = 10^{20}$, respectively. The channel region of the device is intrinsic and is doped on the order of 10^{15}. The radial and lateral directions of the channel are along the radius and z-axis of the confined cylinder. The thickness of the SiO_2 layer and the diameter of the silicon cylindrical pillar is considered as $t_{ox} = 2$ nm and $t_{si} = 10$ nm, respectively. The work function of the gate material used is $\emptyset_M = 4.6$ eV.

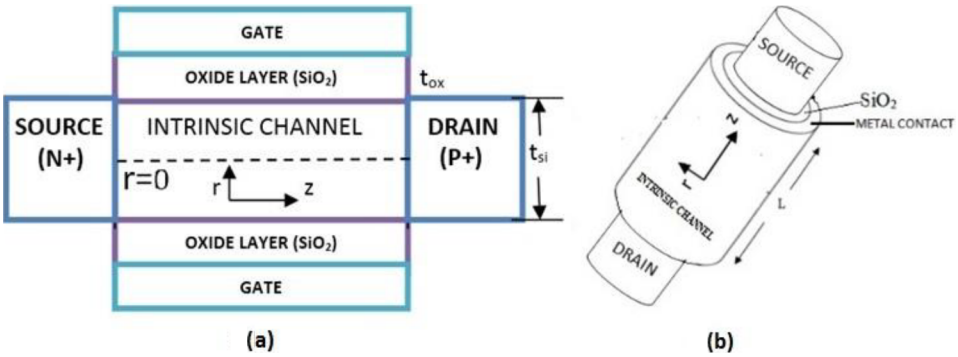

Figure 1. (a) Cross-sectional view, (b) side-view of CG-TFET.

2.1. Center potential formulation

The effect of doping concentration of the channel on electrical parameters of the device is neglected as the channel is considered to be intrinsic. Therefore, the potential distribution $\varphi(rz)$ can be estimated using the

2-D Laplace equation in the cylindrical coordinate system as:

$$\frac{1}{r}\frac{\partial}{\partial r}\left(r\frac{\partial}{\partial r}\varphi(r,z)\right)+\frac{\partial^2\varphi(r,z)}{\partial z^2}=0. \tag{1}$$

Here the effect of the third cylindrical coordinate (?) on the solution is neglected due to the minimal variation of potential in the angular direction. The above equation is used to evaluate the surface potential (φ_s) at the gate–channel interface and center potential (φ_c) at the center of the cylinder along the z-axis.

$$\varphi\left(r,z\right)]_{r=0}=\varphi_c(z) \tag{2}$$

$$\varphi\left(r,z\right)]_{r=\pm\frac{t_{si}}{2}}=\varphi_s(z) \tag{3}$$

The solution of Eq. (1) can be obtained by 2nd order polynomial approximation [5]. The polynomial function takes the help of boundary conditions of potential and electric field at the center of the cylinder and gate–channel interface of the CG-MOS [25]. The potential profile at the center is found to be:

$$\frac{\partial^2\varphi_c(z)}{\partial z^2}+\frac{(V_{GS}-V_{FB}-\varphi_s(z))}{\lambda}=0, \tag{4}$$

where V_{GS} is the gate-to-source voltage, V_{FB} is the flat-band voltage, and λ is the characteristic length of the cylindrical structure mathematically defined as:

$$\lambda=\sqrt{\frac{t_{si}^2\epsilon_{si}\ln\left(1+\frac{2t_{ox}}{t_{si}}\right)}{8\epsilon_{ox}}}. \tag{5}$$

Here ϵ_{si} is the dielectric permittivity of silicon and ϵ_{ox} is the permittivity of the oxide layer. The surface potential along the z-axis $\varphi_s\left(z\right)$ is related to the center potential $\varphi_c(z)$ as follows [24]:

$$\varphi_c\left(z\right)=\left(H^2+1\right)\varphi_s\left(z\right)-H^2(V_{GS}-V_{FB}), \tag{6}$$

where

$$H=\frac{t_{si}}{4\lambda} \quad . \tag{7}$$

Eq. (4) can be expressed in terms of surface potential using Eq. (6):

$$\frac{\partial^2\varphi_s(z)}{\partial z^2}+\frac{(V_{GS}-V_{FB}-\varphi_s(z))}{\lambda^2}=0 \quad . \tag{8}$$

Upon solving Eq. (8), the surface potential of the model along the channel is found to be:

$$\varphi_s\left(z\right)=c_1e^{\left(z/\lambda\right)}+c_2e^{-\left(z/\lambda\right)}+(V_{GS}-V_{FB}) \quad . \tag{9}$$

The coefficients c_1 and c_2 can be calculated using the boundary conditions at the source and drain interface [16].

$$\varphi_s\left(z\right)]_{z=0}=V_{bi} \tag{10}$$

$$\varphi_s(z)]_{z=L} = V_{DS} \tag{11}$$

Here V_{bi} is the built-in potential, V_{DS} is the drain-to-source voltage, and L is the maximum channel length of the device.

Equating Eq. (9) using the boundary conditions at source and drain interface:

$$c_1 = \left[\frac{(V_{DS} - V_{GS} + V_{FB}) - e^{-(L/\lambda)}(V_{bi} - V_{GS} + V_{FB})}{2sinh(L/\lambda)}\right] \quad , \tag{12}$$

and

$$c_2 = -\left[\frac{(V_{DS} - V_{GS} + V_{FB}) - e^{(L/\lambda)}(V_{bi} - V_{GS} + V_{FB})}{2sinh(L/\lambda)}\right] \quad . \tag{13}$$

Substituting Eq. (9) in Eq. (6), the center potential is obtained as:

$$\varphi_c(z) = \left(H^2 + 1\right)\left(c_1 e^{\left(z/\lambda\right)} + c_2 e^{-\left(z/\lambda\right)} + V_{GS} - V_{FB}\right) - H^2(V_{GS} - V_{FB}) \quad . \tag{14}$$

The center potential reduces faster as compared to the surface potential and it attains a larger value at the source–channel interface. This improves the magnitude of tunneling volume by lowering the threshold voltage of the device, so the center potential has been used in the present model to calculate the tunneling path and drain current. However, the flow of charge carriers in the TFET is primarily due to the nonlocal BTBT mechanism [26,27]. The tunneling of the carrier takes place in the z-direction. Therefore, the lateral electric field plays an important role in the tunneling current analysis. The lateral electric field is obtained by differentiating the potential profile in the range of $(0 \leq z \leq L)$.

$$E_{zs}(r,z) = -\frac{\partial \varphi_s(r,z)}{\partial z} = -\frac{c_1}{\lambda}e^{(z/\lambda)} + \frac{c_2}{\lambda}e^{-(z/\lambda)} \tag{15}$$

$$E_{zc}(r,z) = -\frac{\partial \varphi_c(r,z)}{\partial z} = \left(H^2 + 1\right)\left(-\frac{c_1}{\lambda}e^{(z/\lambda)} + \frac{c_2}{\lambda}e^{-(z/\lambda)}\right) \tag{16}$$

2.2. Tunneling path derivation

The charge carriers tunnel through a barrier using BTBT phenomena instead of modulating thermionic emission, as in MOSFETs. The BTBT generation rate is exponentially dependent on the electric field at the tunneling junction. The tunneling of charge carriers for the CG-TFET model can be analyzed using the energy band diagram. The band diagram of the p-channel CG-TFET for both OFF-state and ON-state is depicted in Figures 2a and 2b. When $V_{GS} < V_{th}$, the drain current is minimal due to the absence of a tunneling path as shown in Figure 2a. This minimal current is known as OFF-state current (I_{OFF}) and adversely affects the device performance for sub-32 nm channels. At a decisive value of V_{GS} known as threshold voltage, the conduction band and valence band are aligned with each other due to the potential drop by an amount of unit band gap energy per charge $\left(\frac{E_g}{q}\right)$ [22]. This condition is termed as ON-state and is the boundary to measure tunneling volume. For $V_{GS} > V_{th}$, the probability of tunneling of carriers through the channel increases, hence improving the BTBT volume as shown in Figure 2b. The tunneling path is the difference between z_1 and z_2 along the channel.

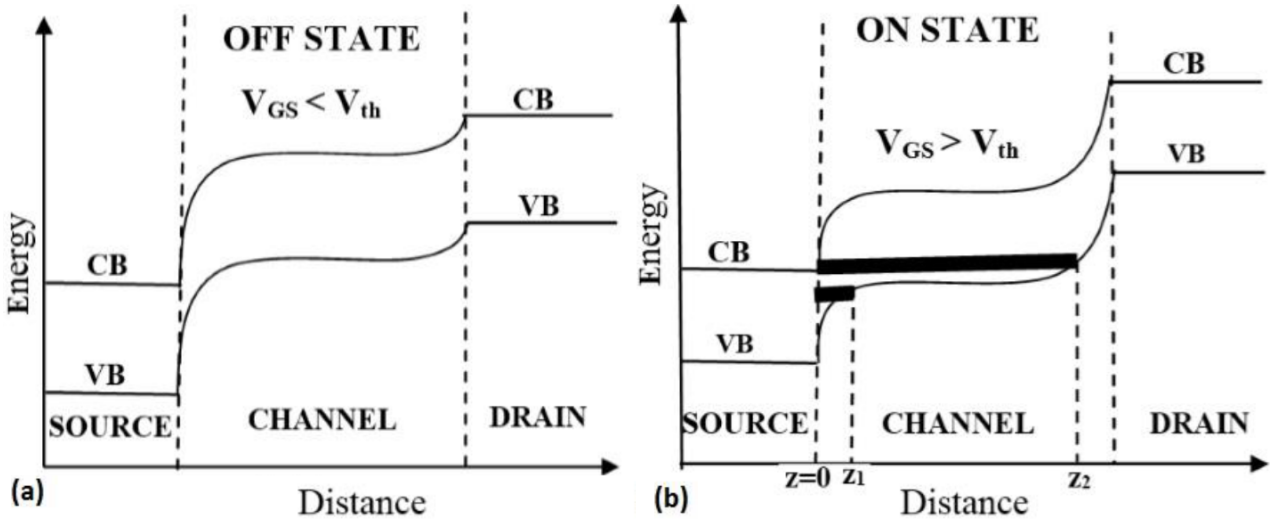

Figure 2. Energy band diagram of p-channel CG-TFET in (a) OFF-state and (b) ON-state.

Here the initial tunneling point (z_1) is the distance between the source–channel interface ($z = 0$) and the point in the channel where the center potential changes by an amount of E_g/q. z_1 also defines the critical threshold condition for gate voltage. The center potential for the conduction band of the source and valence band of the channel are respectively:

$$\varphi_{CB}(z) = \varphi_c(0) = \left(H^2+1\right)V_{bi} - H^2(V_{GS} - V_{FB}) \quad , \tag{17}$$

$$\varphi_{VB}(z) = \varphi_c(z_1) + \frac{E_g}{q} = \left(H^2+1\right)\left(c_1 e^{\left(z_1/\lambda\right)} + c_2 e^{-\left(z_1/\lambda\right)}\right) + V_{GS} - V_{FB} + \frac{E_g}{q} \quad . \tag{18}$$

The initial tunneling point z_1 can be obtained using Eqs. (17) and (18) as:

$$z_1 = \lambda ln\left(\frac{k - \sqrt{k^2 - 4c_1c_2}}{2c_1}\right) \quad , \tag{19}$$

where

$$k = V_{bi} - V_{GS} + V_{FB} - \frac{E_g}{q\left(H^2+1\right)} \quad . \tag{20}$$

Similarly, the final tunneling point z_2 is the z-distance between the source–channel interface and the point in the channel where the center potential is the minimum. The final tunneling point can be obtained by calculating the minimum center potential along the z-axis. Differentiating Eq. (14) w.r.t. the z-axis, we get the value of z_2 as:

$$\left.\frac{\partial\varphi_c(z)}{\partial z}\right]_{z=z_2} = \left(H^2+1\right)\left(c_1 e^{\left(z_2/\lambda\right)} + c_2 e^{-\left(z_2/\lambda\right)}\right) = 0 \quad , \tag{21}$$

$$z_2 = \lambda ln\sqrt{\frac{c_2}{c_1}} \quad . \tag{22}$$

However, the value of z_2 in the center potential model is like that of the surface potential-based DC model because both surface and center potential achieve the same minimum potential at point z_2. However, the

initial tunneling point z_1 arises earlier in the center potential model as compared to surface potential. That also reduces the threshold voltage for a constant drain voltage. The initial tunneling point and tunneling path can be optimized by using band-gap engineering and gate engineering. For a constant gate voltage the tunneling volume is not affected by drain voltage.

2.3. Drain current analysis and threshold voltage formulation

The drain current of the CG-TFET with direct nonlocal tunneling process can be calculated using the Kane model [28]. The drain current in the z-direction along the channel is expressed as:

$$I_D = q \int_{-\frac{t_{si}}{2}}^{\frac{t_{si}}{2}} \left(\int_{z_1}^{z_2} A_{kane} E_{zc} \left(\frac{E_g}{qz} \right) e^{-\left(\frac{qzB_{kane}}{E_g} \right)} dz \right) dr, \tag{23}$$

where A_{kane} and B_{kane} are Kane model parameters and the values of $A_{kane} = 4 \times 10^{15}$ $\mathrm{m}^{-1/2}\mathrm{V}^{-5/2}\mathrm{s}^{-1}$ and $B_{kane} = 1.9 \times 10^9$ V/m, respectively [29]. On simplifying Eq. (23), we get:

$$I_D = t_{si} E_g A_{kane} \left[\int_{z_1}^{z_2} \left(\frac{E_{zc}}{z} \right) e^{-\left(\frac{qzB_{kane}}{E_g} \right)} dz \right]. \tag{24}$$

Substituting the value of the electric field in the z-direction in the above equation:

$$I_D = t_{si} E_g A_{kane} \left(H^2 + 1 \right) \left[\int_{z_1}^{z_2} \frac{-c_1 e^{\left(\frac{1}{\lambda} - \frac{qB_{kane}}{E_g} \right) z}}{z\lambda} dz + \int_{z_1}^{z_2} \frac{c_2 e^{-\left(\frac{1}{\lambda} + \frac{qB_{kane}}{E_g} \right) z}}{z\lambda} dz \right] \quad , \tag{25}$$

$$I_D = I_0 \left[\int_{z_1}^{z_2} \frac{-c_1 e^{\left(\frac{1}{\lambda} - \frac{qB_{kane}}{E_g} \right) z}}{z} dz + \int_{z_1}^{z_2} \frac{c_2 e^{-\left(\frac{1}{\lambda} + \frac{qB_{kane}}{E_g} \right) z}}{z} dz \right] \quad , \tag{26}$$

where

$$I_0 = \frac{t_{si} E_g A_{kane} \left(H^2 + 1 \right)}{\lambda}. \tag{27}$$

Between the two boundaries along the z-direction, the effect of the exponential term is superseding the polynomial term in Eq. (26), so the drain current is obtained by neglecting the polynomial term as:

$$I_D = I_0 \left[\left(\frac{-c_1}{\frac{1}{\lambda} - \frac{qB_{kane}}{E_g}} \right) \left(P_{z_2} - P_{z_1} \right) - \left(\frac{c_2}{\frac{1}{\lambda} + \frac{qB_{kane}}{E_g}} \right) \left(Q_{z_2} - Q_{z_1} \right) \right], \tag{28}$$

where P_z and Q_z are expressed as:

$$P_z = \frac{e^{\left(\frac{1}{\lambda} - \frac{qB_{kane}}{E_g} \right) z}}{z} \text{ and } Q_z = \frac{e^{-\left(\frac{1}{\lambda} + \frac{qB_{kane}}{E_g} \right) z}}{z}. \tag{29}$$

The threshold voltage of the CG-TFET can be evaluated precisely by the TC method [30]. In the present paper, the TC method has been used to extract the threshold voltage of the p-channel CG-TFET based on center

potential. Here V_{th} is calculated by finding the value of gate voltage at which the change in transconductance (2nd order differentiation of current) is the highest.

$$V_{th} = V_{GS}, \text{ when } \left.\frac{d^2 I_D}{dV_{GS}^2}\right]_{V_{DS}=con} = max \tag{30}$$

3. Results and discussion

Device simulation has been performed using the TCAD device simulator from Synopsis [31] and the results are compared with the analytical results to check their accuracy. In this model, a nonlocal path BTBT model is used as the primary carrier transport mechanism. The surface and center potential distribution along the channel in the model is illustrated in Figure 3. The surface potential nearer to the source and drain end is slightly smaller as compared to center potential as defined by Eq. (6). The difference between the potentials is dependent on the characteristic length of the cylinder and work function of gate material, but both the potential curves attain the same minimum magnitude, which is constant for the midregion of the 50 nm channel. This is because the controlling ability of the cylindrical gate on the channel is saturated. However, it is observed that the reduction of the center potential is sharp as compared to surface potential at the interface, validated by device simulator results. This enhances the chances of initiating the tunneling process in the device. Therefore, the tunneling path increases and hence reduces the threshold voltage. Thus, the center potential can be used for calculation of the tunneling path, drain current, and threshold voltage.

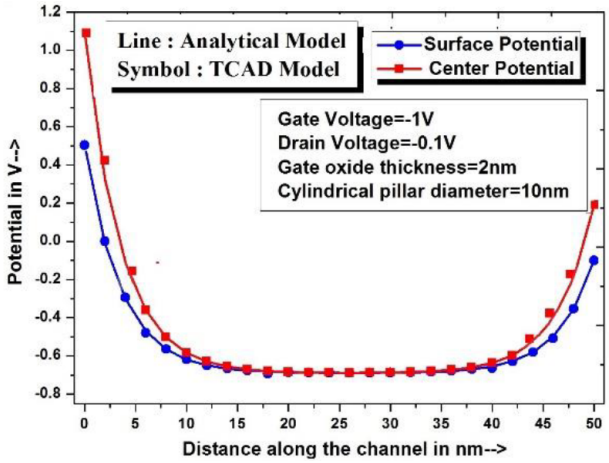

Figure 3. Electrostatic potential profile of CG-TFET for V_{DS} = –0.1 V, V_{GS} = –1 V. The profile includes the variation of surface potential and channel potential w.r.t. distance along the z-axis.

Figures 4a and 4b display the effect of variation of gate voltage and drain voltage on the center potential of the model, respectively. With increase in gate voltage for a constant drain bias, the center potential of the device reduces further, as depicted in Figure 4a. This is due to the enhancement of gate control on the channel. However, the potential distribution remains constant for the middle portion of the channel. This constant potential gives rise to a minimum electric field due to its zero slope. Similarly, Figure 4b illustrates the variation of the center potential for different values of V_{DS}. It is observed that there is no noteworthy change in the center potential at the source interface and middle of the channel. This is because of the prominent influence of the gate over the channel compared to drain. The minimum center potential and its slope remain unchanged irrespective of the variation of drain bias, but there is a small change in potential at the drain interface that

gives rise to DIBL. In this model the DIBL effect on drain current is minimal, but it affects the performance of the device significantly for sub-32 nm channels.

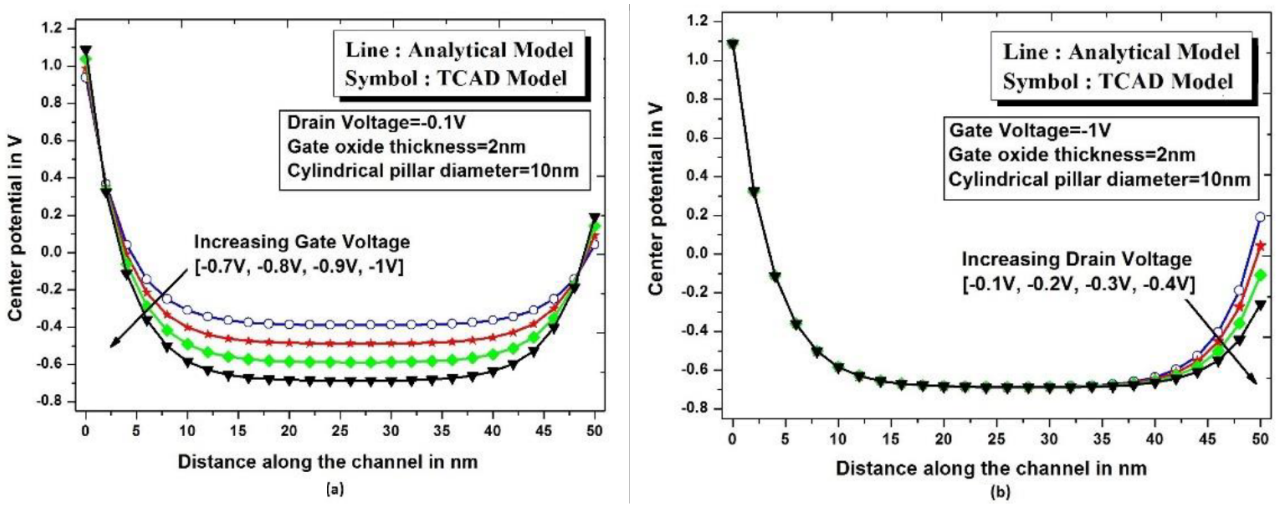

Figure 4. Center potential distribution of p-channel CG-TFET for 50 nm channel length: (a) due to variation of gate voltages, (b) due to variation of drain voltages.

Figure 5a shows the variation of the center potential of the model for different values of gate oxide thickness. With reduction of t_{ox}, the control of the gate on the surface potential increases due to close proximity, but this effect is minimal in the case of center potential. The t_{ox} beyond its physical constraint becomes more prominent with SCEs such as punch-through and hot-carrier effects. Similarly, Figure 5b displays the effect of scaling of the cylindrical pillar diameter on the center potential of the channel. The figure shows the potential distribution for four different values of t_{si}. When the pillar thickness reduces from 18 nm to 6 nm, the center potential reduces faster with high slope and attains a minimum value. This is due to the strong controlling capability of the gate on the center potential as compared to the influence exerted by the source/drain. The sharp slope leads to the small threshold voltage in the nonlocal BTBT phenomena.

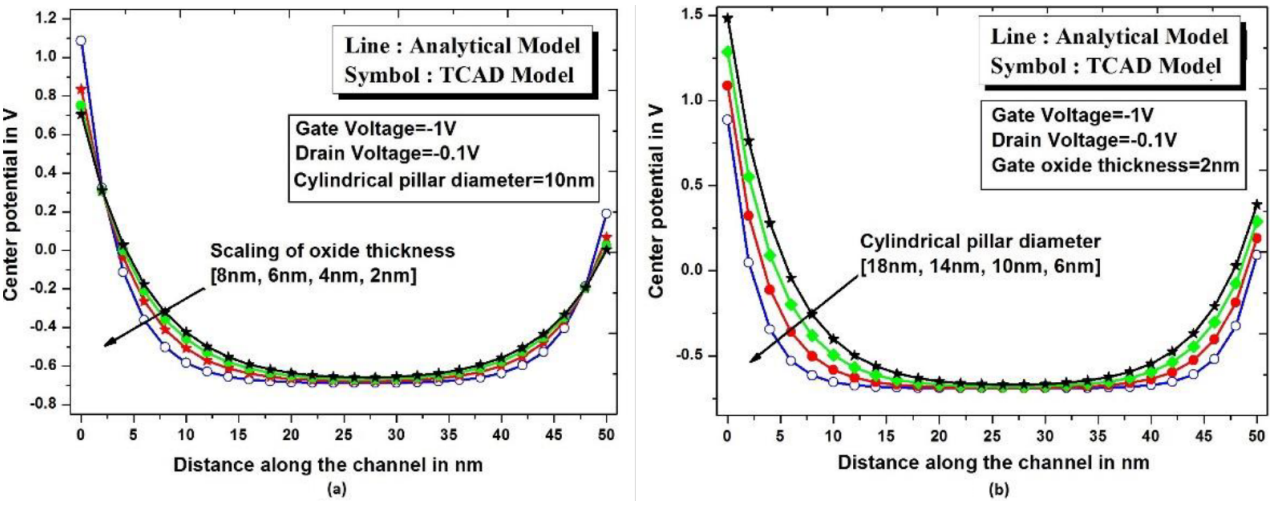

Figure 5. Effect of (a) gate oxide scaling and (b) cylindrical diameter scaling on center potential of the model at constant gate and drain bias.

The initial tunneling point (z_1) as a function of gate voltage is shown in Figure 6. When V_{GS} increases beyond the threshold, the initial tunneling point (z_1) reduces. This indicates larger tunneling volume and thus improves the probability of tunneling rate. This figure also depicts the better performance of the center potential-based model as compared to the surface potential. In the proposed model, z_1 arises earlier for a small gate bias as compared to surface potential, resulting in the reduction of threshold voltage in the case of a center potential-based model. However, for long channel devices, the increase of drain voltage does not affect the initial tunneling point. The drain voltage plays a key role in the tunneling process for channel length below 32 nm due to close proximity between source and drain.

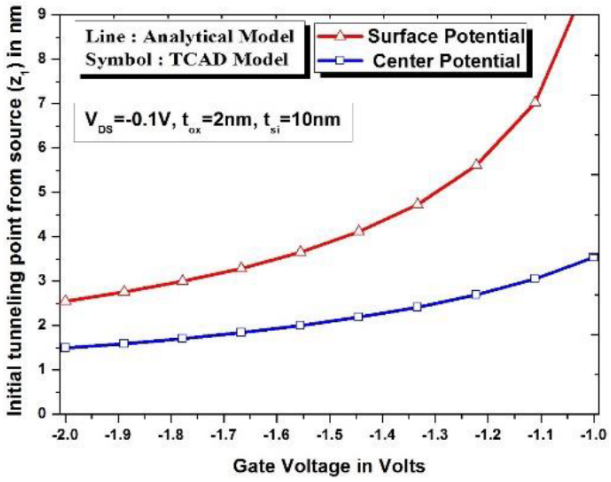

Figure 6. Variation of initial tunneling point (z_1) w.r.t. gate voltages based on surface and center potential distribution.

Figure 7 illustrates the effect of variation of gate voltage on tunneling path. The path gradually increases for $V_{GS} > V_{th}$ and finally gets saturated for higher gate voltage. The same figure shows the tunneling path of the proposed center potential-based model compared to the conventional surface potential. The center potential-based model shows better performance in terms of tunneling volume and threshold voltage. It enhances the volume by improving the tunneling path in the z-direction and thus lowers the threshold voltage for tunneling. Finally, the path ($z_2 - z_1$) is saturated at a higher gate bias due to the saturation of tunneling charge carriers in the channel.

Figure 8a illustrates the drain current characteristics of this model on a logarithmic scale. The results of the center potential-based model are also compared with those of the conventional model. It is evident that the present model provides poor drain current performance, because of the reduction in lateral electric field at the tunneling junction. In the surface potential-based model, though the tunneling volume is less the electric field created at the junction is maximum, which leads to high drain current. On the contrary, the reduction in initial tunneling point leads to the reduction of threshold voltage in the present model, as shown in Figure 8b. This improvement of threshold is due to the sharp reduction of center potential along the channel. Here the threshold voltage is obtained by finding the value of gate voltage for which the $\frac{d^2 I_D}{dV_{GS}^2}$ curve attains the peak value. However, the threshold voltage remains independent of the variation of channel length, as shown in Figure 8b.

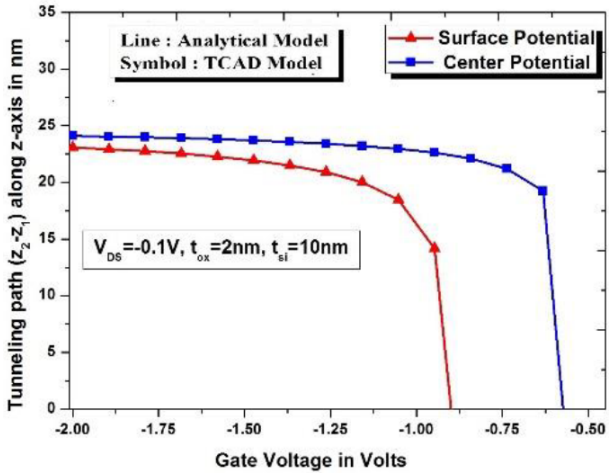

Figure 7. Variation of tunneling path ($z_2 - z_1$) w.r.t. gate voltage based on surface and center potential distribution.

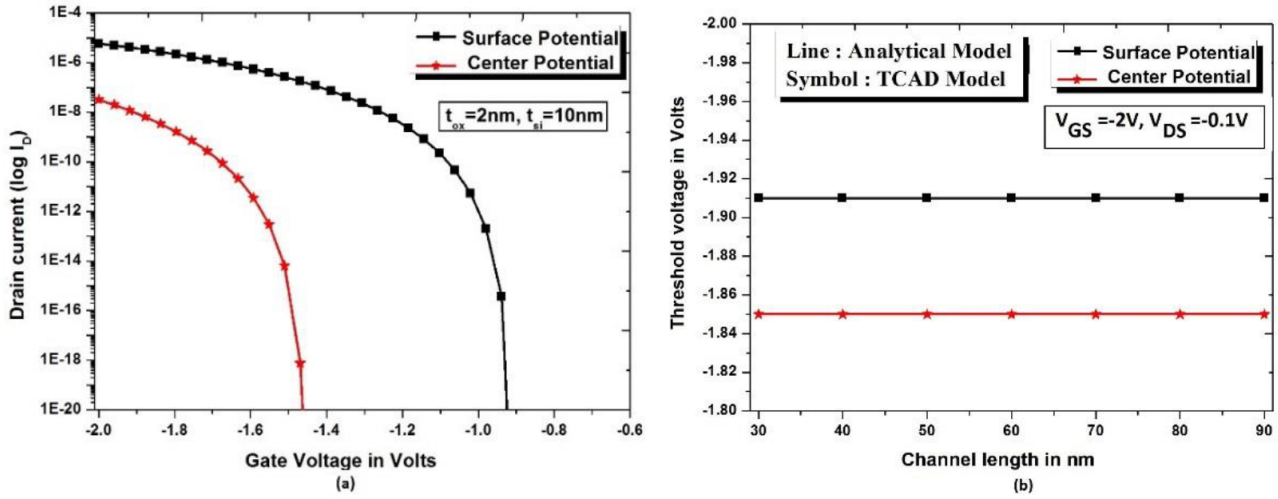

Figure 8. (a) $I_D - V_{GS}$ characteristics and (b) variation of threshold voltage w.r.t. channel length for the center potential-based CG-TFET model. The results are compared with that of the conventional surface potential-based model.

The impact of t_{si} scaling on drain current for the proposed model is investigated in Figure 9. With the reduction in t_{si}, higher drain current and steeper subthreshold slope are achieved. Reduction in cylindrical pillar diameter reduces the gate oxide capacitance per unit area of the cylindrical structure, which increases drain current. The influence of the gate on the channel is dominant at $t_{si} = 6$ nm as compared to 10 nm. At lower t_{si}, the center potential reduces faster and hence it lowers the initial tunneling point z_1. Here the drain current is improved by a factor of 10 because of the scaling of the diameter by 2 nm.

Figure 10 illustrates the impact of variation of band-gap energy on drain current. Here we have considered three different materials, Ge, Si, and GaAs, having band-gap energy (E_g) of 0.66 eV, 1.11 eV, and 1.43 eV, respectively. It is observed that the model exhibits better performance in terms of ON-current for lower band-gap material (Ge). The improvement in drain current is because of the large tunneling volume in the BTBT process. This large volume is obtained as a result of reduction in initial tunneling point for small band-gap energy.

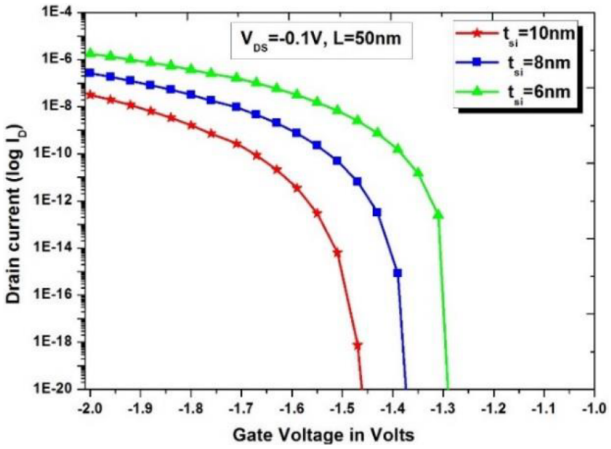

Figure 9. $I_D - V_{GS}$ characteristics for the center potential-based CG-TFET model as a function of cylindrical pillar diameter.

The drain current behavior for the present model using three different gate materials having work functions of 4.6 eV, 4.8 eV, and 5 eV is shown in Figure 11. The higher work function material produces better performance in terms of tunneling current. This is because of the sharp reduction of center potential. However, this also improves the SS compared to low work function materials.

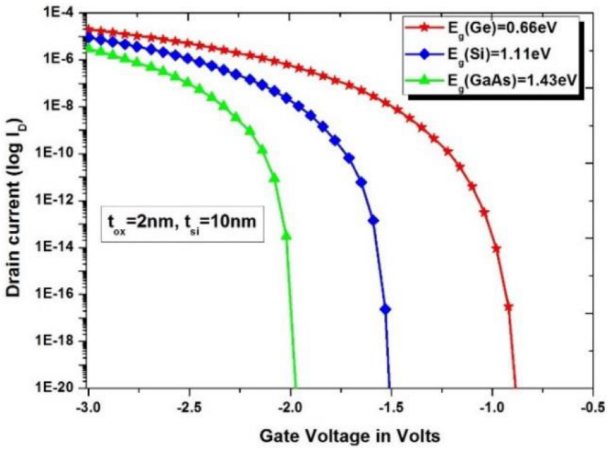

Figure 10. Effect of variation of band-gap energy on $I_D - V_{GS}$ characteristics.

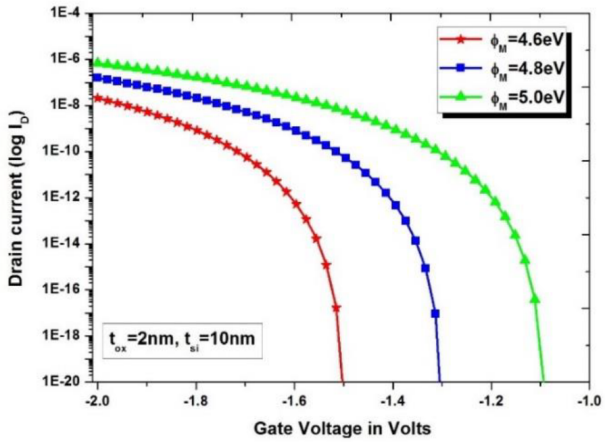

Figure 11. Impact of various metal work functions on $I_D - V_{GS}$ characteristics.

The center potential-based CG-TFET lowers the threshold voltage and SS as compared to the conventional TFET. It also provides better scalability of gate oxide thickness and cylindrical body diameter for 50 nm channels. Therefore, this model can be a solution for high-speed switching applications in the VLSI industry.

4. Conclusion

In this paper a center potential-based CG-TFET model is developed using the solution of the 2-D Laplace equation. The tunneling parameters, drain current, and threshold voltage have been obtained using center potential and the results are compared to that of the conventional model. It is evident from the results that drain current performance degrades in the proposed model because of low electric field at the source–channel interface. On the contrary, it provides higher tunneling rate of charge carriers, improvement in threshold

voltage, and reduced DIBL. The drain current can be enhanced by downscaling cylindrical body diameter, reducing band-gap energy, and increasing the work function of the gate metal. This enhances the chances of using the center potential-based model for high-speed VLSI and embedded system applications.

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