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Single event multiple upset-tolerant SRAM cell designs for nano-scale CMOS technology

Ramin RAJAEI[1,*], Bahar ASGARI[2], Mahmoud TABANDEH[3], Mahdi FAZELI[2]
[1]Department of Electrical Engineering, Shahid Beheshti University, Tehran, Iran
[2]Department of Computer Engineering, Iran University of Science and Technology, Tehran, Iran
[3]Department of Electrical Engineering, Sharif University of Technology, Tehran, Iran

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Abstract: In this article, two soft error tolerant SRAM cells, the so-called RATF1 and RATF2, are proposed and evaluated. The proposed radiation hardened SRAM cells are capable of fully tolerating single event upsets (SEUs). Moreover, they show a high degree of robustness against single event multiple upsets (SEMUs). Over the previous SRAM cells, RATF1 and RATF2 offer lower area and power overhead. The Hspice simulation results through comparison with some prominent and state-of-the-art soft error tolerant SRAM cells show that our proposed robust SRAM cells have smaller area overhead (RAFT1 offers 58% smaller area than DICE), lower power delay product (RATF1 offers 231.33% and RATF2 offers 74.75% lower PDP compared with DICE), much more soft error robustness, and larger noise margins.

Key words: Single event upset (SEU), single event multiple upset (SEMU), soft error, SRAM cell

1. Introduction

As CMOS technology shrinks toward nano-scale, CMOS circuits become more sensitive to radiation induced soft errors [1–4]. When an energetic particle such as a neutron or proton strikes a sensitive node of a memory cell it can change the stored value to an erroneous value. These errors are called soft errors, since the memory cell is not permanently damaged and the faulty value of the memory cell due to particle strike would be corrected in the next write operation. When an energetic particle passes through semiconductor material, along the pass way, it loses its energy and generates electron-hole pairs. The deposited charge generates a current glitch, which in turn produces a transient voltage in the struck node. The transient voltage propagates through the circuit and may change the stored value of the memory cell. Consequently, the stored value of the SRAM cell will turn to a faulty logic value. This phenomenon is called single event upset (SEU) [3–7].

Figure 1a shows the conventional 6T SRAM cell. The failure mechanism of a particle strike inside an SRAM cell is shown in Figure 1b. To this end, we have carried out a fault injection experiment into a sensitive node of an SRAM cell using HSpice simulation using a double exponential current source specified in Eq. (1) [3,4]. The feedback path of an SRAM cell makes it sensitive to SEUs. As shown in Figure 1b, an SEU is injected to node X1. Initially, transistors N1 and P2 were ON and transistors N2 and P1 were OFF. As a result of the SEU injection, some amounts of charge are injected in the struck region and cause the emergence of a voltage pulse at the struck node (i.e. X1). The voltage pulse, i.e. changing the logic value of X1 to ‘0’, makes the transistor N1(P1) OFF(ON) and the logic value of X2 changing from 0 to ‘1’. As nodes X1 and

*Correspondence: r_rajaei@sbu.ac.ir

X2 are connected via two back-to-back inverters, this transient alteration of logic value in nodes X1 and X2 remains unchanged until the next write operation. In Figure 1b, after the second write operation, another SEU is injected to X1. In this case, the value of X1 changes from ‘0’ to ‘1’ and a similar scenario repeats. As SEU is a concerning issue in safety-critical applications, designing of SEU tolerant SRAM cells has been widely taken into consideration [3,4,7]. There are many noticeable factors such as node capacitance and supply voltage of transistors that affect the failure mechanism of SEUs in VLSI circuits. For instance, by reducing the size of transistors and supply voltage, the sensitivity of SRAM cells to the energetic particle collisions increases [3,4].

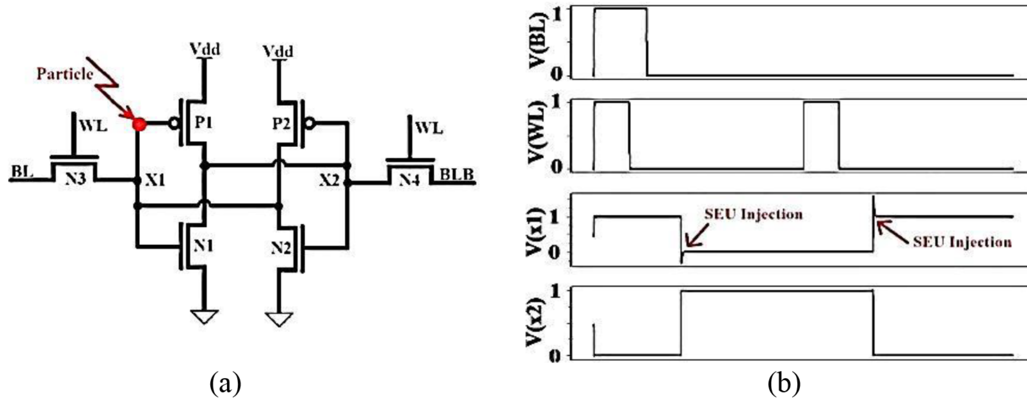

Figure 1. The conventional 6T SRAM cell a) SEU injection to node X1, b) SEU injection to node X1 when its logic value is ‘1’ when its logic value is ‘0’.

Table 1. Comparison of power, area, performance and PDP of our SRAM cells with other leading soft error tolerant SRAM cells. All results are normalized to the 6T SRAM cell.

SRAM type	Power dissipation	Number of transistors	Area	Write delay	Read delay	PDP
RATF1	1.03	8	1.19	1.88	1.10	1.53
RATF2	1.13	10	1.82	2.76	2.39	2.91
11T [8]	2.14	11	2.26	1.04	1.11	2.30
13T [4]	1.52	13	2.69	1.04	1.05	1.59
10T [9]	1.21	10	1.84	1.04	1.59	1.59
DICE [7]	3.27	12	1.88	1.61	1.50	5.08
JAHIN [10]	2.74	10	2.48	2.09	2.42	6.18

A large amount of research has been carried out regarding SEU tolerance of SRAM cells. Most of them assume that an energetic particle could affect only a single node of an SRAM cell. This assumption was acceptable in older technologies in which transistor sizes were larger and nodes were farther away. In recent nanometer scale technologies, where transistors are closer to each other, an energetic particle strike could affect multiple adjacent nodes, the so-called single event multiple upset (SEMU). Consequently, along with the decreasing size of transistors in CMOS technology, SEMU counts as another important challenge related to SRAM cells [3,5].

2. Previous work

To date, many SEU tolerant SRAM cells have been presented in the literature. In this section, we cover some state-of-the-art and prominent robust SRAM cell designs. In [4,8], two SEU-tolerant SRAM cells containing

13 and 11 transistors have been proposed. The main idea behind them is using two transistors in the feedback path of the SRAM cell for periodically connecting/disconnecting of the feedback path. As shown in Figure 2a, M5 and M8 are the additional transistors playing the role of the switch in the feedback path. Two control signals namely RF and RFB turn M5 and M8 ON and OFF frequently, thus preventing the propagation of a transient pulse from the originated side to the opposite side. Consequently, the effect of particle strike will not remain permanently. The circuit proposed in [4] employs two more transistors (M12 and M13) than the circuit proposed in [8]. Using a Schmitt trigger in the feedback loop of the proposed SRAM cell in [4] makes it more robust against SEMU in comparison with the design of [1]. The main shortcoming of the proposed design in [2] is its rather high area overhead as well as power penalty. As will be evaluated in section IV, the proposed design in [1,2] shows weak robustness in the presence of SEMUs.

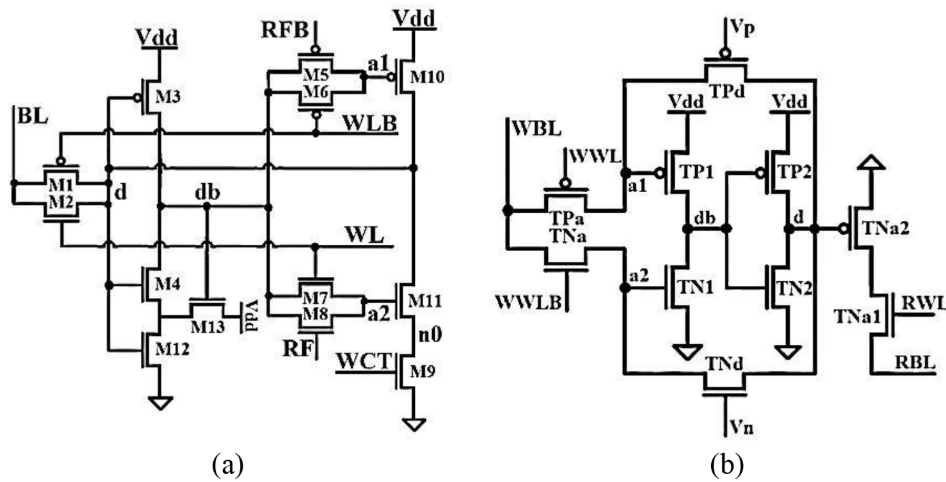

Figure 2. Previous refresh line based rad-hard SRAM cells: a) proposed cell in [4] b) proposed cell in [9].

Table 2. Critical charge of various sensitive nodes when RL = ‘1’.

SRAM type	Node	Qc (normalized)
RATF1	X1	1.54
	X2	1.68
RATF2	X1	1.76
	X2	1.73
11T [8]	d	1.41
	db	1.73
13T [4]	d	1.41
	db	2.38
10T [9]	d	1.51
	db	1.46
JAHIN [10]	a (when holds 0)	1.70
	b (when holds 1)	1.70
	c (when holds 0)	1.65
	d (when holds 1)	1.65
Simple SRAM	X1	1.00
	X2	1.00

A soft error tolerant SRAM cell including 10 transistors is proposed in [9]. As can be seen in Figure 2b, this circuit exploits the same idea as [4,8] to prevent propagation of the transient effect caused by a particle strike. The main shortcoming in this design is that nodes a1 and a2 may easily lose their logic value due to the leakage current of transistor TPa and TNa. In addition, our simulation results show that a1 (a2) is highly sensitive to particle strikes when the cell is storing a logic value of '1' ('0').

Two robust SRAM cells have been proposed in [7] (referred to as DICE) and [10] (referred to as JAHIN) in which, unlike the three other SRAM cells mentioned above, they do not use refresh transistors. The general idea behind the design of DICE is using four inverters employing 12 transistors with a structure shown in Figure 3a. When a transient effect emerges at one of its nodes, the error only propagates to the next level and the stored value will not be affected. Figure 3a shows the structure of the DICE cell. The basic idea of the 10-transistor circuit in [10] is using a differential read operation. Figure 3b shows the JAHIN cell. The noise margin (for sub 0.4 V supply voltage at 90 nm) and leakage current of JAHIN are better than those of DICE. In addition, it includes two transistors less than it. However, our study shows that the node pair of (A,C) when the cell is storing '0' and also node pair (B,D) when storing '1' are very sensitive to high-energy particle collisions, which is considered a disadvantage for JAIHN.

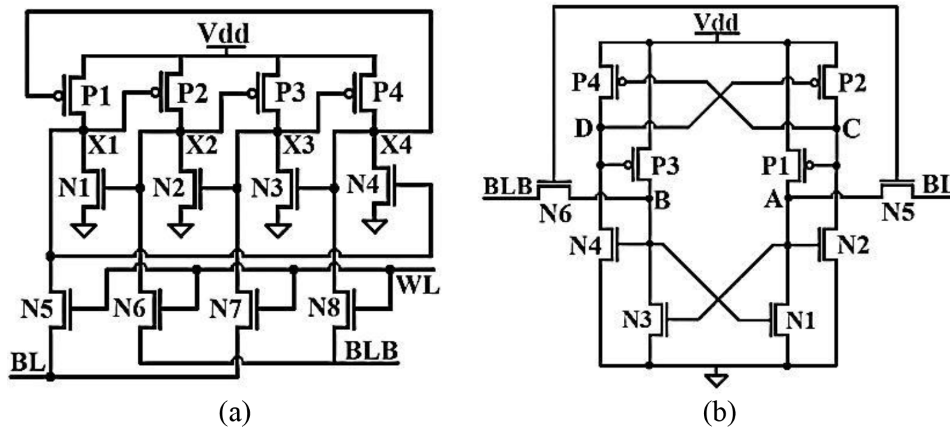

Figure 3. Previous rad-hard SRAM cells: a) proposed cell in [7] b) proposed cell in [10].

3. Proposed hardened memory cells

In this section, we present the proposed radiation hardened SRAM cells. The first low cost SEU tolerant SRAM cell, so-called RATF1, contains 8 transistors. This circuit, which has low power consumption, is much more resistance against SEU in comparison with the conventional 6-transistor SRAM cell. The second circuit, namely RATF2 (an extension to RATF1), includes two more transistors and is fully robust against SEU. Moreover, comparing with our first circuit and other state-of-the-art hardened SRAM cells it offers higher resistance against single event multiple upsets (SEMUs). Moreover, RATF2 occupies a smaller area and provides a reasonable delay and power consumption.

Figure 4a shows the RATF1 cell that, considering bit line and bit line bar transistors, contains 8 transistors. As can be seen in Figure 4a, we placed two transistors in one of the inverters in order to connect/disconnect the feedback path periodically. Signal RL and its complementary, named RLB, turn P2 and N3 ON and OFF frequently. Since the PMOS (NMOS) transistor passes logic value '1' ('0') better than the complementary logic value, we selected PMOS P2 (NMOS N3) to drive PMOS P3 (NMOS N4). Using this

configuration, when transistors in the feedback loop (i.e. P2 and N3) are disconnected, transistors P3 and N3 will go to a more reliable OFF state. Therefore, a transient effect in one side of the loop (e.g., in node X2) cannot pass the loop switches (i.e. P2 and N3) and affect the other side. In Figure 4b, normal operation of our proposed RAMIN cell is shown.

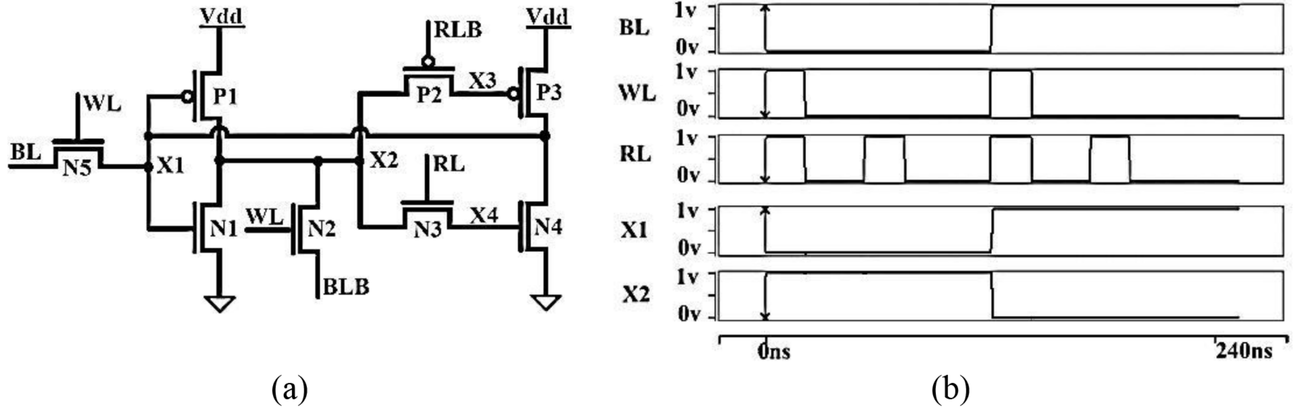

Figure 4. Our first proposed rad-hard SRAM cell (RATF1): a) schematic b) normal operation diagram.

Figure 5a shows the second hardened SRAM cell we have proposed, which contains 10 transistors. Unlike our first design, the structure of RATF2 is symmetrical. As Figure 5a shows, two transistors have been added to each inverter in order to cut the feedback path in most of the times. Similar to RATF1, RL and RLB signals frequently turned P2, P4, N2 and N4 ON and OFF. Regarding to the two additional switch transistors, RATF2 is more robust against SEMU. This is because generally node capacitances are larger than those of RATF1. In addition, both sides of feedback paths are enhanced with switch transistors that have a high resistance in OFF state. In Figure 5b, normal operation of our proposed RATF2 cell is shown.

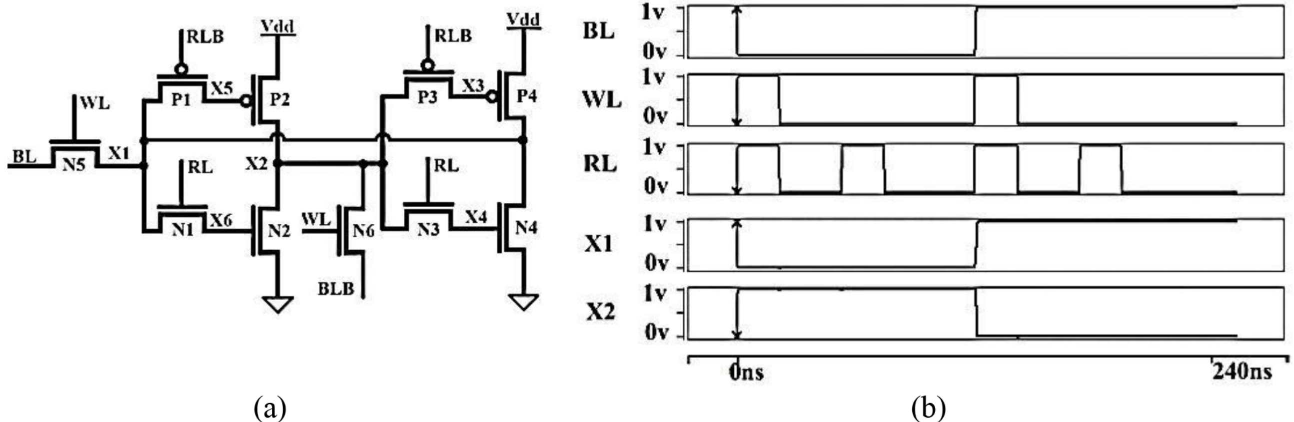

Figure 5. Our second proposed rad-hard SRAM cell (RATF2): a) schematic b) normal operation diagram.

4. Evaluation results

In order to compare our proposed SRAM cells with other previously proposed rad-hard SRAM cells, we have simulated the SRAM circuits by HSPICE tool, using Predictive Technology Model (PTM) 65 nm library [11].

The supply voltage was set to 1 V and temperature to 25 ^{circ}C. Furthermore, to have a fair comparison, we set all transistors to minimum size, i.e. the minimum applicable size that the SRAM cell can have its appropriate functionality.

4.1. Comparative analyses

Usually improving a design parameter will have a negative impact on other parameters. In other words, there is a tradeoff between various design parameters [12]. Therefore, providing the best trade-off between different parameters is an important design challenge. The reliability of memory cells is a major concern in safety-critical applications [9,13] as they hold vital information. For this reason, in this paper, we have promoted the reliability of the SRAM cells considering some emerging reliability issues in current VLSI designs including SEMUs and process variations. Moreover, there are some constraints in power consumption, delay, and area that should be considered in the design. In this section, the proposed SRAM cells are compared with other state-of-the-art rad-hard SRAM cells described in previous sections.

Our proposed RATF1 and RATF2 SRAM cells consist of 8 and 10 transistors (considering bit line and bit line bar transistors), respectively. It should be noted that the proposed memory cell in [8] and [4] consists of 11 and 13 transistors and the DICE cell consists of 12 transistors as well. Generally, additional transistors would cause more power consumption and also occupy more area. Furthermore, the switch transistors of the feedback path could increase circuit delay. To avoid reducing the performance of the circuit, we have considered the size of access transistors larger. In Table 1, the number of transistors, power, delay, and area of SRAM cells are compared. The write delay shown in this table is the average delay of writing ‘0’ and ‘1’ logic values. In addition, access delay is the mean of reading logic values of ‘0’ and ‘1’. For a fair comparison of area, all circuits are drawn in 65 nm CMOS technology. As the reported results in Table 1 show, our proposed RATF1 and RATF2 circuits offer some attractive lower design costs over the previous work. As an example, our proposed RATF1 cell offers the lowest area. A low area, high density. and soft error tolerant bit cell is of interest in many applications [9]. As another example, the proposed RAFT2 circuit has 189.4% lower power consumption and 74.75% lower PDP than the prominent DICE cell [7].

Figures 6a and 6b show the layout of our proposed RATF1and RATF2 SRAM cells.

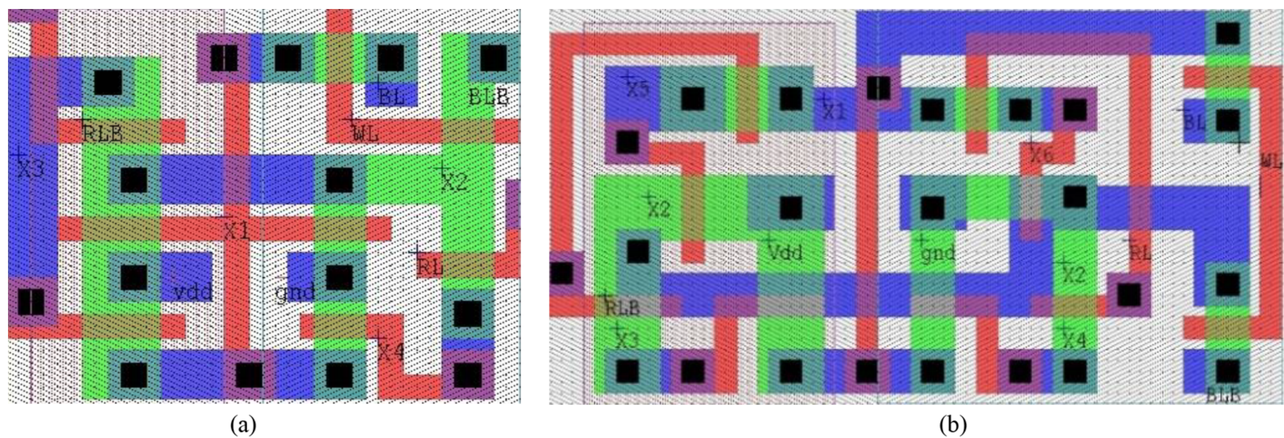

Figure 6. Layouts of proposed SRAM cells: a) RATF1 b) RATF2.

In Figure 7, the static noise margin (SNM) of SRAM circuits is compared. SNM is the maximum static noise that can be tolerated by an SRAM cell without changing its logical state. Static sources of noise are

process offsets and mismatches and operating condition variations [10]. Actually, SNM is the length of the side of the largest square placed in the eyes of the voltage transfer curve (VTC) diagram [14]. The VCT diagram is obtained by applying equal and inverse DC noise to two nodes that keep '0' and '1' logic values (for example, nodes X1 and X2 in Figure 1a). Compared with other circuits using feedback line switching technique [1–3], by 0.9 to 1 V supply voltage, our RATF1 and RATF2 cells offer better SNM. In 1.1 V and 1.2 V the SNM of [9] is better than SRAM circuits designed in this paper. In the same supply voltage, the result of RATF1 and RATF2 is better than that of [8] and [4]. Therefore, there is a trade-off between the SNM and power consumption, related to the supply voltage. Depending on the application, these parameters can be adjusted in such a way that the cell works in appropriate conditions.

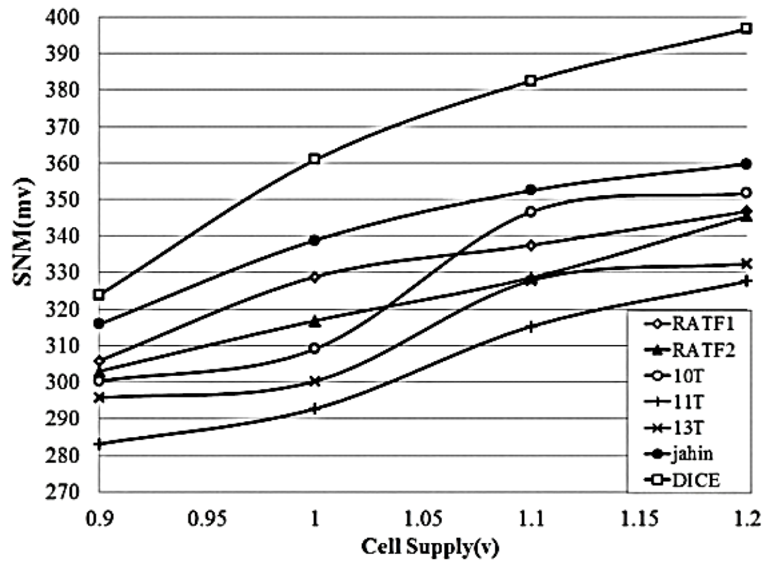

Figure 7. Investigation of static noise margin (SNM) of our RATF1 and RATF2 SRAM cells in comparison with other SEU/SEMU tolerant SRAM cells.

4.2. Radiation robustness in the presence of single event upsets

In order to investigate the SEU tolerance capability of RATF1 and RATF2, we inject charge to all of their nodes. In order to model the charge injection of energetic particle collisions, we use the model presented in [15,16]. This model has been used in many studies such as [3,6,17–19]. This model, indeed, is a mathematical form of an independent current source that includes a double-exponential function and is given by Eq. (1). In this equation, Q_{inj} denotes the amounts of induced charge at time t. Furthermore, τ_1 and τ_2 are time constants that depend on several process-related factors [19]. τ_1 is the collection time constant of the junction. It depends on doping concentration in the silicon material, which is a technology dependent parameter [20]. τ_2 is the time constant for initially establishing the ion track resulted by particle strike. In Eq. (1), the value of τ_2 is assumed to be 5×10^{-11} s. It is negligible comparing to the value of τ_1 [19-20].

Both of our SRAM cells are capable of tolerating any energetic particle strikes into all of their nodes regardless of the deposited charge value when their RL is '0'.

$$I_{inj}(t) = \frac{Q_{inj}}{\tau_1 - \tau_2}\left(e^{-t/\tau_1} - e^{-t/\tau_2}\right) \quad (1)$$

Referring to Figure 8a, assume that the cell is keeping the logic value of '1' and switch transistors of feedback loop are in OFF state and hence the feedback path is disconnected. In this case, transistors N2/P4 are ON and N4/P2 are OFF. If a high-energy particle strikes node X1, this particle will inject some amounts of charge in the struck region. As a result, the logic value of X1 would go to '0' for a short time (see in Figure 8a). As switch transistors are in OFF state, the value of X3 will not change to the complementary logic value (i.e. '0'). Consequently, the resulting transient effect has been masked and the value of node X1 returns to its initial value. In the next lines of this figure, we show SEU injection to other nodes of this circuit. Then the same scenario is repeated for when the cell contains '0' value in Figure 8b. Although the proposed RATF1 circuit takes up a small area and has good robustness against SEUs, the proposed RATF2 SRAM cell shows a higher robustness against SEMUs.

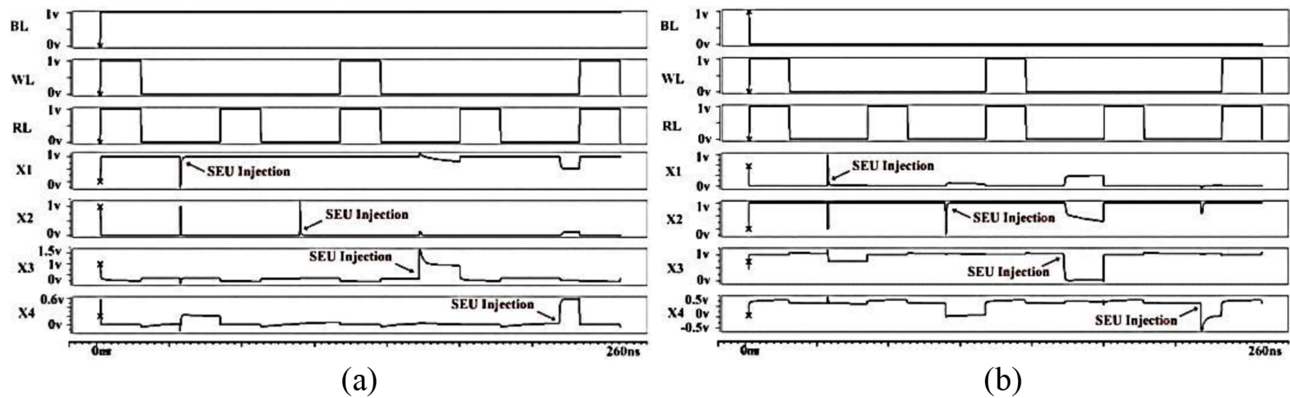

Figure 8. Investigation the SEU tolerance capability of our proposed RATF1 SRAM cell: a) when holding logic value of '1', b) when holding logic value of '0'.

In this part, we repeat the same simulations and charge injection as like as what we did for RATF1. As shown in Figure 9a, assume that the cell is keeping logic value of '1' and refresh transistors are in OFF state. In this case, the feedback path is disconnected, transistors N2 and P4 are ON, transistors N4 and P2 are OFF, and an SEU is injected to node X1. The value of X1 changes to '0' for a short time. As refresh transistors are in OFF state, the value of X2 will not change to '1'. A similar scenario could repeat when the cell contains logic value of '0' (shown in Figure 9b). In cases in which the switch transistors are ON for a short time, energetic particle strikes could alter the stored value of the RATF1, RATF2, 10T [9], 11T [8], and 13T [4]. All these SRAM cells use the periodically ON/OFF feedbacks and hence they have some nodes that striking energetic particles could change the stored value of. Also, the JAHIN cell has susceptive nodes in some cases of holding logics '1' or '0'. In Table 2, we compared the critical charge of susceptive nodes of all considered SRAM cells (except DICE as it does not include any susceptive node in the presence of a single event upset). It should be noted that the JAHIN cell is always prone while the others (10T, 11T, 13T, RATF1, and RATF2) are prone just for a short time to the feedback loop being closed. The associated critical charges are compared in Table 2. The reported values are all normalized based on the related value of the simple SRAM cell (shown in Figure 1).

It also is notable that the frequency and duty cycle of the refresh line (RL) of our RATF1 and RATF2 circuits (and also the proposed 10T, 11T, and 13T cells) should be as low as possible to increase the probability of SEU occurrence. In the performed simulations, the duty cycle of the RL is set to 20%. This value can be lowered depending on the technology.

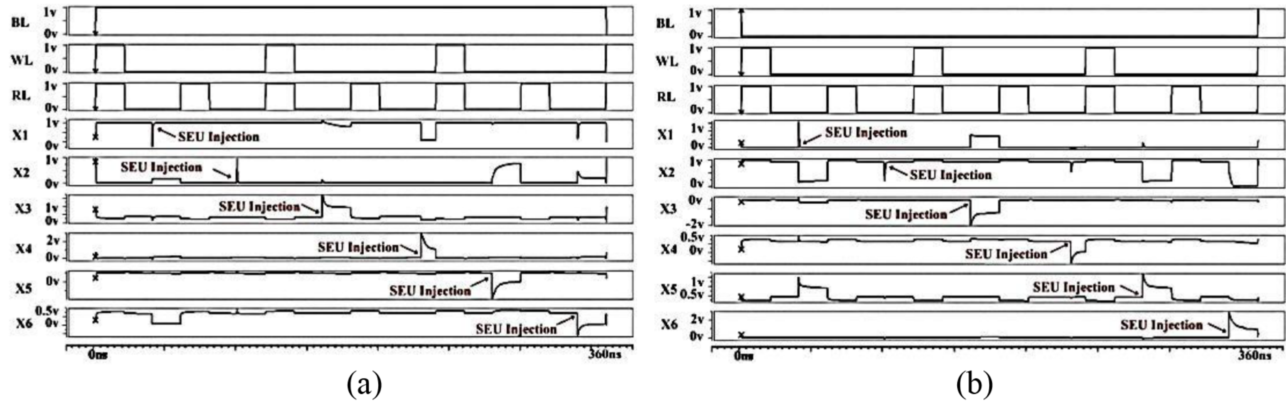

Figure 9. Investigation of the SEU tolerance capability of our proposed RATF2 SRAM cell: a) when holding logic value of '1', b) when holding logic value of '0'.

4.3. Radiation robustness in the presence of single event multiple upsets

To simulate and compare the robustness of SRAM cells in the presence of SEMUs, first we have to recognize pairs of critical nodes of each circuit [20]. Total number of pairs in each circuit (containing n nodes) to select is $\frac{n!}{2(n-2)!}$. After diagnosis of these pairs, we plotted the amount of charge injection to the first node related to the amount of charge injected into the second node for all SRAM cells for the supply voltage of 1 V. In other words, in each curve, each point represents the critical charge of primary affected node versus the secondary one for the affected node pair. Critical charge of a node refers to the minimum charge needed to be injected to this node and alter the stored value of the cell. Each point placed up to this curve will cause an upset. However, a point under the curve would be tolerated by the circuit. Consequently, the area under the curve represents the robustness against SEMU. For a SRAM cell, the node pair that has smaller critical charges than the other pairs is the associated critical node pair. In Figure 10, the associated curve of the most sensitive node-pair of the considered SRAM cells is shown.

As can be seen in Figure 10, near the X and Y axes, the curve tends to infinity. This means that in these regions the circuit is quite robust against SEU. In other words, if the amount of charge injected into a node is zero, any amount of charge deposited to the other node will not cause any upset in the circuit. As Figure 10 reveals, RATF2 has better resistance against multiple nodes upset than other circuits that employed a refreshing technique, because the area under the curve observed for RATF1 is larger than that for the other SRAM cells. However, the DICE cell is a little different. In circuits that are based on refreshing the feedback loop, when the cell is storing a logic value, the feedback line is disconnected for a large portion of the holding time duration. As a result, when the charge deposited on the first node is large enough to alter the value of the node, the robustness against particles strikes that can cause multiple upsets will be determined directly with amount of charge deposited on the secondary affected node. As can be seen in these curves, there are four types of regions for charges. In a region, both the DICE and RATF2 cells are capable of tolerating the double effect particle strikes. In another region, both are not capable. In a region, DICE is capable while the RATF2 is not and in some regions, the RATF2 is capable while DICE is not. It seems that, in reality, it is less probable than the deposited charge is divided equally between the sensitive node pairs and usually more charge is deposited to the primary node than the secondary node [4,20]. Therefore, most of the regions that DICE can tolerate single event double effect and the proposed RATF2 cannot tolerate are not so probable. To the best of our

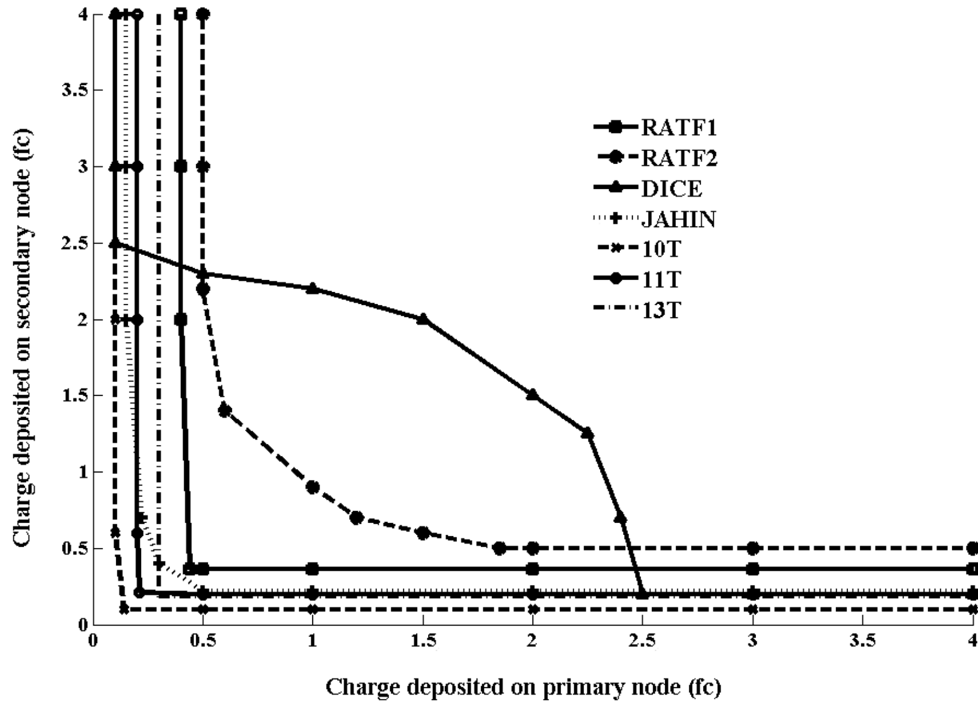

Figure 10. Critical charge plot on critical pair for our proposed SRAM cells in comparison with other SRAM cells.

knowledge, there is no comprehensive study regarding the portion of charge sharing in a single particle strike affecting multiple nodes [4,20]. It would be a valuable study for further related research.

5. Investigation of process variation effects

By shrinking the size of transistors, the impact of process variation (PV) on circuit transistors is increasing [12]. In this section, we investigate the impact of process variation (threshold voltage and transistor dimension variation) on the proposed SRAM cells. In order to figure out the effects of PV on power and delay, a set of simulations have been carried out using HSPICE tool. In Figure 11, variation in power consumption and delay of RATF1, RATF2, and the reference circuit (i.e. Simple 6T SRAM) versus the variation in transistor width (W/L) and threshold voltage (Vth) is shown. Different values for W/L and Vth are obtained randomly using a normal distribution function with different maximum deviations [6]. The maximum deviation varies from 2% to 20% for each case. The simulations are performed 20 times [6]. To make a fair comparison, values are normalized to original values where no variation exists.

From Figure 11, it can be concluded that variation in W/L and V_{th} has a negative impact on both delay and power consumption. However, the sensitivity of the proposed SRAM cells is lower than that of the reference circuit. As can be seen in Figure 11, sensitivity of delay and power consumption to variation in V_{th} is higher than to variation in W/L. However, in comparison with the reference SRAM cell, the proposed SRAM cells offer lower sensitivity. The reasoning of the lower sensitivity of our circuits in comparison with the normal SRAM cell is its larger values associated with power and delay. In fact, as the power consumption and delay of our proposed circuits are higher than those of the normal circuit, process variation can have a lower effect on the mentioned parameters.

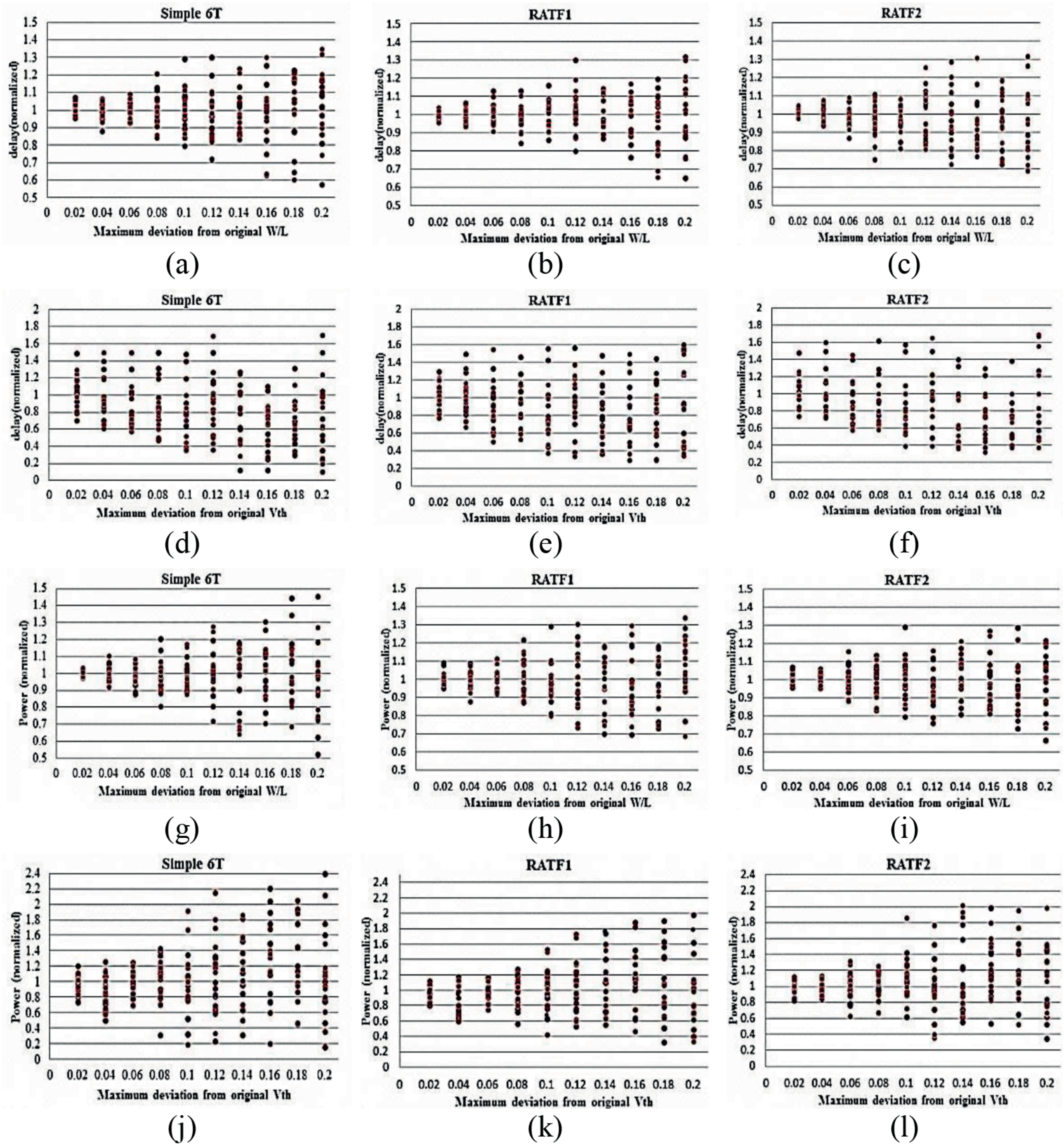

Figure 11. Process variation effect on delay and power consumption of RATF1 and RATF2 in comparison with simple 6T SRAM cell: W/L variation vs. delay of a) 6T cell, b) the RATF1cell, c) the RATF2 cell. Vth variation vs. delay of d) 6T cell, e) the RATF1 cell, f) the RATF2 cell. W/L variation vs. power consumption of g) 6T cell, h) the RATF1 cell, i) the RATF2 cell. Vth variation vs. power consumption of j) 6T cell, k) the RATF1 cell, l) the RATF2 cell.

6. Conclusion

In this paper, two SEU and SEMU tolerant SRAM cells have been proposed and evaluated, the so-called RAFT1 and RAFT2. Generally, the proposed circuits have a high degree of robustness against radiation effects while offering lower overhead in area, power, and performance as compared with other previously proposed radiation hardened SRAM cells. As our simulation results reveal, if a high-energy particle strikes one of the proposed SRAM cells nodes, the stored value will remain unchanged in most of the times and therefore the proposed SRAM cells are mostly robust again SEUs. Furthermore, we showed that, comparing with some of recent and prominent rad-hard SRAM cells, RATF1 and RATF2 are also more robust against SEMU. Our simulation results also showed that the impact of process variation on the power consumption and delay of our proposed SRAM cell is less than those of the reference.

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