Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2017) 25: 1116 – 1136

doi:10.3906/elk-1508-250

Electronically tunable MOS-only current-mode high-order band-pass filters

Pipat PROMMEE[1,*], **Aphinat TIAMSUPHAT**[1], **Muhammad TAHER ABUELMA'ATTI**[2]
[1]Department of Telecommunications Engineering, Faculty of Engineering, King Mongkut's Institute of Technology, Ladkrabang, Thailand
[2]King Fahd University of Petroleum and Minerals, Dhahran, Saudi Arabia

Received: 29.08.2015 • **Accepted/Published Online:** 24.03.2016 • **Final Version:** 10.04.2017

Abstract: This paper presents new CMOS current-mode ladder Chebyshev and elliptic band-pass filters (BPFs). The signal flow graph and the network transformation methods are used to synthesize the proposed BPFs by using Chebyshev and elliptic RLC low-pass prototypes. CMOS-based lossy and lossless integrators with grounded capacitors are used to synthesize the proposed BPFs. The proposed filters can be electronically tuned between 10 kHz and 100 MHz by adjusting the bias current from 0.02 μA to 200 μA. Both filters use a 1.5 V DC power supply, which leads to low dynamic power consumption. Both filters enjoy total harmonic distortion of less than 1.5% along the range of the tuning bias currents. Simulation results are included to illustrate the functionality of the proposed filters.

Key words: Current mode, ladder filters, Chebyshev, elliptic, band-pass filter, CMOS

1. Introduction

In the analog signal processing area, one of the important building blocks is the continuous time filter. Several types of filters are realized for obtaining particular characteristics. Both passive and active filters are used in telecommunication and electronic areas. Unfortunately, passive filters cannot provide tunability features and are not suitable for integration. Recently, tunable active filters have received considerable attention and are continuously developed not only to reduce the circuit die areas but also to improve their performances.

A first-order filter is a basic building block that can be implemented by the well-established operational amplifiers (OpAmps) and operational transconductance amplifiers (OTAs) [1,2]. Some of the first-order functions were realized by different active devices such as the second-generation current-conveyor (CCII) [3]. First-order filters find numerous applications in realizing control systems [4], oscillators [5], and second-order universal filters [6,7]. However, the application of first-order filters is limited due to their frequency response characteristic. To achieve a better performance, second-order filters can be used and several realizations are available using OpAmps and OTAs; see, for example, [8,9] and the references cited therein. Alternated active devices, OTRA [10] and CDTA [11], have also been introduced to realize the tunable active filter. Although they can provide many types of frequency responses, they suffer from the need for a large number of active elements and can therefore operate only at relatively low frequencies. In telecommunications, for example, high performance filters operating at relatively high frequencies are needed and usually low-order filters (first-order and second-order) cannot be used for achieving the required selective frequency responses. MOS-only multifunction second-order filters were introduced [12–14] using their gate-source intrinsic capacitors. Unfortunately,

*Correspondence: pipat@telecom.kmitl.ac.th

it seems that the parasitic elements affect the filter performances and response of filters cannot be achieved in electronic tunability. High-order filters are therefore needed as they can provide the superior performance required for selecting the desired frequencies and rejecting the undesired ones.

Realizing high-order ladder filters using the RLC network is a well-known method; see, for example, [15,16]. The simulated RLC network prototype using a generalized impedance converter (GIC) circuit is one of the methods used for realizing high-order filters [15–17]. High-order LPF based on GIC has been introduced by using OpAmps and an RC network [18]. The circuit uses many floating passive elements and cannot provide electronic tuning and is, therefore, not suitable for integration. The signal flow graph (SFG) method was used to simulate the RLC ladder filters [19,20] by using MOS switched capacitor integrators. Several active high-order filters based on gm-C [21–24] and its improvements [25] were developed with different structures. Operation in current-mode, rather than voltage-mode as in the previously mentioned references, is a promising approach for implementing high-performance and low-voltage circuits. An interesting CMOS-based current-mode high-order LPF for higher frequency applications was presented in [26]. The CCII with SFG method was also used to develop a current-mode high-order LPF [27]. Multiple loop feedback using OTA-C is another method for realizing a high-order LPF. It is suitable for synthesizing from high-order all-pole biquad functions [28,29]. However, no tunable current-mode high-order BPF has been introduced.

The major intention of this paper is, therefore, to present CMOS-based electronically tunable current-mode ladder Chebyshev and elliptic BPFs. The proposed filters are obtained using the SFG and transformed RLC passive low-pass filters prototypes. The proposed current-mode ladder Chebyshev BPF uses 33 MOS transistors and 6 grounded capacitors. The proposed current-mode ladder elliptic BPF uses 52 MOS transistors and 7 ground capacitors. Both of the proposed filters enjoy many advantages, including relatively low number of active and passive components, low power consumption, low voltage supply, relatively very high frequency operation, and a wide range of electronic tuning of the filter parameters.

2. Theory and principle of operation

2.1. CMOS-based lossy and lossless integrator

Figure 1 illustrates the block diagram of the inverting lossy integrator with 2 equal outputs Y_1 and Y_2, given by the transfer function of Eq. (1).

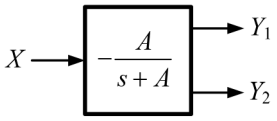


Figure 1. Block diagram of dual-output lossy integrator.

$$\frac{Y_1}{X} = \frac{Y_2}{X} = -\frac{A}{s+A} \tag{1}$$

Using the block diagram in Figure 1, a lossless integrator can be realized by adding an inverting gain to the output Y_1 and then feeding it back to input as shown in Figure 2. Hence, the output transfer functions of the obtained positive and negative lossless integrator functions as Z_1 and Z_2 can be expressed as follows.

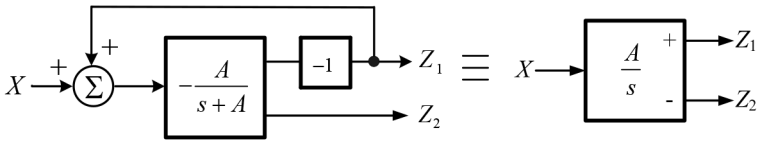


Figure 2. Block diagram of the lossless dual-output integrator.

$$\frac{Z_1}{X} = \frac{A}{s} \tag{2}$$

$$\frac{Z_2}{X} = -\frac{A}{s} \tag{3}$$

The CMOS-based lossy integrator with positive and negative outputs (I_{O1} and I_{O2}) can be implemented as shown in Figure 3 and its small signal model is shown in Figure 4. Assuming that transconductances of the transistors (g_{mi}) are matched ($g_{mi} = g_m$), the transfer function can be expressed as follows.

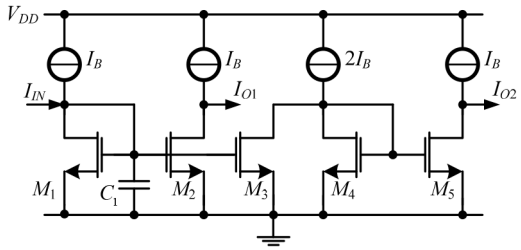


Figure 3. CMOS-based lossy integrator with positive and negative outputs.

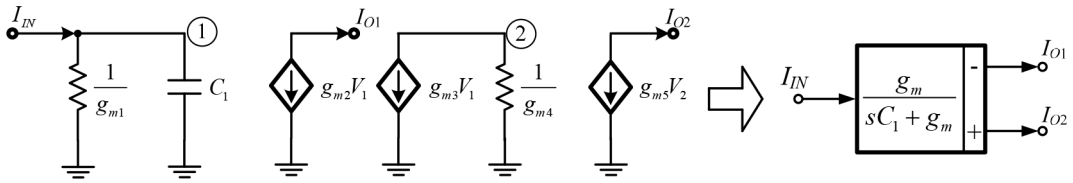


Figure 4. Small signal model of Figure 3 and its simplified block diagram.

$$\frac{I_{O1}}{I_{IN}} = -\frac{g_m}{sC_1 + g_m} \tag{4}$$

$$\frac{I_{O2}}{I_{IN}} = \frac{g_m}{sC_1 + g_m} \tag{5}$$

Using Figure 2, the CMOS-based lossless integrator can be implemented as shown in Figure 5. By cascading the lossy integrator formed of M_1 and M_2 with inverting gain stage M_4 and M_5 and feeding back its output to the input, two outputs, I_Y and I_Z, can be obtained from M_2 and M_6, respectively. Considering the small signal model of the lossless integrator of Figure 6, assuming that transconductances of the transistors (g_{mi}) are matched ($g_{mi} = g_m$), the transfer functions of the lossless integrator can be expressed as follows.

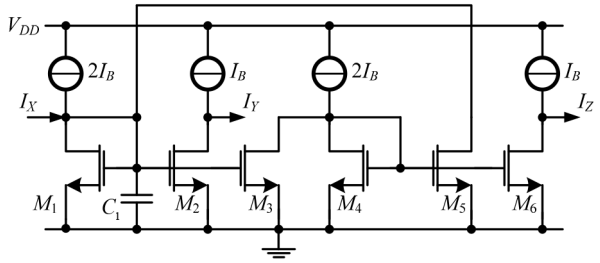


Figure 5. CMOS-based lossless integrator with positive and negative outputs.

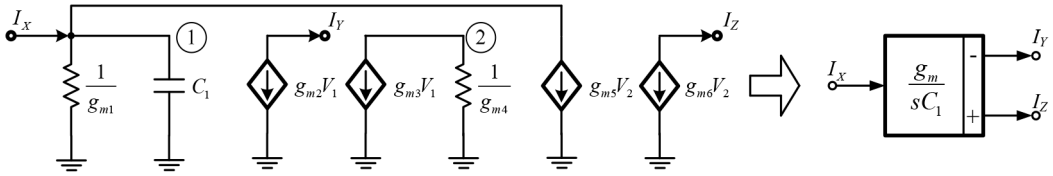


Figure 6. Small signal model of Figure 5 and its simplified block diagram.

$$\frac{I_Y}{I_X} = -\frac{g_m}{sC_1} \tag{6}$$

$$\frac{I_Z}{I_X} = \frac{g_m}{sC_1} \tag{7}$$

In Eqs. (4)–(7) the transconductance g_m can be expressed as

$$g_m = \sqrt{2\mu C_{OX}\frac{W}{L}I_B}, \tag{8}$$

where μ, C_{ox}, W, and L are surface mobility, channel oxide capacitance, channel width, and channel length of the MOS transistor. From Eq. (8), it is clear that the transconductance can be tuned through bias current I_B.

2.2. Design of RLC passive ladder band-pass filters using low-pass filter prototypes

2.2.1. Chebyshev band-pass ladder filter

The sixth-order Chebyshev band-pass ladder filter prototype can be realized by using the transformation of the doubly terminated RLC passive Chebyshev ladder LPF prototype in Figure 7 and the network transformation in the Table. Figure 8 shows the resulting Chebyshev RLC sixth-order BPF ladder prototype.

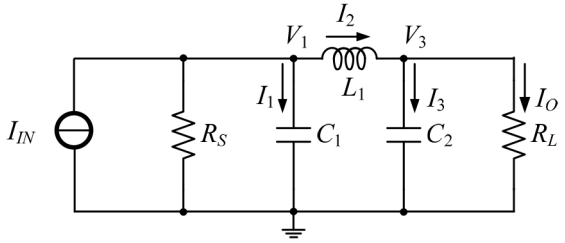


Figure 7. Doubly terminated Chebyshev RLC passive ladder low-pass filter prototype.

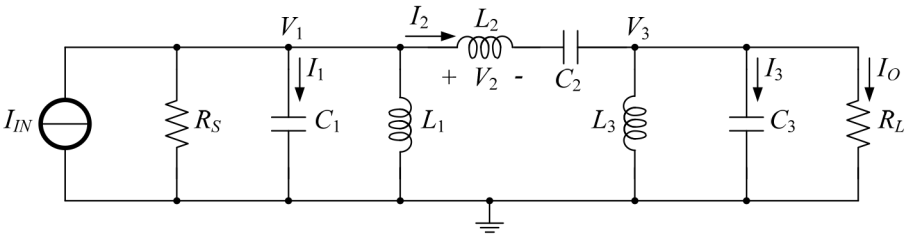
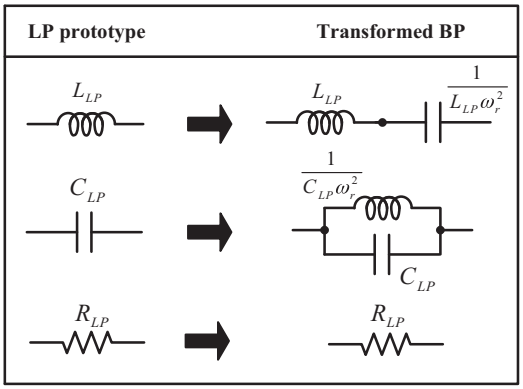


Figure 8. Transformed Chebyshev RLC passive ladder BPF prototype.

Table. RLC network transform.



Considering Figure 8 and using KCL yields the following.

$$V_1 = \frac{I_1}{sC_1} \tag{9}$$

$$V_2 = V_1 - V_3 - \frac{I_2}{sC_2} \tag{10}$$

$$V_3 = \frac{I_3}{sC_3} \tag{11}$$

$$I_1 = I_{IN} - \frac{V_1}{R_S} - \frac{V_1}{sL_1} - I_2 \tag{12}$$

$$I_2 = \frac{V_2}{sL_2} \tag{13}$$

$$I_3 = I_2 - \frac{V_3}{sL_3} - \frac{V_3}{R_L} \tag{14}$$

Eqs. (9)–(14) can be represented by the SFG shown in Figure 9. Normalizing voltage terms into current terms by using transconductance (g_m) and replacing the lossless integrators with negative feedbacks at the beginning and the end of the prototype by lossy integrators, the resulting SFG is shown in Figure 10. Based on the SFG of Figure 10, the BPF can be implemented by using lossy and lossless integrators, which is described in the next section.

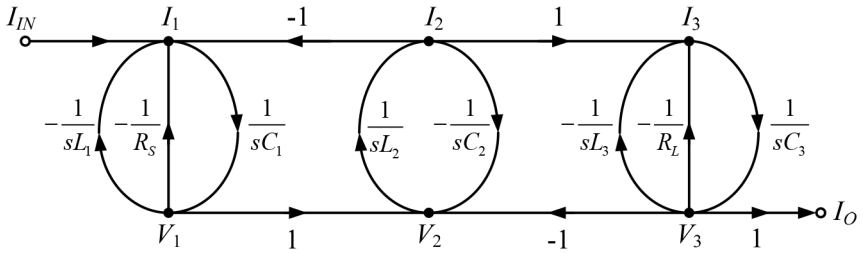


Figure 9. SFG of sixth-order Chebyshev RLC passive ladder BPF prototypes.

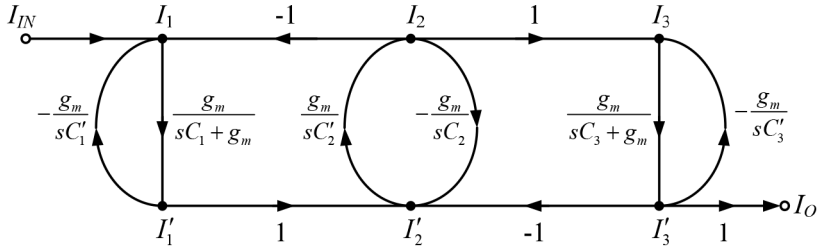


Figure 10. Normalized SFG of Figure 9.

2.2.2. Elliptic band-pass ladder filter

A sixth-order elliptic band-pass ladder filter prototype can also be realized based on the transformation of the doubly terminated RLC passive ladder elliptic low-pass filter prototype shown in Figure 11 by using the network transformation in the Table. Figure 12 shows the elliptic RLC band-pass ladder filter prototype based on the network transformation method in the Table.

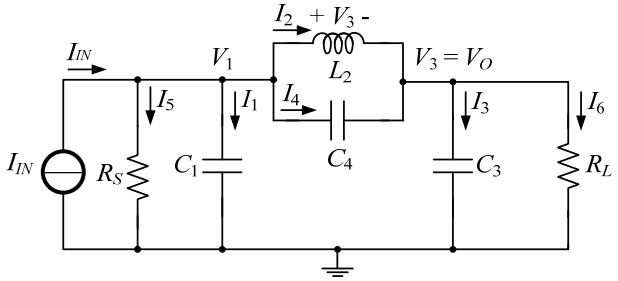


Figure 11. Doubly terminated elliptic RLC passive ladder LPF prototype.

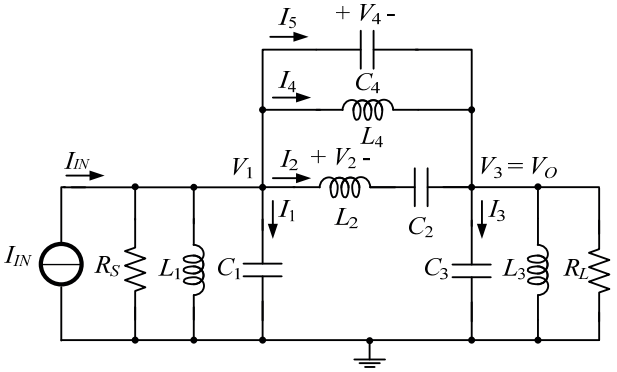


Figure 12. Transformed elliptic RLC passive ladder BPF prototype.

Considering Figure 12 and using KCL yields the following.

$$I_1 = I_{IN} - I_2 - I_4 - I_5 - V_1/sL_1 - V_1/R_S \tag{15}$$

$$I_2 = \frac{V_2}{sL_2} \tag{16}$$

$$I_3 = I_2 + I_4 + I_5 - \frac{V_3}{sL_3} - \frac{V_3}{R_L} \tag{17}$$

$$I_4 = \frac{V_4}{sL_4} \tag{18}$$

$$V_1 = \frac{I_{IN} - I_2 - I_4 - V_1/sL_1 - V_1/R_S}{s\left(C_1 + C_4\right)} + V_3\frac{C_4}{C_1 + C_4} \tag{19}$$

$$V_2 = V_1 - V_3 - \frac{I_2}{sC_2} \tag{20}$$

$$V_3 = \frac{I_2 + I_4 - V_3/sL_3 - V_3/R_L}{s\left(C_3 + C_4\right)} + V_1\frac{C_4}{C_3 + C_4} \tag{21}$$

$$V_4 = V_1 - V_3 = V_2 + \frac{I_2}{sC_2} \tag{22}$$

From Eqs. (19) and (21), a modified RLC prototype can be obtained by replacing capacitor C_4 with two new capacitors (C_1+C_4 and C_3+C_4) connected with dependent voltage sources. The resulting modified elliptic RLC passive ladder BPF prototype is shown in Figure 13.

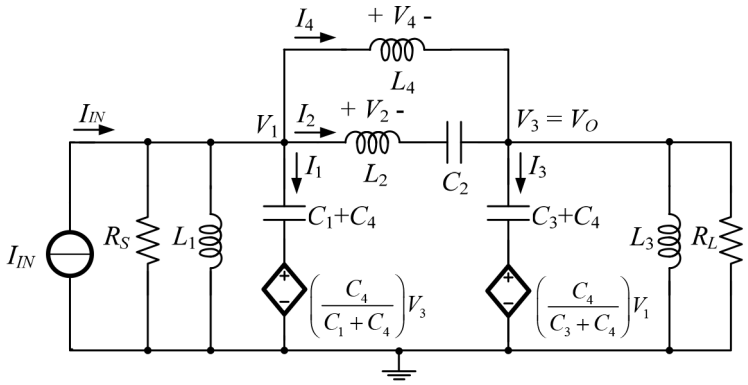


Figure 13. Modified elliptic RLC passive ladder BPF prototype.

A SFG can be drawn from Eqs. (15)–(22) as shown in Figure 14. Normalizing voltage terms into current terms by using transconductance (g_m), replacing the variables R_S and R_L by $1/g_m$, and replacing the lossless integrators with negative feedbacks at the beginning and the end of the prototype by lossy integrators, the resulting SFG is shown in Figure 15.

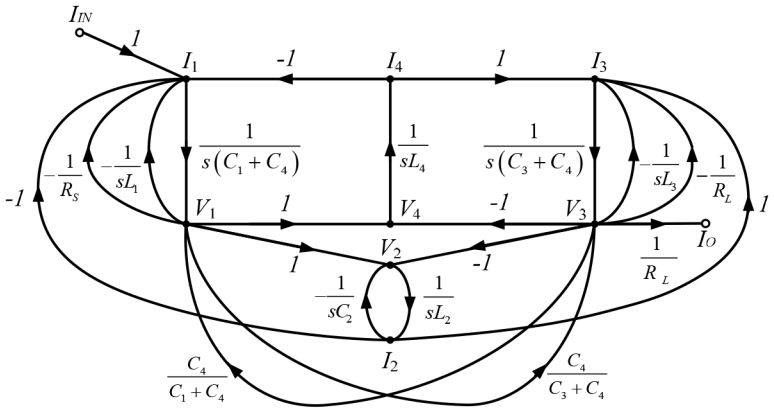


Figure 14. SFG of elliptic RLC passive ladder BPF prototype.

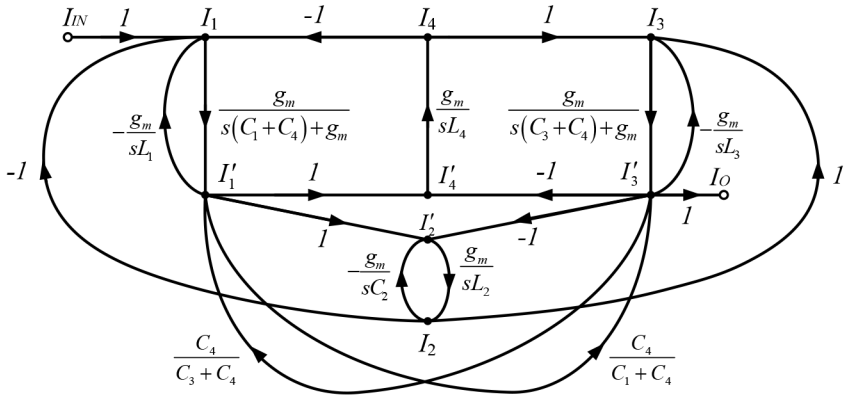


Figure 15. Normalized SFG in Figure 14.

3. Realization of CMOS-based ladder BPF

From the normalized SFG of Figure 10, a sixth-order current-mode Chebyshev ladder BPF can be easily realized using the lossy and lossless integrator block diagrams of Figures 4 and 6 and replacing inductors L_i by capacitors C_i' as shown in Figure 16. Using Figure 16, the CMOS-based implementation of the Chebyshev ladder bandpass filter can be obtained and is shown in Figure 17.

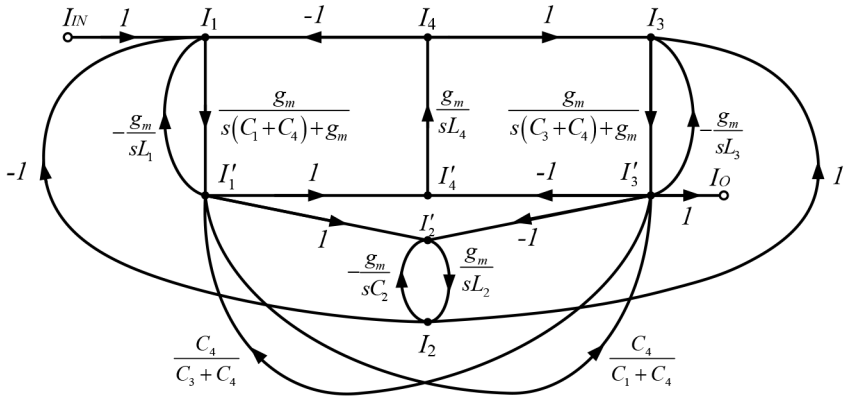


Figure 16. Sixth-order Chebyshev ladder BPF.

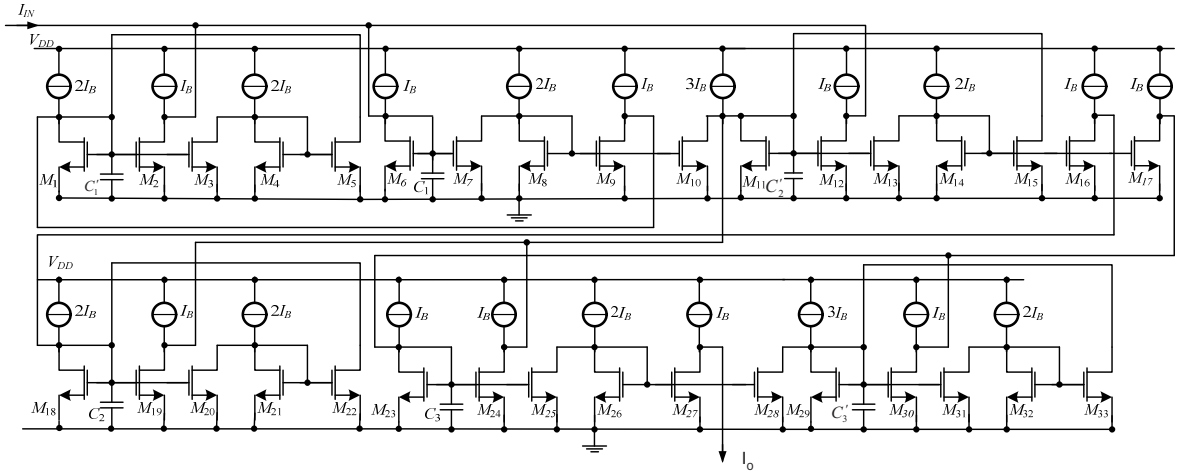


Figure 17. Proposed CMOS-based sixth-order Chebyshev ladder BPF.

In the SFG of Figure 15, there are feedback loops between two nodes (I_1' and I_3') with current gains (k). Following the same procedure described for the Chebyshev ladder BPF, the sixth-order current-mode elliptic ladder BPF can be realized as shown in Figure 18.

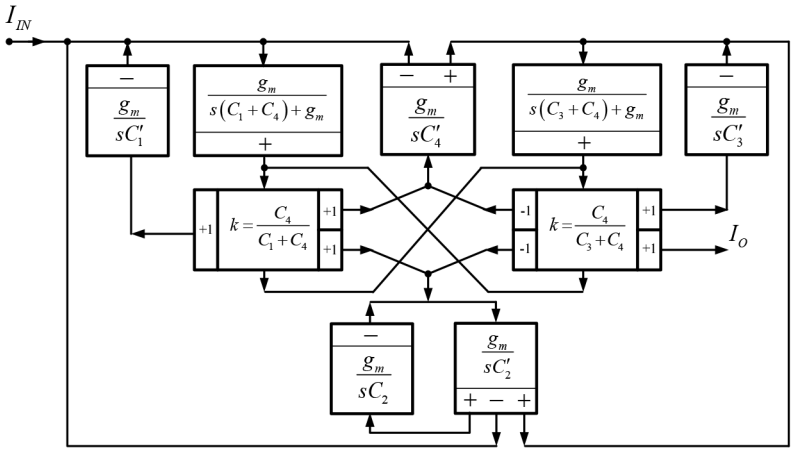


Figure 18. Sixth-order elliptic ladder BPF.

The proposed elliptic sixth-order ladder BPF contains 2 lossy integrators, 5 lossless integrators, and 2 multiple output gain stages. The positive and negative current buffers and current gain (k) can be realized as shown in Figure 19.

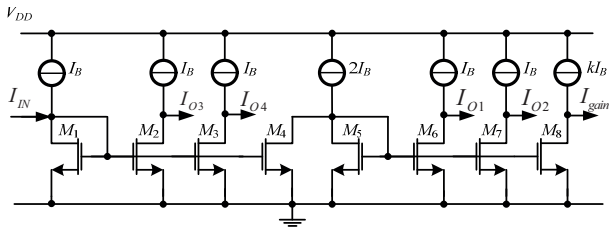


Figure 19. Multiple outputs current amplifier/buffer.

In Figure 19 all the MOS transistors have the same transconductance except transistors M_i and M_8 (i = 1,2,...,7) having transconductances equal to g_{m1} and g_{m2}, respectively. Thus, the current gain can be expressed as follows.

$$k = \frac{g_{m2}}{g_{m1}} \tag{23}$$

Figure 20 shows an implementation of the CMOS-based sixth-order current-mode elliptic ladder BPF using the lossy and lossless integrators of Figures 3 and 5. Note that the highlighted blocks are the current gains (k), which are actually less than 1 according to Eq. (23).

4. Nonideal analysis

This section describes the influences of the NMOS transistors' parasitic components. Lossy and lossless integrators are the main building blocks of the proposed circuits. The performance of these building blocks may deviate from the ideal analysis while operating at relatively high frequencies. This is usually attributed to the effect of the transistors' parasitic components. Nonideal analysis of the integrators including the effect

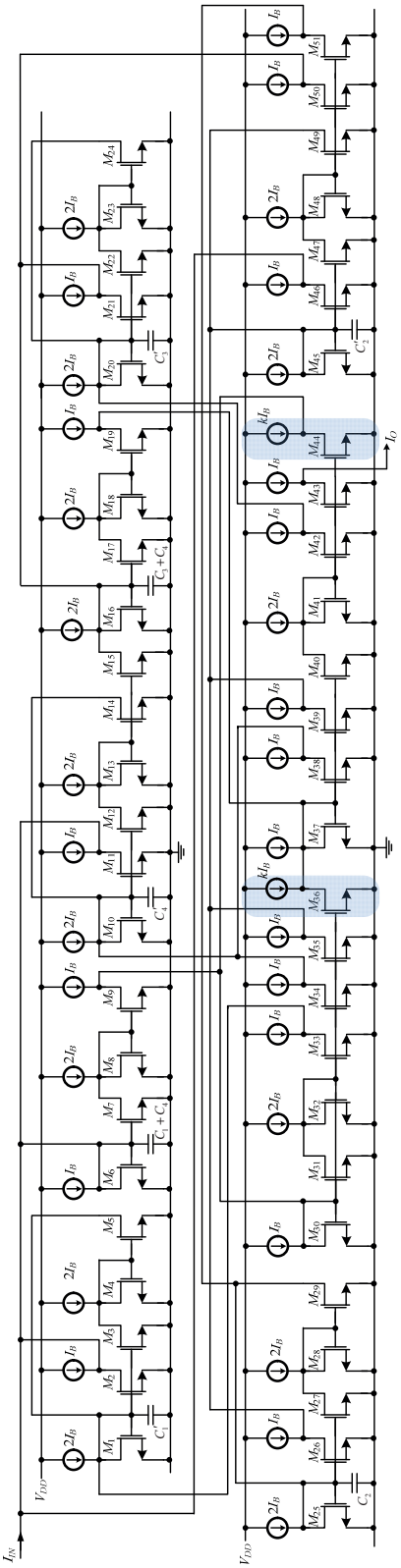


Figure 20. Proposed CMOS-based sixth-order current-mode elliptic ladder BPF.

of the transistors' parasitic components can be performed by using the simplified small signal model of NMOS transistors shown in Figure 21.

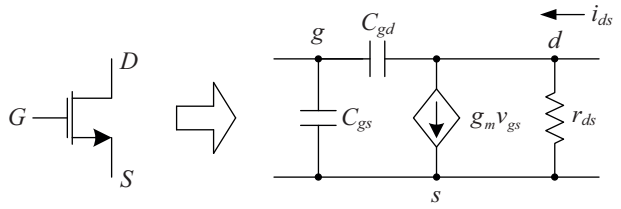


Figure 21. Simple small signal model of MOS transistor.

In the small signal model shown in Figure 21, the input parasitic capacitances (C_{gs} and C_{gd}), the resistance (r_{ds}), and the transconductance (g_m) are incorporated. The effects of the transistor parasitic components on the performance of the proposed BPFs are described in the following subsections.

4.1. Parasitic capacitance (C_{gd} and C_{gs})

This section will consider the effect of the parasitic capacitances (C_{gd} and C_{gs}), which is important for determining the performance of a circuit, particularly at high frequencies.

4.1.1. Lossy integrators

Using the small signal model of the MOS transistor of Figure 21, considering only the parasitic gate-drain capacitance (C_{gd}), and assuming that the transconductances of the MOS transistors are identical, the transfer functions of the lossy integrator of Figure 3 can be approximated by Eqs. (24) and (25), respectively.

$$\frac{I_{O1}}{I_{IN}} = \frac{-g_m}{g_m + s(C_{gd2} + C_1)} \tag{24}$$

$$\frac{I_{O2}}{I_{IN}} = \frac{g_m}{g_m + s\left(3C_{gd2} + C_{gd4} + C_1\right)} \tag{25}$$

Similarly, considering only the parasitic gate-source capacitance (C_{gs}), and assuming that the transconductances of MOS transistors are identical, the transfer functions of the lossy integrator of Figure 3 can be approximated by Eqs. (26) and (27), respectively.

$$\frac{I_{O1}}{I_{IN}} = \frac{-g_m}{g_m + s(C_{gs1} + C_{gs2} + C_1)} \tag{26}$$

$$\frac{I_{O2}}{I_{IN}} = \frac{g_m}{g_m + s\left(C_{gs3} + C_{gs4} + C_{gs1} + C_{gs2} + C_1\right)} \tag{27}$$

Eqs. (24)–(27) show the effect of the parasitic capacitances on the lossy integrator performance. In saturation operation, the parasitic gate-drain capacitance (C_{gd}) and gate-source capacitance (C_{gs}) will vary depending on the bias current. Assuming that the parasitic capacitances $C_{gdi} = C_{gd}$, $C_{gsi} = C_{gs}$ with $C_{gd} = WL_DC_{ox}$ and $C_{gs} = W\left((2/3)(L) + L_D\right)C_{ox}$, it can be seen that parasitic capacitances C_{gd} and C_{gs} produce a small deviation in the frequency response of the lossy integrator. To prevent significant errors, capacitance C_1 should be selected so that

$$C_1 >> 4\left(C_{gs} + C_{gd}\right). \tag{28}$$

4.1.2. Lossless integrators

Likewise, the effect of the parasitic gate-drain and gate-source capacitance (C_{gd} and C_{gs}) on the inverting and noninverting lossless integrator of Figure 5 can be considered. Assuming that the transconductances of MOS transistors are identical, the transfer functions of the lossless integrator affected by the parasitic capacitances C_{gd} and C_{gs} can be approximated by the following equations.

$$\frac{I_{Y1}}{I_X} = \frac{-g_m}{s\left(4C_{gd3} + 4C_{gd5} + C_{gd2} + C_1\right)} \tag{29}$$

$$\frac{I_{Z1}}{I_X} = \frac{g_m}{s\left(4C_{gd2} + 4C_{gd4} + C_{gd5} + C_1\right)} \tag{30}$$

$$\frac{I_{Y2}}{I_X} = \frac{-g_m}{s\left(C_{gs1} + C_{gs2} + C_{gs3} + C_{gs4} + C_{gs5} + C_1\right)} \tag{31}$$

$$\frac{I_{Z2}}{I_X} = \frac{g_m}{s\left(C_{gs1} + C_{gs2} + C_{gs3} + C_{gs4} + C_{gs5} + C_1\right)} \tag{32}$$

Eqs. (29)–(32) show the effect of the parasitic capacitances (C_{gd} and C_{gs}) on the lossless integrator performance. In the saturation region, the parasitic gate-drain and gate-source capacitances (C_{gd} and C_{gs}) will vary depending on the bias current. To prevent significant errors, capacitance C_1 should be selected so that

$$C_1 >> 9C_{gd} + 5C_{gs}. \tag{33}$$

From Eq. (33), it is clear that the errors can be minimized by selecting relatively large values for the capacitance (C_1).

4.2. Parasitic conductance (g_{ds})

In Figure 21 the voltage-controlled current source, $g_m v_{gs}$, is the most important component of the model, with the transistor current-voltage relationship given by

$$i_{DS} = \frac{\mu_n C_{ox} W}{2L}\left(v_{GS} - V_T\right)^2\left(1 + \lambda v_{DS}\right). \tag{34}$$

In Eq. (34) $\lambda < 1\ (\mathrm{V})^{-1}$ represents the channel-length modulation effect. It produces the slope of the drain current as a function of the drain-to-source voltage (v_{DS}). The channel conductance will be dependent upon L through λ, which is inversely proportional to $L\,(\lambda \propto 1/L)$. The small-signal channel conductance g_{ds} can be expressed as

$$g_{ds} = \frac{\partial i_{DS}}{\partial v_{DS}} = \frac{\lambda i_{DS}}{1 + \lambda v_{DS}} \approx \lambda i_{DS}. \tag{35}$$

4.2.1. Lossy integrator

Using the small signal model of Figure 21 for the MOS transistor, considering only the effect of the parasitic conductance, and assuming that the transconductances of the MOS transistors are identical, the transfer

functions of the lossy integrator of Figure 3 can be rewritten as follows.

$$\frac{I_{O1}}{I_{IN}} = \frac{-g_m}{g_m + g_{ds1} + sC_1} \tag{36}$$

$$\frac{I_{O2}}{I_{IN}} = \frac{(g_m)^2}{(g_m)^2 + g_m\left(g_{ds1} + g_{ds2} + g_{ds3}\right) + sC_1\left(g_m + g_{ds2} + g_{ds3}\right)} \tag{37}$$

Assuming that $g_{dsi} = g_{ds}$ for all the transistors and since the parasitic conductance $g_{ds} << g_m$, then Eq. (37) reduces to

$$\frac{I_{O2}}{I_{IN}} \approx \frac{g_m}{g_m + 3g_{ds} + sC_1}. \tag{38}$$

Eq. (38) shows that in order to avoid significant errors in the transfer functions of the lossy integrators the transconductance g_m must satisfy the following condition.

$$g_m >> 3g_{ds} \tag{39}$$

Inspection of Eqs. (11) and (39) shows that significant errors can be prevented if a large transistor width (W) is used.

4.2.2. Lossless integrator

Likewise, taking only the effect of the parasitic drain-source conductance (g_{ds}) into consideration, the inverting and noninverting lossless integrator transfer functions of Figure 5 can be rewritten as follows.

$$\frac{I_{Ya}}{I_X} = \frac{-(g_m)^2}{g_m\left(g_{ds1} + g_{ds3} + g_{ds4} + g_{ds5}\right) + sC_1\left(g_m + g_{ds3} + g_{ds4}\right)} \tag{40}$$

$$\frac{I_{Za}}{I_X} = \frac{(g_m)^2}{g_m\left(g_{ds1} + g_{ds2} + g_{ds3} + g_{ds4}\right) + sC_1\left(g_m + g_{ds2} + g_{ds3}\right)} \tag{41}$$

Eqs. (40) and (41) show how the parasitic drain-to-source conductance (g_{ds}) affects the lossless integrator transfer functions of Figure 5. Assuming that the transconductances of MOS transistors are identical, then Eqs. (40) and (41) reduce to the following.

$$\frac{I_{Ya}}{I_X} \approx \frac{-g_m}{4g_{ds} + sC_1} = \left(\frac{-g_m}{4g_{ds}}\right)\frac{4g_{ds}/C_1}{s + 4g_{ds}/C_1} \tag{42}$$

$$\frac{I_{Za}}{I_X} \approx \frac{g_m}{4g_{ds} + sC_1} = \left(\frac{g_m}{4g_{ds}}\right)\frac{4g_{ds}/C_1}{s + 4g_{ds}/C_1} \tag{43}$$

From Eqs. (42) and (43), it can be seen that both outputs of the lossless integrator are affected by the parasitic conductance (g_{ds}) as a parasitic pole at very low frequency ($\omega_L = 4g_{ds}/C_1$) will appear in the transfer functions. However, these effects will be significant at very low frequency where the operating frequency is much larger than the frequency of the parasitic pole. Thus, the resulting parasitic poles will provide the lower frequency limitation of the lossless integrator and maximum gain at low frequency will be given by ($|k| = g_m/4g_{ds}$).

5. Simulation results

In this section PSpice simulation results obtained from the integrators, the Chebyshev BPF, and the elliptic BPF are presented. All simulations were carried out using model TSMC 0.25 μm CMOS technology [30] and a 1.5 V DC power supply.

The frequency responses of CMOS-based lossy integrator in Figure 3 and lossless integrator in Figure 5 are shown in Figures 22 and 23. Following the results of the nonideal analysis, the capacitor $C_1 = 10$ pF is selected to prevent the effect of parasitic capacitances, and the aspect ratios of the MOS transistors of Figures 3 and 5 of $W/L = 70$ μm/0.5 μm were selected to prevent the errors of all integrators. Figures 22 and 23 clearly show that the frequency responses can be tuned roughly between 10 kHz and 100 MHz by adjusting the bias current I_B [0.02, 0.2, 2, 20, 200] μA.

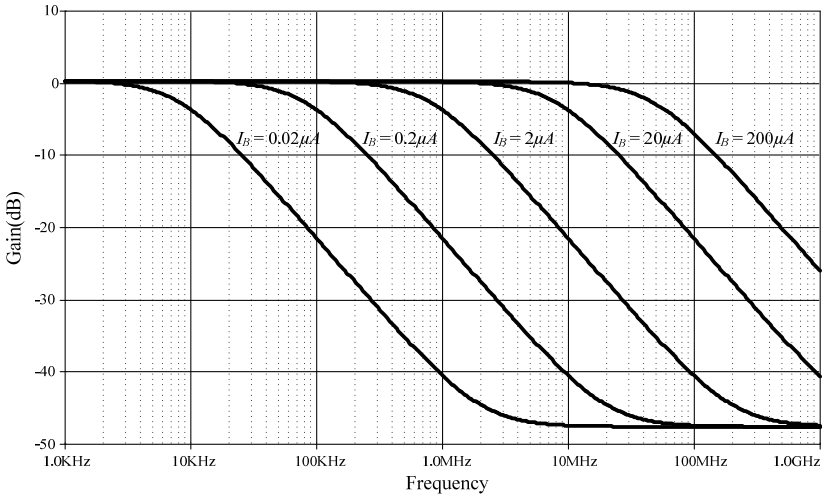


Figure 22. Variation of the magnitude responses of the lossy integrator in Figure 3 by adjusting the bias current (I_B).

The proposed sixth-order Chebyshev ladder BPF RLC prototype obtained was simulated using $C_1 = C_2 = C_3 = 20nF$, $L_1 = L_2 = L_3 = 20nH$, $R_S = R_L = 1\,\Omega$, 1.5 V DC power supply, W/L = 70 μm/0.5 μm, bias current $I_B = 20$ μA, and $C_1 = C_2 = C_3 = C_1' = C_2' = C_3' = 10$ pF. The results obtained are shown in Figure 24. Inspection of Figure 24 clearly shows that the magnitude responses are almost the same, but in the pass-band the ripples are slightly different with error around 0.8 dB. The electronically tunable frequency responses of the proposed BPF were obtained by adjusting the bias current I_B [0.02, 0.2, 2, 20, 200] μA. Figure 25 shows the tunability feature of frequency responses between 10 kHz and 100 MHz. The input impedance in the pass-band at bias current $I_B = 200$ μA is around 200 Ω, as shown in Figure 26.

The simulation results of the proposed sixth-order elliptic ladder BPF RLC prototype were obtained using $C_1 = C_2 = C_3 = 25$ nF, $C_4 = 2.5$ nF, $L_1 = L_2 = L_3 = 25$ nH, $L_4 = 250$ nH, $R_S = R_L = 1$ Ω, 1.5 V DC supply, and W/L = 70 μm/0.5 μm for all transistors, except the transistors at outputs, which are set with W/L = 5 μm/0.5 μm to provide $k = 0.1$ I_B. The values of capacitors are set as $C_1 + C_4 = 12$ pF, $C_3 + C_4 = 12$ pF, $C_2 = 15$ pF $C_1' = 10$ pF, $C_4' = 100$ pF, $C_3' = 10$ pF, and $C_2' = 15$ pF and bias current $I_B = 20$ μA. Magnitude responses of the proposed filter and its prototype are shown in Figure 27. It can be seen that the magnitude response of the proposed filter has a small error in the left-hand side of the stop-band and its pass-band ripples are around 2 dB more than its prototype.

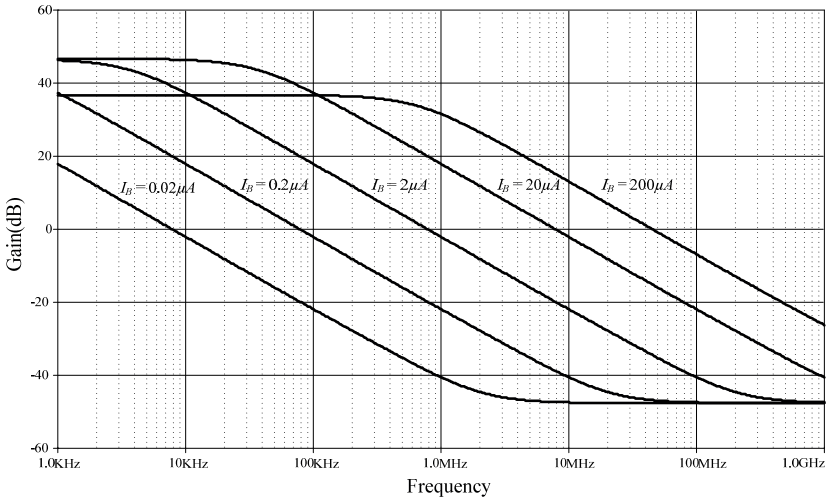


Figure 23. Variation of the magnitude responses of the lossless integrator of Figure 5 by adjusting the bias current (I_B).

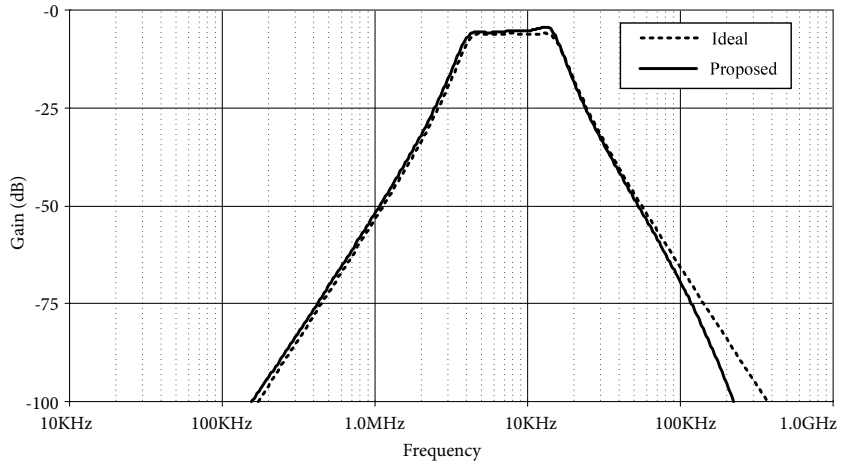


Figure 24. Magnitude responses of the proposed Chebyshev BPF (I_B = 20 μA) and its RLC prototype.

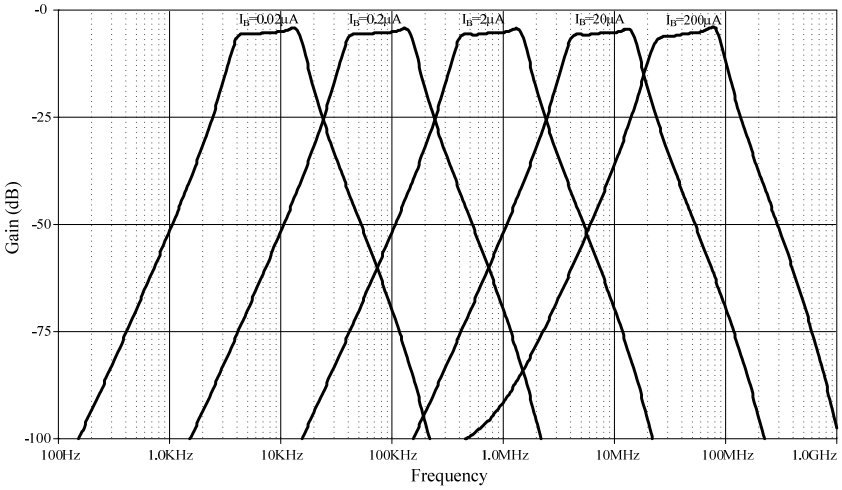


Figure 25. Electronic tunability of the proposed Chebyshev BPF by adjusting I_B [0.02, 0.2, 2, 20, 200] μA.

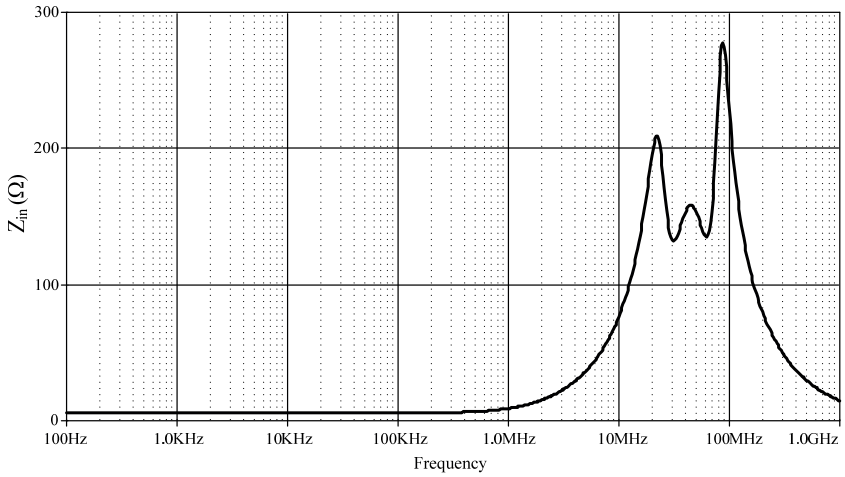


Figure 26. Input impedance of sixth-order Chebyshev BPF ($I_B = 200\ \mu$A).

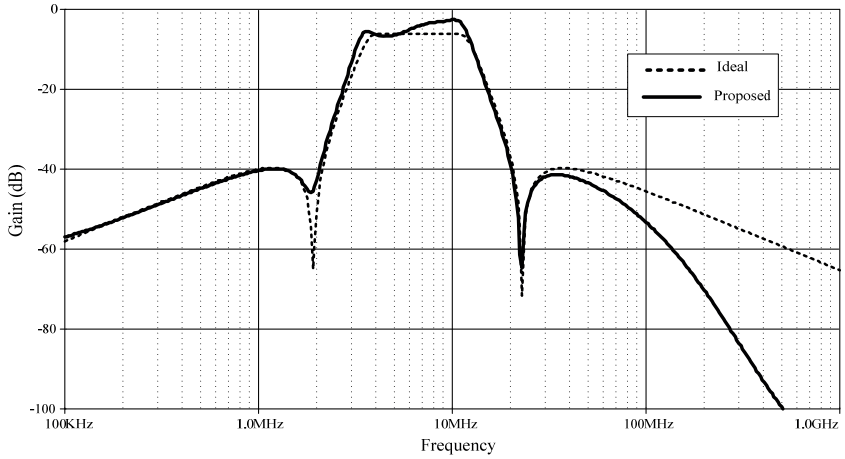


Figure 27. Magnitude responses of the proposed elliptic BPF ($I_B = 20\ \mu$A) and its prototype.

Figure 28 shows the tunability feature of magnitude responses of the proposed elliptic high-order ladder BPF obtained by adjusting I_B [0.02, 0.2, 2, 20, 200] μA. Inspection of Figure 28 shows that the frequency response of the proposed filter can be tuned in the range of 10 kHz to 100 MHz. The input impedance in the pass-band at bias current $I_B = 200\ \mu$A is around 300 Ω, as shown in Figure 29.

The performance of the proposed Chebyshev and elliptic types of BPF performance can be verified by using Monte Carlo analysis as shown in Figures 30 and 31, respectively. The 5% deviation in the oxide thickness (t_{ox}) of the process is assumed and 100 samples are run to verify the center frequency deviation of the proposed two types of BPF. For the 200 μA bias current, it can be seen that both of the proposed BPFs have small deviation around 100 kHz.

Furthermore, a multitone test is also used to confirm the proposed BPFs' performance at bias current = 200 μA. First multitones of frequencies [10–210] MHz are applied at the input of the proposed Chebyshev BPF (20–80 MHz pass band). It can be seen that only dominant tones 30–70 MHz and a small 90 MHz tone are obtained at the output, as shown in Figure 32. Secondly, multitone frequencies [10–210] MHz are applied at the input of the proposed elliptic BPF (30–70 MHz pass band). It can be seen that only dominant tones 30–70

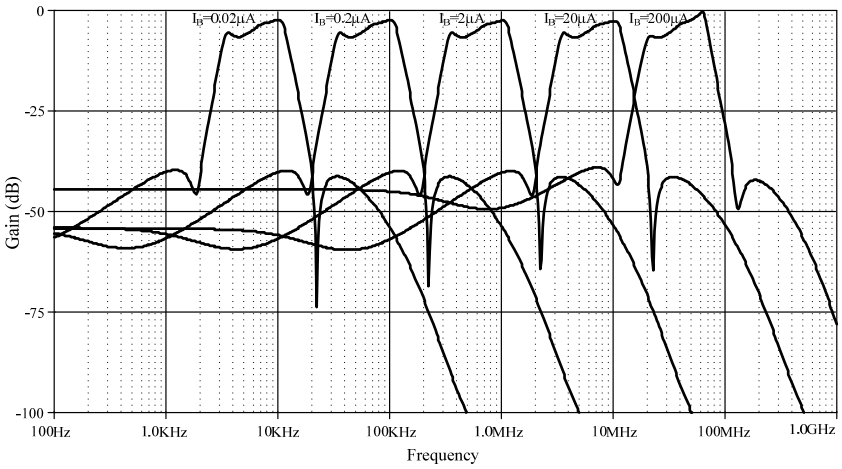


Figure 28. Electronic tunability of the proposed elliptic BPF by adjusting I_B [0.02, 0.2, 2, 20, 200] μA.

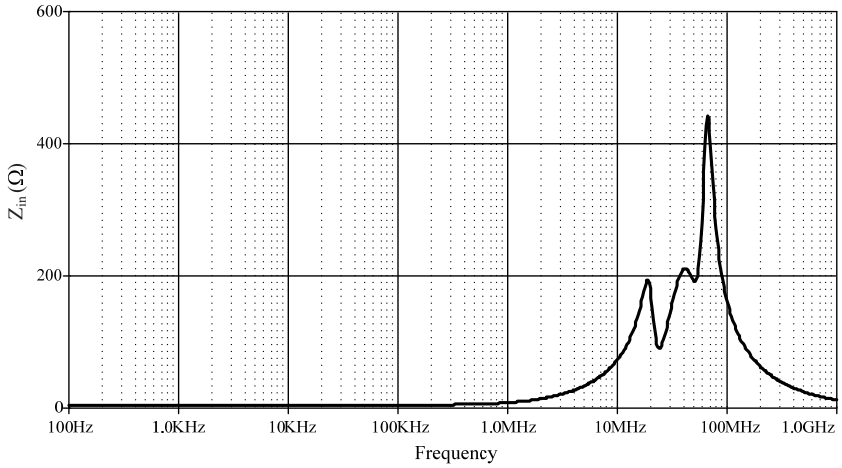


Figure 29. Input impedance of proposed elliptic BPF (I_B = 200 μA).

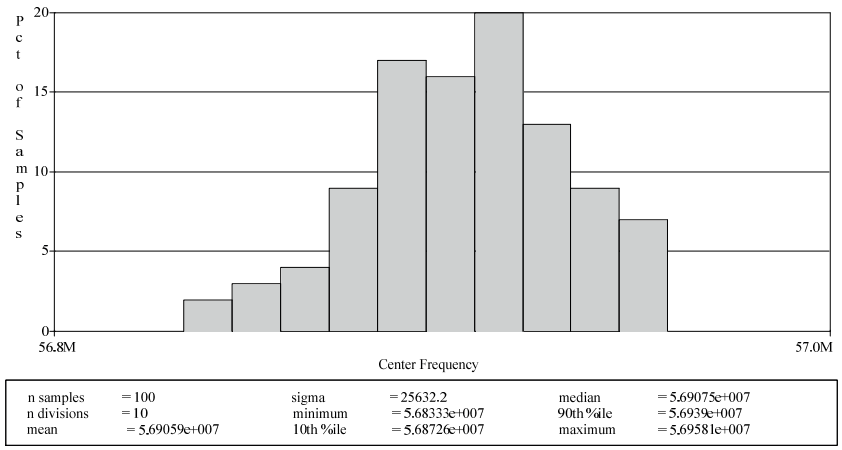


Figure 30. Monte Carlo simulation of the proposed Chebyshev BPF (I_B = 200 μA).

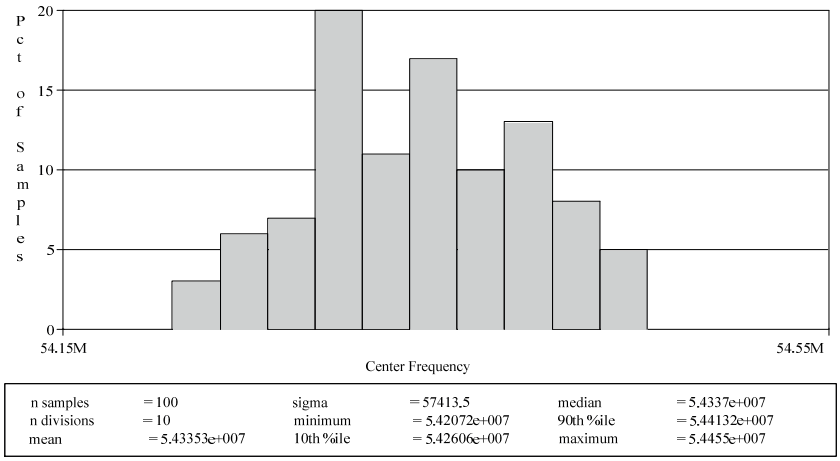


Figure 31. Monte Carlo simulation of the proposed elliptic BPF ($I_B = 200\ \mu$A).

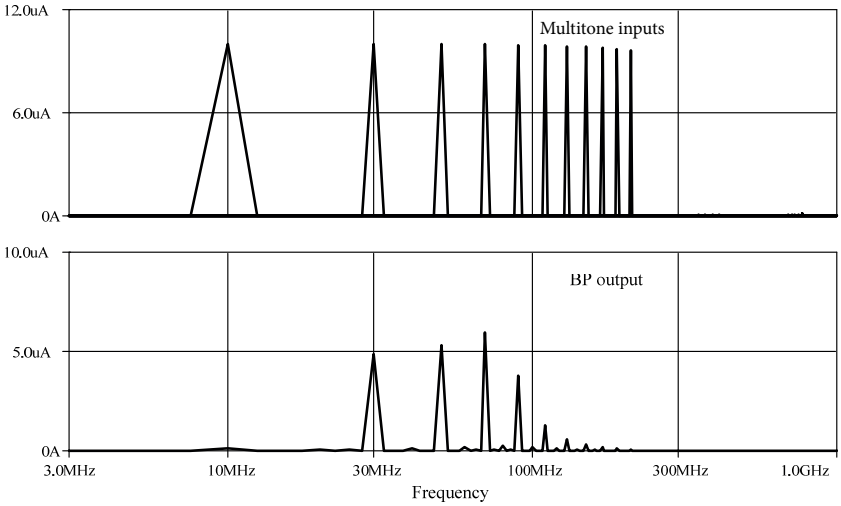


Figure 32. Multitone test of proposed Chebyshev BPF ($I_B = 200\ \mu$A).

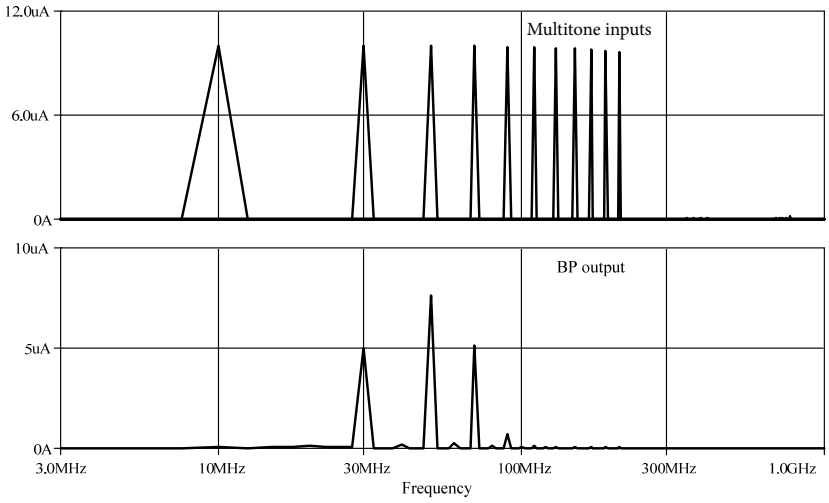


Figure 33. Multitone test of proposed elliptic BPF ($I_B = 200\ \mu$A).

MHz and a very small 90 MHz tone are obtained at the output as shown in Figure 33. These results confirm the functionality of the proposed filters.

Finally, the total harmonic distortion (THD) in the pass-band of the proposed two types of BPFs was measured at bias current = 200 μA. A 50 MHz input signal with variable amplitude is applied to the proposed Chebyshev and elliptic BPFs and the THDs of the outputs are measured; the results are shown in Figures 34 and 35. From Figures 34 and 35 it is obvious that the THDs of both types are below 1.5% within 50 μA_{p-p} of amplitude input.

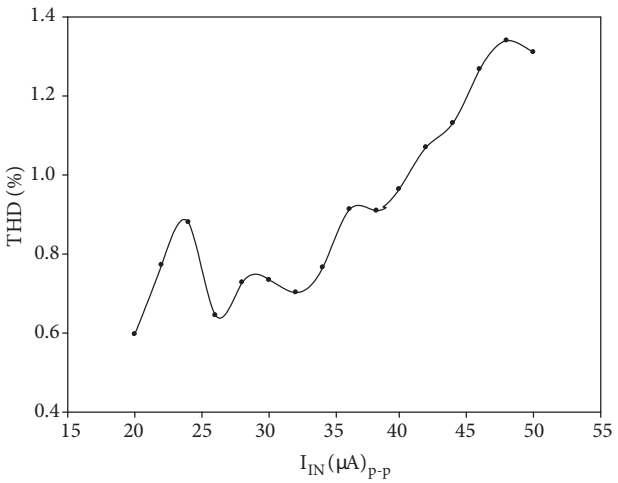


Figure 34. THD at 50 MHz of proposed Chebyshev BPF (I_B = 200 μA).

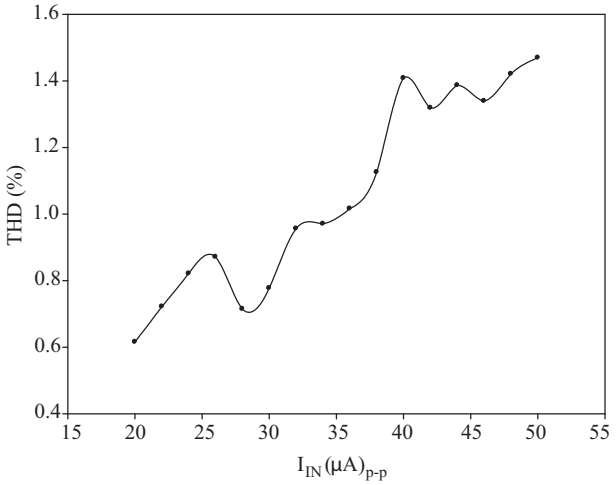


Figure 35. THD at 50 MHz of proposed elliptic BPF (I_B = 200 μA).

6. Conclusion

In this paper electronically tunable current-mode Chebyshev and elliptic ladder BPFs have been presented. Both filters are realized using network transformation of RLC ladder low-pass filter prototypes and the SFG method. Both filters are realized at the transistor level using MOSFETs. This would be attractive for integration. The proposed Chebyshev ladder BPF comprises 2 lossy integrators, 4 lossless integrators, and 6 grounded capacitors. Its frequency response can be tuned between 10 kHz and 100 MHz by adjusting the bias current from 0.02 μA to 200 μA. The proposed elliptic ladder BPF comprises 2 lossy integrators, 5 lossless integrators, and 2 multiple outputs current with different aspect ratio of MOS transistors. The frequency response can be tuned between 10 kHz and 100 MHz by adjusting the bias current from 0.2 μA to 200 μA. The proposed Chebyshev and elliptic BPFs use a 1.5 V DC power supply with dynamic power consumption between 1.34 μW and 13.4 mW and between 2.18 μW and 21.8 mW, respectively, along the tuning of bias currents between 0.02 μA and 200 μA. THDs less than 1.5% at high frequencies are obtained within 50 μA_{p-p} of input range.

References

[1] Huelsman LP. Active and Analog Filter Design. New York, NY, USA: McGraw-Hill, 1993.

[2] Sedra AS, Bracket PO. Filter Theory and Design: Active and Passive. Beaverton, OR, USA: Matrix Publishers, 1978.

[3] Shah NA, Iqbal SZ, Parveen B. Simple first-order multifunction filter. Indian J Pure Appl Phys 2004; 42: 787-866.

[4] Cao LY, Schwartz HM. Oscillation control in non-linear systems using a first-order filter. Int J Control 2002; 75: 1504-1524.

[5] Horng JW, Wu CM, Herencsar N. Three-input-one-output current-mode universal biquadratic filter using one differential difference current conveyor. Indian J Pure Appl Phys 2014; 52: 556-562.

[6] Kaçar F, Yeşil A, Gürkan K. Design and experiment of VDCC-based voltage mode universal filter. Indian J Pure Appl Phys 2015; 53: 341-349.

[7] Ozoguz S, Toker A, Cicekoglu O. First-order allpass sections-based current-mode universal filter using ICCIIs. Electron Lett 2000; 36: 1443-1444.

[8] Ahmad SN, Khan MR, Moinuddin. Operational transconductance amplifier based voltage-mode universal filter. Indian J Pure Appl Phys 2005; 43: 714-719.

[9] Kumngern M, Suwanjan P, Dejhan K. Electronically tunable voltage-mode universal filter with single-input five-output using simple OTAs. Int J Electron 2013; 100: 1118-1133.

[10] Gökçen A, Kilinç S, Çam U. Fully integrated universal biquads using operational transresistance amplifiers with MOS-C realization. Turk J Elec Eng & Comp Sci 2001; 19: 363-372.

[11] Jin J, Wang C. Current-mode universal filter and quadrature oscillator using CDTAs. Current-mode universal filter and quadrature oscillator using CDTAs. Turk J Elec Eng & Comp Sci 2014; 22: 276-286.

[12] Arslan E, Metin B, Cicekoglu O. MOSFET-only mult-function biquad filter. AEU-Int J Electron Commun 2015; 69: 1737-1740.

[13] Arslan E, Metin B, Kuntman H, Cicekoglu O. MOS-only second order current-mode LP/BP filter. Analog Integr Circuits Process 2013; 74: 105-109.

[14] Safari L, Minaei S, Metin B. A low power current controllable single-input three-output current-mode filter using MOS transistors only. AEU-Int J Electron Commun 2014; 68: 1205-1213.

[15] Deliyannis T, Sun Y, Fidler JK. Continuous-Time Active Filter Design. London, UK: CRC Press, 1999.

[16] Schaumann R, Ghausi MS, Laker KR. Design of Analog Filters: Passive, Active RC and Switched Capacitor. Englewood Cliffs, NJ, USA: Prentice Hall, 1995.

[17] Ananda Mohan PV. Current-Mode VLSI Analog Filters: Design and Applications. Boston, MA, USA: Birkhäuser, 2003.

[18] Rollett JM, Nightingale C. Design and economical realisation of a hybrid RC-active lowpass filter for PCM. IEE P-Circ Dev Syst 1981; 128: 201-204.

[19] Allstot DJ, Brodersen RW, Gray PR. Fully-integrated high-order NMOS sampled-data ladder filters. In: IEEE International Solid-State Circuits Conference; 15–17 February 1978; San Francisco, CA, USA. New York, NY, USA: IEEE. pp. 82-83.

[20] Jacobs G, Allstot D, Brodersen R, Gray PR. Design techniques for MOS switched capacitor ladder filters. IEEE T Circuits Syst 1978; 25: 1014-1021.

[21] de Queiroz ACM, Caloba LP, Sanchez-Sinencio E. Signal flow graph OTA-C integrated Filters. In: IEEE International Symposium on Circuits and Systems; 7–9 June 1988; Espoo, Finland. New York, NY, USA: IEEE. pp. 2165-2168.

[22] Tan MA, Schaumann R. Simulating general parameter LC-ladder filters for monolithic realizations with only transconductance elements and grounded capacitors. IEEE T Circuits Syst 1989; 36: 299-307.

[23] Fiez TS, Allstot DJ. CMOS switched-current ladder filters. IEEE J Solid-State Circuit 1990; 25: 1360-1367.

[24] Ng AEJ, Sewell JI. Ladder decompositions for wideband SI filter applications. IEE P-Circ Dev Syst 1998; 145: 306-313.

[25] Martin K. Improved circuits for the realization of switched-capacitor filters. IEEE T Circuits Syst 1980; 27: 237-244.

[26] Lee SS, Allstot DJ. CMOS continuous-time current-mode filters for high-frequency applications. IEEE J Solid-State Circuit 1993; 28: 323-329.

[27] Wu J, El-Masry E. Current-mode ladder filters using multiple output current conveyers. IEE P-Circ Dev Syst 1996; 143: 218-222.

[28] Sun Y, Fidler JK. Structure generation and design of multiple loop feedback OTA-grounded capacitor filters. IEEE T Circuits Syst 1997; 44: 1-11.

[29] Chang CM, Al-Hashimi BM. Analytical synthesis of current-mode high-order OTA-C filters. IEEE T Circuits Syst 2003; 50: 1188-1192.

[30] Prommee P, Angkeaw K, Somdunyakanok M, Dejhan K. CMOS-based near zero-offset multiple inputs max–min circuits and its applications. Analog Integr Circuits Process 2009; 61: 93-105.