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An inductorless wideband LNA with a new noise canceling technique

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Abstract: An inductorless wideband low-noise amplifier (LNA) employing a new noise canceling technique for multi-standard applications is presented. The main amplifier has a cascode common gate structure, which provides good input impedance matching and isolation. The proposed noise canceling technique not only improves the noise figure and power gain but also embeds a g_m-boosting technique in itself, which reduces the power consumption of the main amplifier. Using current-steering and current-reuse techniques in the noise canceling branch makes the design realizable and low power. The proposed LNA is simulated and optimized in 0.13 μm CMOS technology. The LNA achieves a noise figure of 2.8–3.4 dB, power gain of 19.2 dB, and input impedance matching better than –10.5 dB over bandwidth of 0.04–4.6 GHz. It consumes only 8.5 mW from 1.2 V supply voltage, which makes it a low power LNA.

Key words: Current reuse technique, G_m-boosting technique, low power LNA, noise canceling technique

1. Introduction

Fast growth of wireless technology has led to the appearance of various new communication standards that accommodate different applications at distinctive frequency bands such as terrestrial digital (450–850 MHz) video broadcasting, satellite communications (950–2150 MHz), global positioning systems (GPS) at 1.2 GHz and 1.575 GHz, and cellular radios (850–1900 MHz) [1,2]. Accordingly, software-defined radio (SDR) and multiband/multistandard radio receivers are considered as future radios. One of the main blocks of these receivers is the low-noise amplifier (LNA) at the front-end, which has to provide high gain while introducing the least noise. One approach to implement multiband receivers is to utilize multiple narrowband front-ends, which is in contrast to a single wideband front-end, the alternative approach, in terms of area, power, and cost. Besides this, single-ended input LNAs are preferred to save I/O pins and because antennas and RF filters usually produce single-ended signals [3].

Among different topologies for realization of wideband LNAs, the ones with noise canceling technique are very popular as the trade-off between noise figure and input impedance matching is alleviated [4–6]. The main structures proposed for this are shunt resistive feedback and common gate LNAs. In the former, the resistive feedback reduces the input impedance providing input matching, while in the latter, the wideband transconductance of the common gate amplifier is used for input matching.

The main idea of the noise canceling technique is to use two nodes with in-phase signal voltages and out-of-phase noise voltages or vice versa and add them at the output by the use of auxiliary amplifier(s) in such a way that noise is canceled but signal is amplified. Whereas the shunt resistive feedback and CG LNAs are

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not the only implementations of the noise canceling technique, a new noise canceling technique based on the cascode common gate structure is proposed. The proposed LNA achieves a low noise figure, high gain, and low power consumption while other parameters are kept within acceptable ranges.

The paper is organized as follows: in Section 2, the proposed wideband LNA is presented. Explaining the new noise canceling technique, a detailed analysis of gain, input impedance, and noise figure is addressed. In Section 3, the designed LNA and simulation results are presented. Finally, conclusions are drawn in Section 4.

2. The proposed LNA

2.1. The proposed noise canceling technique

Figure 1a shows a conventional cascode common gate LNA. The gain transistor, M1, develops the LNA's gain while the cascode transistor, M_2, improves its output impedance, bandwidth, and particularly its isolation. M_1's dominant noise contributor, its channel thermal noise, is modeled by a noise current source connected between its drain and source nodes. Investigating the signal and noise voltage polarities on the source and drain nodes of M_1, it is observed that the signal voltages are in-phase while the noise ones show 180° phase shift. If the amplified source voltage of M_1 is turned back to M_2's gate with 180° phase shift, M_2's gate-source experiences a canceled noise voltage but amplified signal one, which is the main idea of the proposed LNA shown in Figure 1b. Consequently, M_1's noise is canceled at the output.

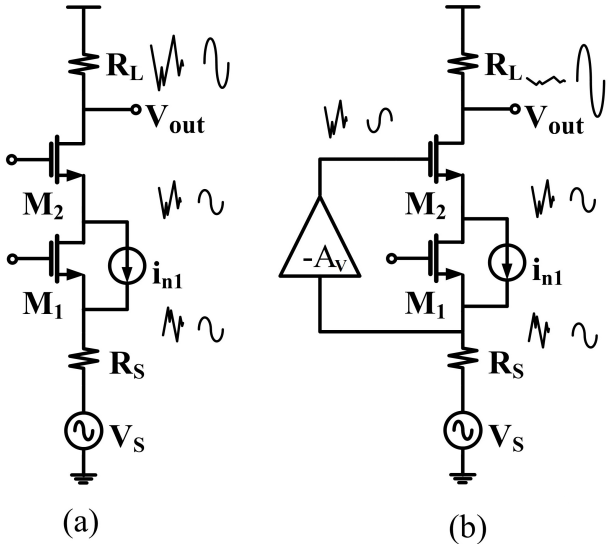

Figure 1. (a) Conventional cascode common gate LNA, (b) proposed LNA with noise canceling technique.

Considering the LNA shown in Figure 1b, the noise canceling condition is found to be:

$$v_{s1,n} \cdot A_v = v_{d1,n}, \tag{1}$$

where $v_{s1,n}$ and $v_{d1,n}$ are M_1's source and drain voltages, respectively. Because of the negative feedback loop, increasing gain A_v causes $v_{s1,n}$ to decrease but $v_{d1,n}$ to increase. Then, for complete noise canceling, the gain A_v has to be chosen very high, which is not practical. However, a moderate value of A_v still leads to significant noise cancelation.

2.2. Gain

Implementing the gain stage $-A_v$ by a common source structure, as shown in Figure 2a, the voltage gain of the LNA, G_v, at frequencies well below f_T is obtained by considering its small signal equivalent circuit shown in Figure 2b:

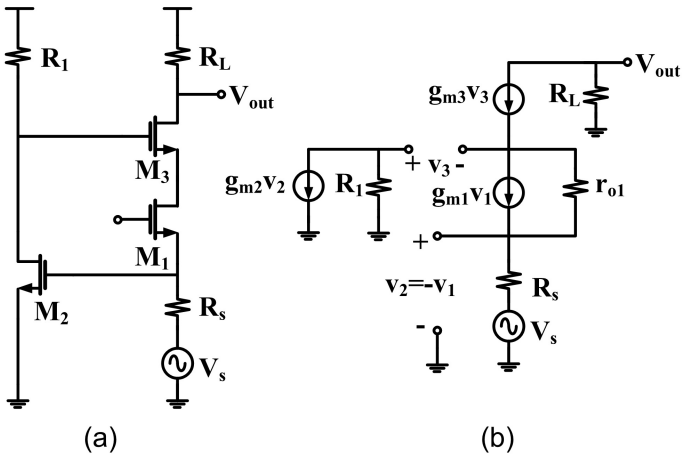

Figure 2. (a) The proposed LNA, (b) its small signal equivalent circuit.

$$\begin{aligned} G_v &= \frac{v_{out}}{v_s} = \frac{g_{m3}.(1+g_{m1}.r_{o1}+g_{m2}.R_1)}{1+g_{m3}.(r_{o1}+R_s.(1+g_{m1}.r_{o1}+g_{m2}.R_1))} \times R_L \\ &\approx \frac{1}{r_{o1}/(1+g_{m1}.r_{o1}+g_{m2}.R_1)+R_s} \times R_L \end{aligned} . \tag{2}$$

It is observed that increasing $g_{m2}.R_1$ improves G_v.

Replacing the input source with the Norton equivalent, the input impedance is calculated as follows:

$$Z_{in} = \frac{1}{g_{m1}+g_{m2}.(R_1/r_{o1})+1/r_{o1}} \approx \frac{1}{g_{m1}+g_{m2}.(R_1/r_{o1})}, \tag{3}$$

where it is assumed that $r_{o1} >> 1$. Appearance of g_{m2} in the denominator of Z_{in} denotes that the proposed LNA embeds the g_m-boosting technique in itself, contributing to its low power design.

2.3. Noise analysis

The noise equivalent circuit of the LNA is shown in Figure 3. Considering the channel thermal noise of M_1 as its dominant noise contributor and using a finger digitized gate structure, the noise figure of the LNA is found to be approximately:

$$\begin{aligned} F &= 1+F_{M_1}+F_{M_2}+F_{R_2}+F_{R_L} = 1+(\frac{r_{o1}}{1+g_{m1}.r_{o1}+g_{m2}.R_1})^2.\frac{\gamma.g_{m1}}{R_s}+(\frac{R_1}{1+g_{m1}.r_{o1}+g_{m2}.R_1})^2.\frac{\gamma.g_{m2}}{R_s} \\ &+(\frac{R_1}{1+g_{m1}.r_{o1}+g_{m2}.R_1})^2.\frac{\gamma}{R_s.R_L}+\frac{(1+g_{m3}.(r_{o1}+R_s.[1+g_{m1}.r_{o1}+g_{m2}.R_1]))^2}{g_{m3}^2.R_L.R_s.(1+g_{m1}.r_{o1}+g_{m2}.R_1)^2} \end{aligned} . \tag{4}$$

It is observed that the appearance of the $g_{m2}.R_1$ term in the denominator of F_{M1} reduces M_1's noise contribution at the output. Although further increase of $g_{m2}.R_1$ reduces F_{M1} more, M_2's noise contribution increases, as the F_{M2} term shows. Then there is a tradeoff between F_{M1} and F_{M2}, which can be removed by proper selection of R_1 and increasing g_{m2}, but this leads to more power consumption of the LNA. In addition,

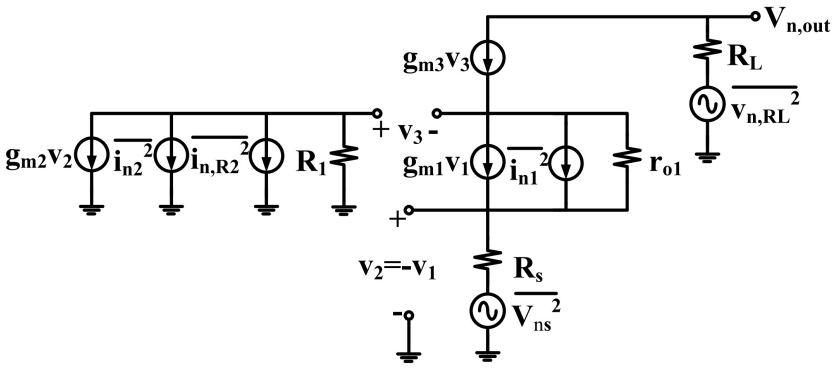

Figure 3. The proposed LNAs noise equivalent circuit.

increasing g_{m1} can also contribute to further reduction of F_{M1} and F_{M2}. Even though increasing g_{m1} and g_{m2} improves the circuit noise performance, according to Eq. (3), the input impedance is degraded and consequently g_{m1} and g_{m2} cannot be increased arbitrarily.

In order to gain insight into circuit design and proper selection of different parameters, it is helpful to draw the contour curves of S_{11} and NF (NF = 10log (F)) with respect to g_{m2} and R_1 and address the effect of g_{m1} variation on them. Furthermore, these plots help to better understand the interaction between S_{11} and NF.

In Figure 4 the contour curves of S_{11} and NF for two values of g_{m1} (g_{m1} = 5 mA/V and g_{m1} = 25 mA/V) were plotted. The goal is to address the effect of g_{m1} increase. As it is inferred, the turn-around point of contours moves roughly on the line $R_1 = g_{m2}$ towards the origin of the coordinate system as g_{m1} increases. The contour curves of S_{11} move faster than those of NF, which means that g_{m1} variations affect S_{11} more than NF. This causes good input impedance matching to be obtained for larger values of NF. On the other hand, large g_{m1} is provided by high bias current of transistor M_1, which restricts the design to the selection of a low value for the load resistor, and then the gain of the circuit degrades. Moreover, choosing g_{m1} very low causes the desired input impedance matching and low NF to be obtained for high values of g_{m2} and R_1 such that the former increases the power consumption and the latter makes the circuit design challenging from the bias point of view. Thus, selecting a mean value for g_{m1} (10 mA/V $< g_{m1} <$ 15 mA/V) not only facilitates the circuit design but also leads to proper circuit performance.

2.4. Gain stage ($-A_v$) design

Low noise design of the LNA demands large R_1 and g_{m2}. High g_{m2} corresponds to high current consumption. Choosing large values for I_2 and R_1 leads to a large voltage drop on R_1, and consequently the LNA needs a high supply voltage for proper performance. Besides this, high current degrades the output resistance of the noise canceling branch transistor and makes it difficult to use a large R_1. Using a cascode structure along with a current steering technique can alleviate these problems and makes the use of large R_1 and lower supply voltage possible. Furthermore, adding a current reuse technique to the current steering one reduces the power consumption of the LNA significantly.

3. LNA design and simulation

Figure 5 shows the complete schematic of the proposed LNA. A single V_{dd} = 1.2 V supply voltage and MIM capacitors for AC-coupling were used. A buffer stage was used at the output of the LNA for impedance matching.

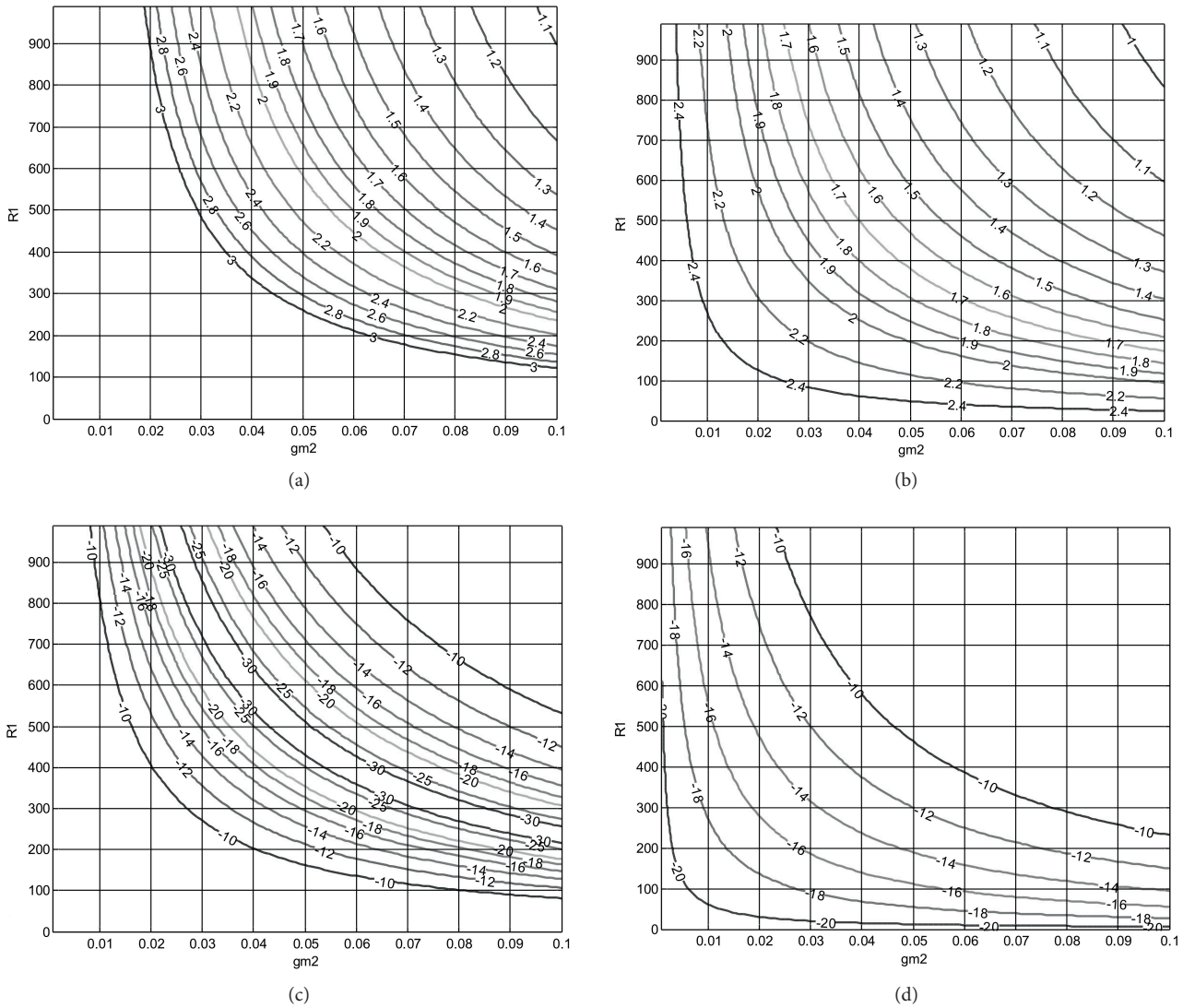

Figure 4. (a) The contour curves of NF for $g_{m1} = 5$ mA/V; (b) the contour curves of NF for $g_{m1} = 25$ mA/V ($r_{o1} = 1500\ \Omega$, $g_{m3} = 10$ mA/V, $R_S = 50\ \Omega$, $R_L = 550\ \Omega$, $\gamma = 2/3$); (c) the contour curves of S_{11} for $g_{m1} = 5$ mA/V; (d) the contour curves of S_{11} for $g_{m1} = 25$ mA/V ($r_{o1} = 1500\ \Omega$, $g_{m3} = 10$ mA/V, $R_S = 50\ \Omega$, $R_L = 550\ \Omega$, $\gamma = 2/3$).

The circuit was simulated in TSMC RF CMOS 0.13 μm with ADS. Using RF transistors in the circuit implementation, the minimum length of channel ($l_r = 0.13\ \mu$m) and finger width of 2 μm are chosen for gate resistance thermal noise reduction and bandwidth enhancement. Using genetic algorithm optimization tools in ADS, the LNA was optimized simultaneously for the least NF and S11 over the –3 dB bandwidth while keeping other parameter values in an acceptable range. As Figure 6 shows, the highest gain of LNA is 19.2 dB in the bandwidth of 0.04–4.6 GHz and the input impedance matching, S_{11}, is lower than –10 dB (Figure 7). If the noise performance of the proposed LNA is compared with the one without noise canceling (Figure 8), the effectiveness of the new noise canceling technique is proved and the noise figure reaches a minimum of 2.8 dB. Due to the cascode structure, isolation of lower than –50 dB (Figure 7) is observed, which will be about 5 to 10 dB worse but still very high in practice. The simulated value of IIP3 at 1.9 GHz is –13 dBm, as shown in

Figure 9, and –8 dBm and –14 dBm at 0.5 GHz and 4.5 GHz, respectively. In the Table, the simulated results are compared with previously reported ones. The proposed LNA achieves high gain and a very low noise figure over a wide bandwidth while the power consumption is just 8.5 mW.

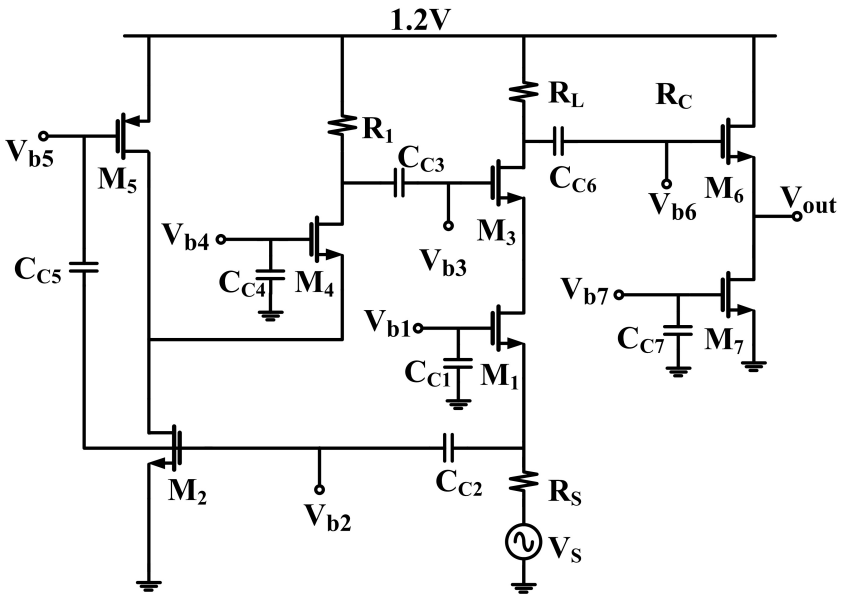

Figure 5. The complete schematic of the proposed LNA.

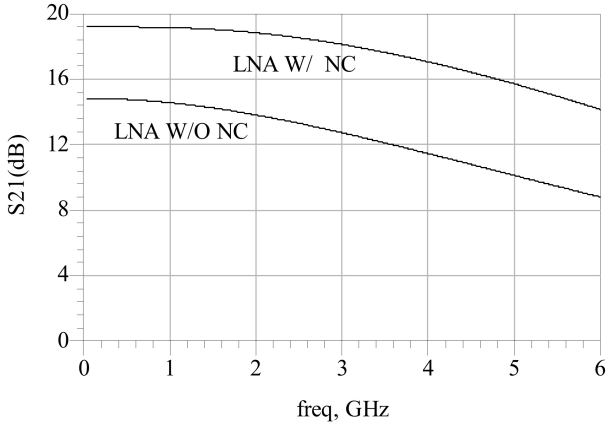

Figure 6. Simulated S_{21} of the proposed LNA with and without applying noise canceling technique.

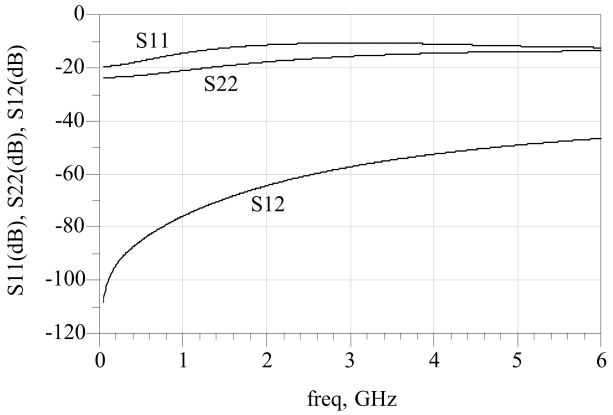

Figure 7. Simulated S_{11}, S_{22}, and S_{12} of the proposed LNA with applying noise canceling technique.

4. Conclusion

Based on the cascode common gate structure, a new noise canceling technique for multistandard wideband LNA design was presented in this paper. The proposed LNA was analyzed in detail, which shows significant improvement of noise figure and gain. Simulated in 0.13 μm CMOS technology, the LNA achieves the noise figure of 2.8–3.4 dB, power gain of 19.2 dB, and input impedance matching better than –10.5 dB over bandwidth of 0.04–4.6 GHz. The IIP3 at 1.9 GHz is –13 dBm and the LNA consumes only 8.5 mW, which makes it a low power LNA.

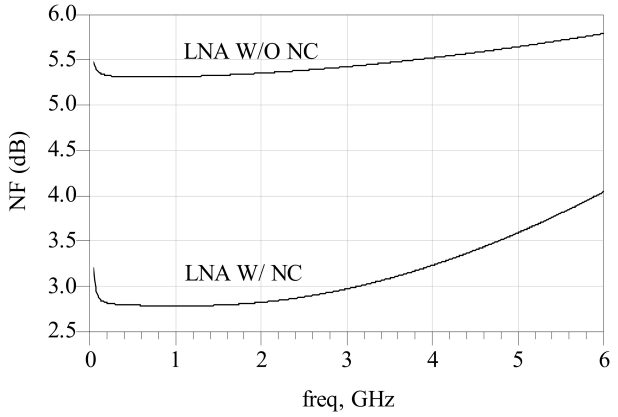

Figure 8. Simulated NF of the proposed LNA with and without applying noise canceling technique.

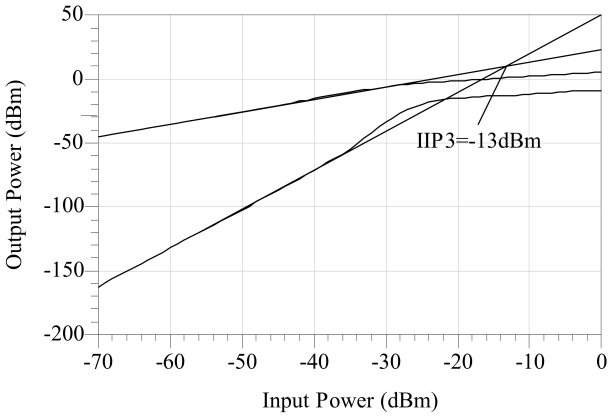

Figure 9. Simulated IIP3 at 1.9 GHz.

Table. Performance summary.

Reference	Technology	–3dB-BW	Gain	NF	S11	IIP3	Supply	Power
	(CMOS)	(GHz)	(dB)	(dB)	(dB)	(dBm)	voltage (V)	(mW)
[2]	90 nm	0.002–2.3	21	1.4	< -10	–1.5	1.8	18
[3]	0.18 μm	0.004–1.2	16.4	2.1–3.4	< -10	0	1.8	14.4
[4]	0.13 μm	0.8–2	14.5	2.6	< -8.5	+16	1.5	17.4
[5]	0.18 μm	1.2–11.9	9.7	4.5–5.1	< -11	–6.2	1.8	20
[6]	0.13 μm	0.2–3.8	19 VG	2.8–3.4	< -9	–4.2	1	5.7
[7]	65 nm	0.2–5.2	13–15.6	< 3.5	< -10	> 0	1.2	21
[8]	0.25 μm	0.002–1.6	13.7 VG	2.4	< -8	0	2.5	35
This work	0.13 μm	0.04–4.6	19.2	2.8–3.4	< -10.5	–13	1.2	8.5

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