Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2017) 25: 717 – 734

doi:10.3906/elk-1506-173

# Modeling hybrid modulation strategy with nearest leveled vector switching pattern in space vector control technique for multilevel inverters

**Rohith Balaji JONNALA*, Sai Babu CHOPPAVARAPU**
Department of Electrical and Electronics Engineering, University College of Engineering Kakinada, Jawaharlal Nehru Technological University Kakinada, Kakinada, Andhra Pradesh, India

**Received:** 19.06.2015 • **Accepted/Published Online:** 19.02.2016 • **Final Version:** 10.04.2017

**Abstract:** The multilevel inverter's impact in the area of power electronics is augmented because of its nimble nature. This paper presents an efficient switching pattern for multilevel inverters using the nearest leveled vector (NLV) strategy through a space vector control (SVC) technique. The objective is to reduce the total harmonic distortions by generating an optimal switching sequence with the newly introduced NLV-SVC for multilevel inverters. The proposed NLV modulation is applied for an asymmetrical multilevel inverter, which has a high number of levels with reduced switch count, sources, and lower switching losses. The effectiveness of the proposed method is verified on a 27-level 3-cell asymmetrical multilevel inverter. The efficacy of the proposed method in terms of total harmonic distortions is compared with the existing nearest vector control (NVC) modulation strategy. Implementation and experimental verification of the proposed NLV-SVC modulation strategy for an asymmetrical cascaded H-bridge multilevel inverter is presented for real-time validation with the comparison of the NVC modulation strategy.

**Key words:** Asymmetrical multilevel inverter, space vector control, nearest leveled vector modulation, switching pattern, better total harmonic distortion

## 1. Introduction

The escalation of qualitative power requirements raises opportunities for the arrival of many contemporary power converter topologies, which are capable of providing all needed power. Either to improve the quality of the signal or to reduce energy wastage, adequate power electronic technologies and their associated control strategies are necessary.

Nowadays multilevel inverters are becoming popular in various power applications as they are capable of high-power applications using advanced medium-power semiconductor devices [1]. The nature of multilevel inverter and proper modulation strategies are essential to find an improvement in nominal power in the converter and output signal quality [2,3]. The load-side voltage waveform with effective modulation improves its quality with the increase in the number of levels and in turn reduces the total harmonic distortion (THD) [3,4] at the output of the converter. A hybrid asymmetrical multilevel inverter that gives higher voltage levels than the conventional asymmetrical multilevel inverter topologies is considered in this paper.

Multilevel converter modulation and control strategies have been gaining more attention from researchers over the last few years. The modulation strategies used for multilevel inverters can be classified based on switching frequency as shown in Figure 1 [5,6]. Among all control strategies from the classification, a commonly

*Correspondence: rohithbalajijonnala@yahoo.com

accepted strategy for industrial application is standard carrier-based sinusoidal pulse width modulation that uses the phase-shifting strategy to reduce the harmonics in the output voltage signal. The other alternative captivating strategy is space vector modulation, which has been used in multilevel inverters with low switching frequency. One of the representatives of this family is the space vector control (SVC); in this modulation, the output voltage signal is generated like a staircase waveform [7]. Along with the progress of multilevel inverter topologies, there is a need to extend the traditional modulation techniques for reliable operation. Though huge numbers of multilevel inverter topologies are available, the modulation strategies are limited and hence there is a need to enhance traditional modulation techniques for reliable operation of recently developed converters [8,9].

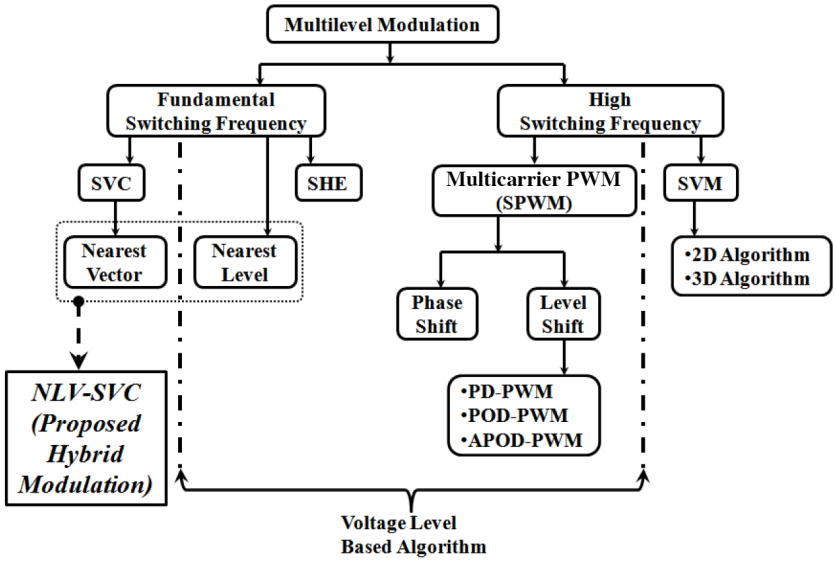


**Figure 1.** Classification of multilevel inverter's modulation strategies.

The two main categories of modulation strategies are space vector-oriented and level-based modulation techniques. Both these strategies have their own forte in different areas of applications. In open loop operation, there is no such contest between these vector-oriented and level-based strategies. In closed loop operation, the major control methodologies are based on vectors or samples for the optimal control actions. Among the two control methodologies (vector or sample), vector-based modulation techniques such as SVM and SVC have more desirability in closed loop operations. Though SVM is widely used and has reached a certain state of influence in multilevel applications, it is very difficult to implement and design for converters with higher numbers of levels due to the complexity in computation of switching angles. In this operating situation, other low switching frequency-related strategies are more convenient, such as multilevel SVC. It has the advantage of a larger number of voltage vectors generated by a converter with respect to different levels by approximating the reference signal to the nearest generatable space vector. This SVC or nearest vector control (NVC) principle gives the output with fundamental switching frequency and hence low switching losses.

### 1.1. Nearest vector control

In this strategy, the voltage vectors are simply selected by approximating the reference signal to the adjacent vectors in the operating zone of a hexagonal space without any operational conditions like other strategies. Therefore, this strategy is specified as the closest vector control method in place of the closest vector modulation

strategy [3,5–7]. The operating principle of NVC is shown in Figure 2, where all the selected states of a control vector of the space vector strategy for an 11-level converter with overmodulated reference are illustrated. The overmodulated SVM strategy is used for general practice, in view of getting the maximum effective output voltage of the converter. The selection of voltage vectors changes with the change in modulation index. Each and every dot, as shown in Figure 2, is one of the feasible voltage control vectors generated by the inverter, and all of these dots are covered by a hexagon, which represents the boundary of the area where there is a closest available voltage vector [8–10]. The dashed line shown in Figure 2 is the control voltage reference trajectory and it passes through the d-q plane. Hence, when the required signal come into any hexagon, the respective control vectors are selected according to the illustrative logic in Figure 2 of the NVC strategy.

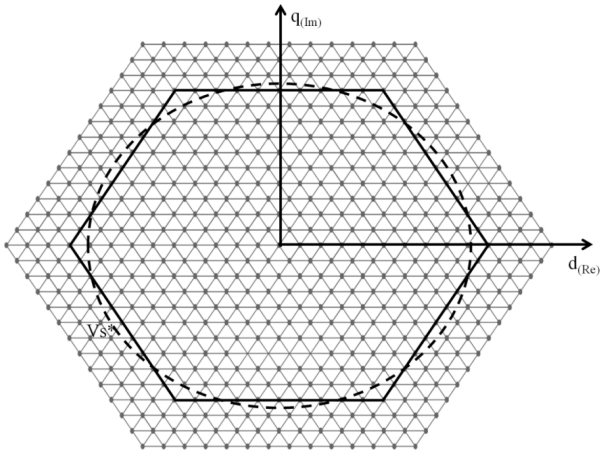


**Figure 2.** Operating principle of NVC.

Some researchers concentrated on the NVC strategy in view of cell-wise modifications of modulation in asymmetrical multilevel inverters; some modifications were made with the level of the reference signal and this was called nearest level control (NLC) [11]. This NLC is not in the space vector-oriented strategy, but the quality of the output signal and the straightforwardness of the control strategy are better than NVC, because of approximate reference signal generation in the output side. In vector-based modulations, the fundamental selection of the nearest control vector gives a better reduction in the commutations number. Those reduced commutations reflect the reduction in switching losses. This strategy does not avoid low-order harmonic distortions because of its operating nature of strategy. The NVC has a predetermined operating principle for a fixed load condition and is very easy to implement. However, the computation of the nearest vectors for the required load is not simple in nature because this algorithm is needed to find the closest vector in numerical form with NVC logic for the required conditions. In view of the application point of reference, vector-oriented and level-based modulations have their own priorities in different areas of applications. Major control methodologies are based on vector-oriented strategies for the desired control actions in closed loop operation [6,11,12].

A new hybrid strategy for control operation based on the space vector orientation is presented in this paper. This modulation strategy operates at a very low switching frequency and avoids problems of the space vector-based NVC strategy to get high-quality signal on the load side. The working principle and features of the proposed strategy are discussed in Section 2.

## 2. Proposed modulation strategy

Various multilevel converter modulation strategies have been introduced over the years, including a comprehensive review of recent development in modulation techniques [1,3,12], and different variations on NVC strategies were discussed in Section 1. The proposed modulation strategy is a combination of an organized approach with NVC and a rounded reference signal to improve the quality of signal in the output side of a multilevel inverter with vector-based approach.

The basic strategy of space vector control is united with the space vectors of the hexagon and voltage vector of different levels. Figure 3 shows the voltage vectors at different levels of space vector regions and zones of each level, where blue and green circles represent the overmodulation zones of 3- and 2-level space vector trajectories, respectively. The black circle indicates the linear modulated reference signal. If the required signal is overmodulated, the selected voltage vectors are the outermost vectors of the 3-level hexagon. Otherwise, the reference signal is within the black and green circles, i.e. linearly modulated, and here the selected voltage vectors are adjacent to the required signal [7].

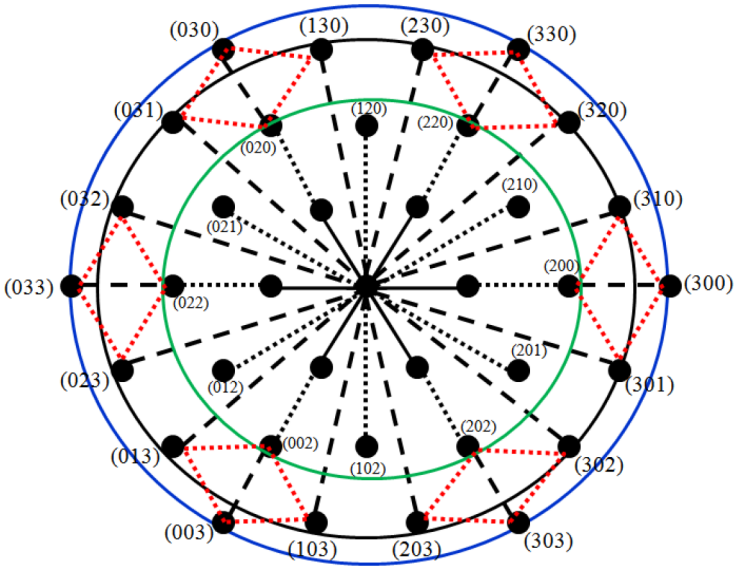


**Figure 3.** Three-level voltage space vectors.

The output signal generated by the selected voltage vectors of SVC strategy is not tracking the required signal, neither in overmodulated nor in linear modulated zones. If the output does not follow the required reference signal, the quality of the system is impaired. To avoid this problem, a few alternative methodologies are suggested. One of the popular alternatives is just to follow the level of the reference to select the vectors [11], but this violates the space vector orientation. Another alternative is shifting the reference signal by using a ceiling or floor function [13,14] at each sector's duration. In the approach with ceiling or floor function the approximation error is very high with unfair selection for a particular sector like the ith sector shown in Figure 4.

In Figure 4, a part of a 3-level space vector hexagon is illustrated. The levels j and j+1 are indicated with green and light green dashed lines separated by a sectional blue line. The reference (Vref) signal is above the blue line in the (i+1)th and successive sectors. At this position of reference, if the ceiling function is used to select the adjacent vector, the approximation error is low and for the floor function it will be very high. In the

ith sector, the three yellow dots indicate the different level positions of the reference with respect to a sectional line and they are represented as Case A/B/C. In Case A, B, and C the reference signal is above, in, and below the sectional line, and either of the alternative functions gives the wrong selection of vectors. To avoid all these constraints, the nearest leveled vector modulations approach and its methodology to select a vector and the pattern of switching states are clearly discussed in Section 3.

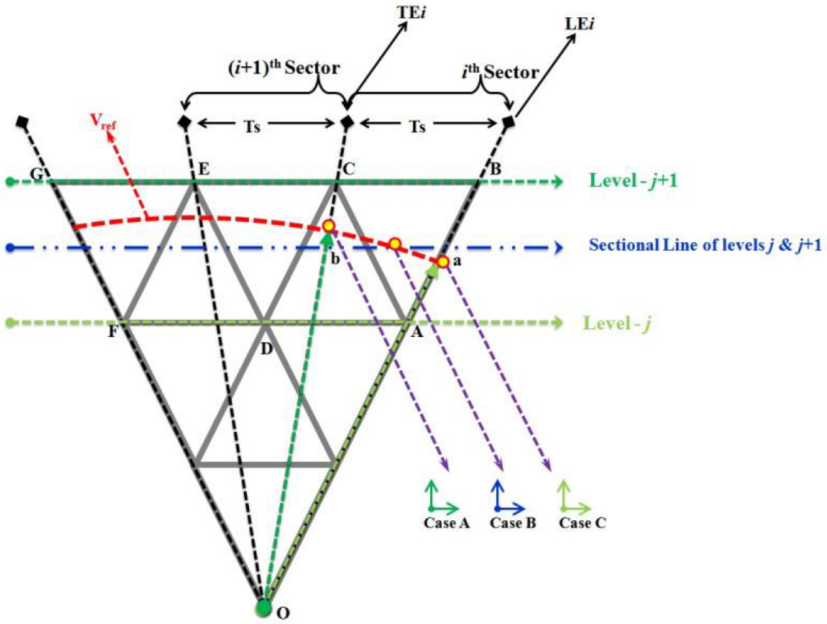


**Figure 4.** Selection of voltage space vectors by the strategies.

## 3. Methodology for proposed strategy

For a particular closed loop application like machine control, NVC is the best strategy to control the load for a required performance. The NVC strategy has less output power quality than level-based strategies and those have more complexity to implement in closed loop systems than NVC. An algorithm is proposed to upgrade the NVC strategy with rounded reference signal operating conditions for a better quality in output. The proposed modulation is a combinational one or a hybrid modulation called nearest leveled vector (NLV)-SVC. This proposed hybrid strategy takes all of the operating conditions of the level-oriented approach with better power quality in vector-based operating conditions.

The flow diagram of a control algorithm is shown in Figure 5. Vref shown in Figure 4 is the trajectory component of the required space vectors in the dq plane, and $V_v$ and $V_h$ are the dq components of Vref. In this strategy, the approach for the selection of voltage vector is based on the value of $V_h$ with the reference position of either in the leading edge (LE$i$) or trail edge (TE$i$) of each of the sectors. In this approach the rounded function is used to choose the future voltage vector ($V_F$).

Vref = $f$($V_v$ and $V_h$):

$V_v$ = (1/3) × (2Va – Vb – Vc), i.e. the d component of Vref.

$V_h$ = (1/sqrt(3)) × (Vb – Vc), i.e. the q component of Vref.

Here Va, Vb, and Vc are the abc components of Vref.

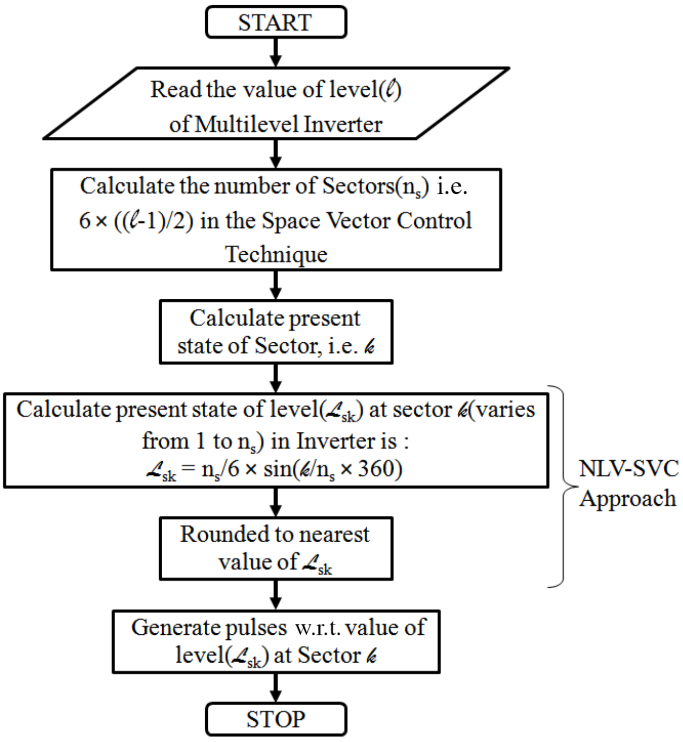


**Figure 5.** Control algorithm for nearest leveled vector technique.

$L_{sk} = f_{round}\ (V_h)$, i.e. the rounded value of $V_h$ at the preferred edge of the sector. This $L_{sk}$ contains the values of the $j-1, j$, or $j+1$ levels, and that level of the required signal is to be generated in the output side. A progressive path with the selected level decides the future voltage vector. As shown in Figure 4, the present sector is the $i$th and the voltage vector is A, and then the proposed strategy selects the $j+1$ level and the path moves from A to C; otherwise, it is the $j$ level and then the path moves towards D. A clear explanation and digital implementation of the NLV-SVC strategy is as follows.

We primarily collect/read the value of level (l), i.e. l = 3N, corresponding to the number of sectors ($n_s$), with the help of a space voltage vector diagram, i.e. $n_s = 6 \times ((l-1)/2)$. The logic circuit or processor has the data of parameters $n_s$ and l for a required operation, and with these data the present state of sector k (LEk/TEk) is calculated by using the system clock; k varies from 1 to $n_s$. This k value depends on the output frequency ($f_o$) and $n_s$, i.e. $n_s/f_o$ gives the value of the time period of the sector and then the processor will get the k value from 1 to $n_s$ by comparing the system clock and time period of the sector. With all the computed data from the start pulse of the clock, it is possible to calculate the present state of the level ($L_{sk}$) of the inverter. The required level of the inverter at sector k, i.e. $L_{sk} = n_s/6 \times \sin((k/n_s) \times 360)$, is useful to generate appropriate pulses. This computational stage is the key operation of the NLV-SVC.

The level is approximated in this strategy with respect to a particular sector, i.e. calculating the p.u. value of reference sinusoidal magnitude with the reference of the clock, but it was segmented by sectors. Then rounding the $L_{sk}$ value at a particular sector to the nearest value, all the rounded $L_{sk}$ values are stored in the switching state table with respect to sector k (LEk/TEk). The switching state table data are never changed until the resetting or shutdown of the system process. The stored rounded $L_{sk}$ values are transferred to the pulse generator with respect to sector k(LEk/TEk). The pulses are generated by the NLV-SVC logic and transferred to an asymmetrical cascaded H-bridge multilevel inverter to get a better output. This operation

repeats with the help of the switching state table (having rounded $L_{sk}$ values) until shutdown or resetting of the system. The selected voltage vectors for LEk or TEk are same, because the trail edge of one sector is the leading edge of a successive sector. The 27-level voltage space vectors are shown in Figure 6 in the dq plane and the red colored dots are the selected voltage vectors by NLV-SVC approach. The switching state pattern of the proposed modulation is shown in Figure 7.

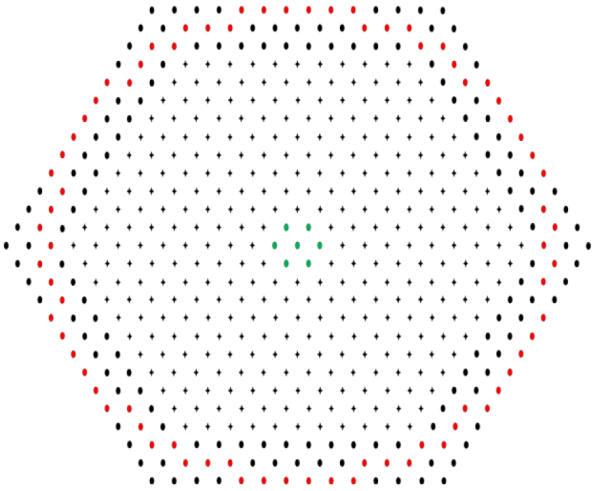

**Figure 6.** The 27-level selected voltage space vectors by the proposed NLV-SVC.

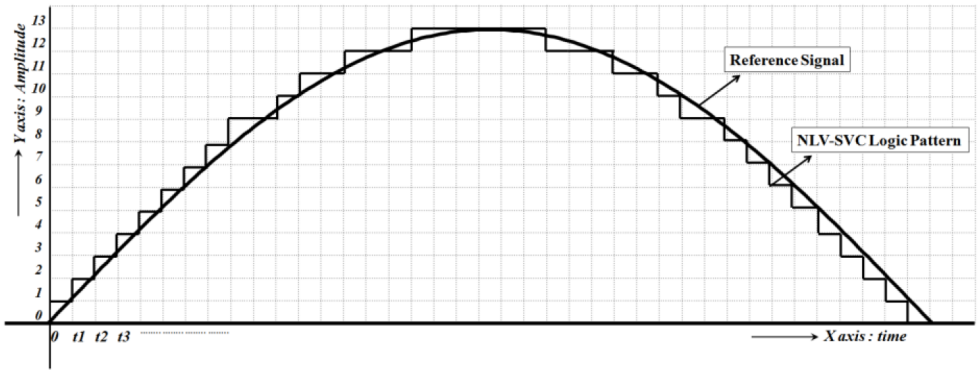


**Figure 7.** NLV-SVC switching state pattern.

Simulation and experimental implementation of the proposed NLV-SVC modulation strategy to a 3-cell asymmetrical multilevel inverter [9,10,15–17] is compared with the NVC modulated results and discussed in Section 4. The experimental implementation and performance analysis of NLV-SVC and NVC modulation strategies are carried out by the low-power ($1\Phi$) model. For comparison purposes, low-power and medium-power ($1\Phi$ and $3\Phi$) models are simulated.

## 4. Results and analysis

### 4.1. Simulation results

The simulated model of the 3-cell asymmetrical multilevel inverter shown in Figure 8 is designed with the parameters shown in Table 1. Both low- and medium-power models are equipped with 1:3:9 ratio-related

individual DC sources to get an asymmetrical nature in construction and operation to analyze the performance of the NLV-SVC modulation.

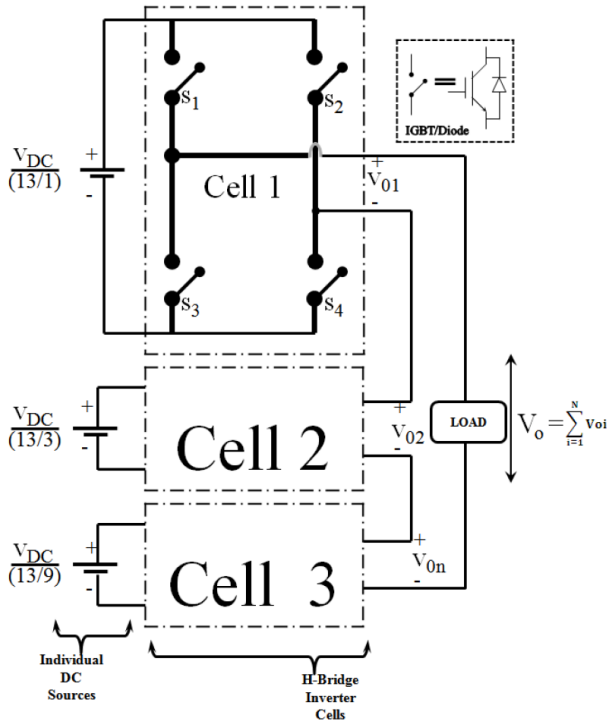


**Figure 8.** Asymmetrical CHB multilevel inverter.

**Table 1.** Simulation model parameters.

| | | |
|---|---|---|
| DC voltages | 1 V : 3 V : 9 V (3 cells) | |
| | 3 V : 9 V : 27 V<br>Low-power model | 18 V : 53 V : 159 V<br>Medium-power model |
| Load | R = 10 Ω, L = 25 mH | |
| $f_0$ | 50 Hz | |
| Switches | IGBT / D | |
| Modulation strategy | NVC and NLC | |
| Max. step size | 1e-6 s | |

The proposed modulation technique, NLV-SVC, is a combination of rounded reference signal with NVC strategy. Comparisons like implementation, operation, and performance analyses are done with NVC. The low-power model with simulation results for NVC and NLV-SVC modulation strategies are shown in Figures 9–16. The comparison of results for the low-power and medium-power ($1\Phi$ and $3\Phi$) models is shown in Table 2.

Figures 9–12 present simulated results for the single-phase low-power model with NVC strategy. The 27-level voltage and current waveforms are shown in Figure 9. The asymmetrical multilevel inverter is operated with different ratings of DC sources for each conversion cells. These cells are operated in the +ve region, -ve region, and a neutral or freewheeling state to get a particular level in the output side. The asymmetrical nature of operation reflects the low-rated conversion cell having more changes in the operating region than the high-rated cell. This asymmetrical nature also affects the switching frequency of switches and the power

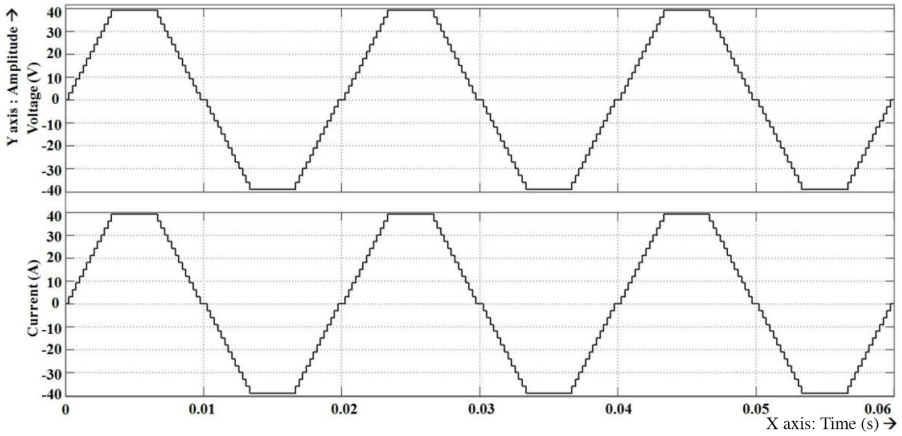


**Figure 9.** Output voltage and current waveforms for NVC.

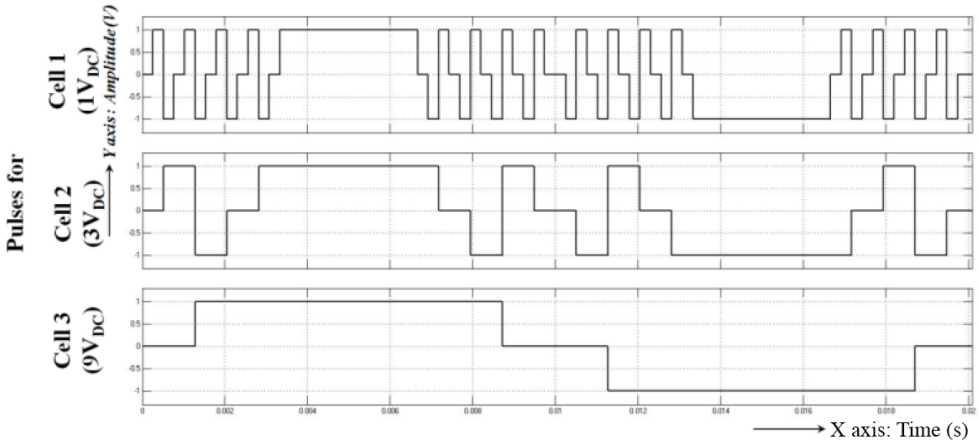


**Figure 10.** Gating pulses to asymmetrical multilevel inverter for NVC.

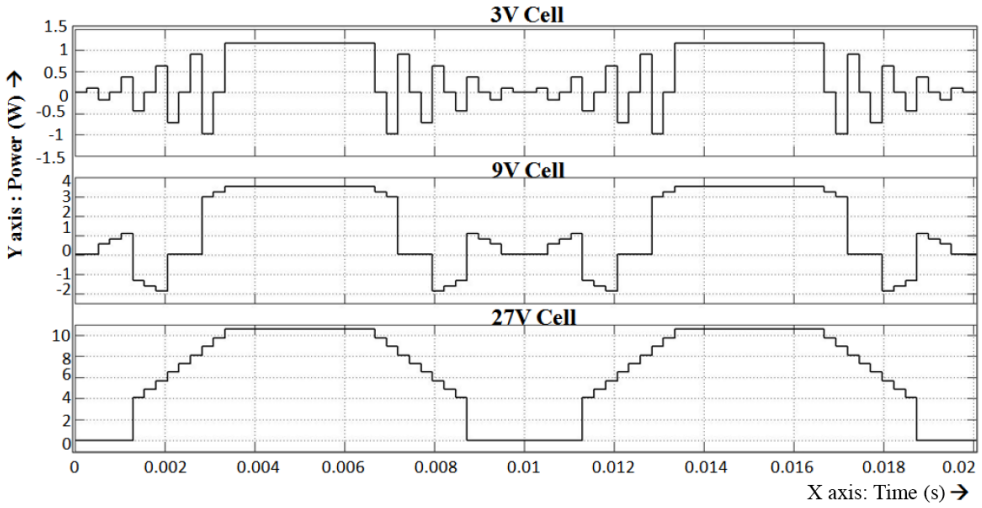


**Figure 11.** Cell-wise power sharing waveforms with NVC strategy.

sharing of DC sources is different among the three cells. The individual voltage sources help to avoid the cell-balancing problem. The switching pulses and power of the 3 cells are shown in Figures 10 and 11, respectively.

**Table 2.** Comparison of THD for NVC and NLV-SVC strategies.

| Modulation strategy | Type of model | Type of phase | Fundamental value (V) | | VTHD (%) | |
|---|---|---|---|---|---|---|
| | | | R load | RL load | R | RL |
| NVC | Low-power | 1-Φ | 40.08 | 40.08 | 6.55 | 6.55 |
| | Medium-power | 1-Φ | 236.2 | 236.2 | 6.57 | 6.57 |
| | | 3-Φ | 409.1 | 409.1 | 5.53 | 5.53 |
| NLV-SVC | Low-power | 1-Φ | 38.97 | 38.97 | 3.33 | 3.33 |
| | Medium-power | 1-Φ | 229.5 | 229.5 | 3.34 | 3.34 |
| | | 3-Φ | 397.5 | 397.5 | 3.34 | 3.34 |

The spectral analysis of the NVC strategy-based line-to-line voltage wave of low- and medium-power models is shown in Figure 12.

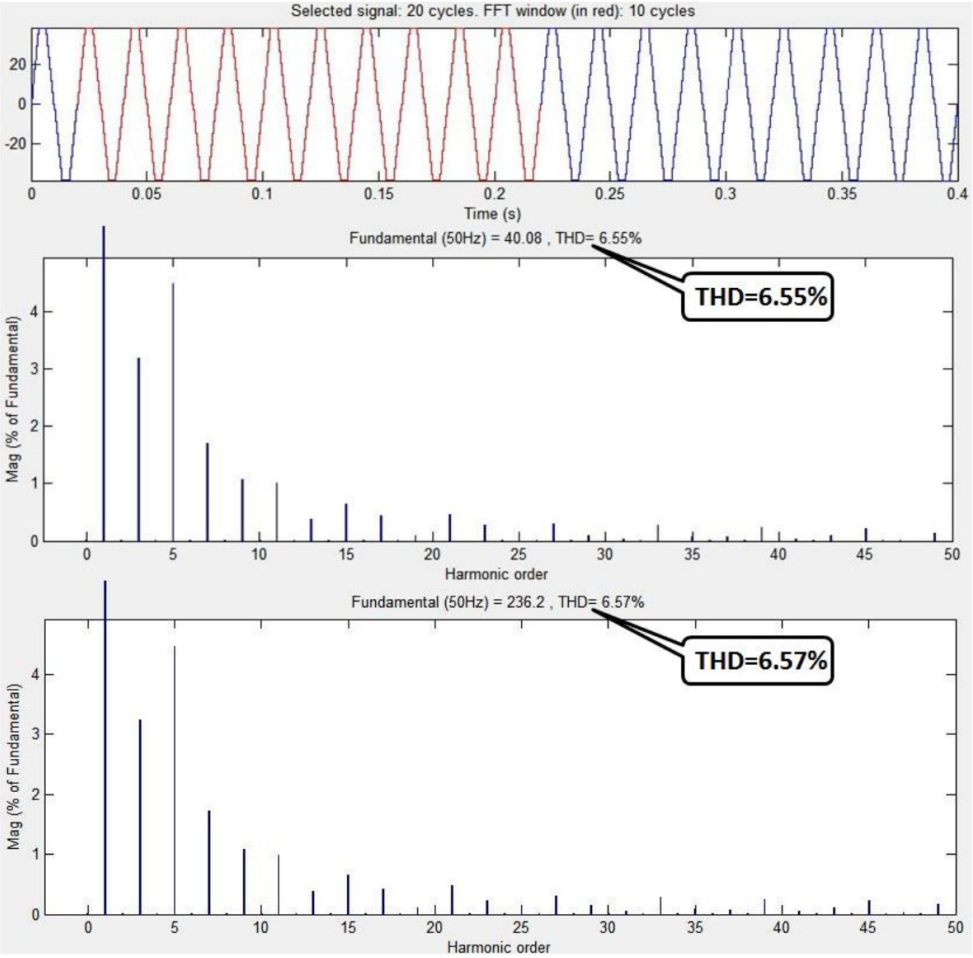


**Figure 12.** Simulated frequency spectrum of voltage signal for NVC strategy.

Figures 13–16 illustrate the simulated results for the single-phase low-power model with the proposed NLV-SVC modulation strategy. The 27-level voltage and current waveforms are shown in Figure 13, with the comparison of NVC-based voltage and current waveforms as shown in Figure 9 whereby the proposed NLV-SVC-based voltage and current signals are smooth and sinusoidal in nature.

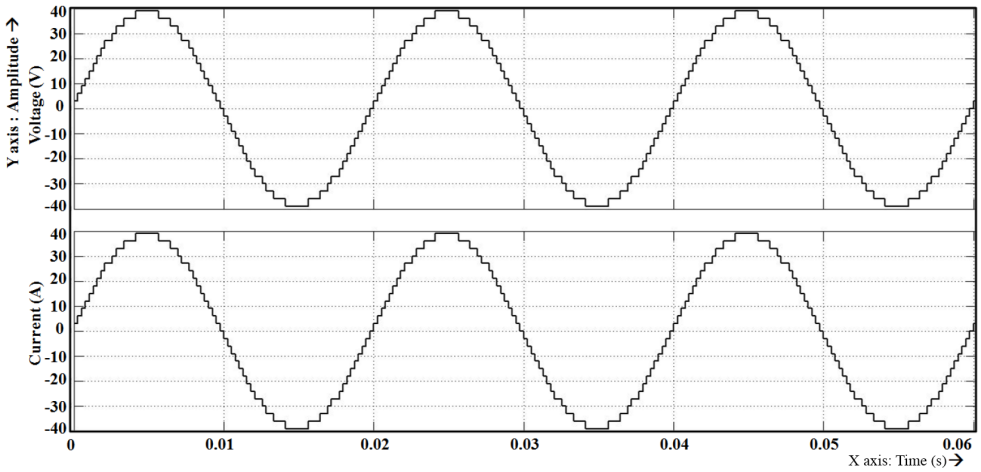


**Figure 13.** Output voltage and current waveforms for NLV-SVC.

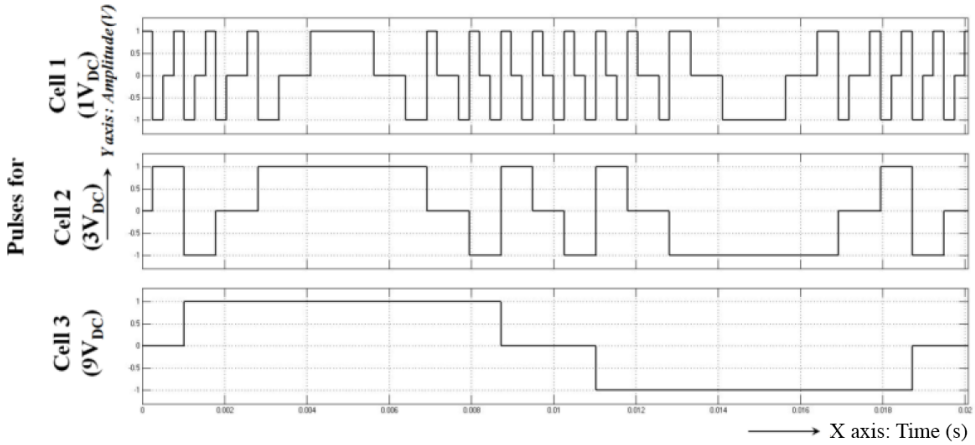


**Figure 14.** Gating pulses to asymmetrical multilevel inverter for NLV-SVC.

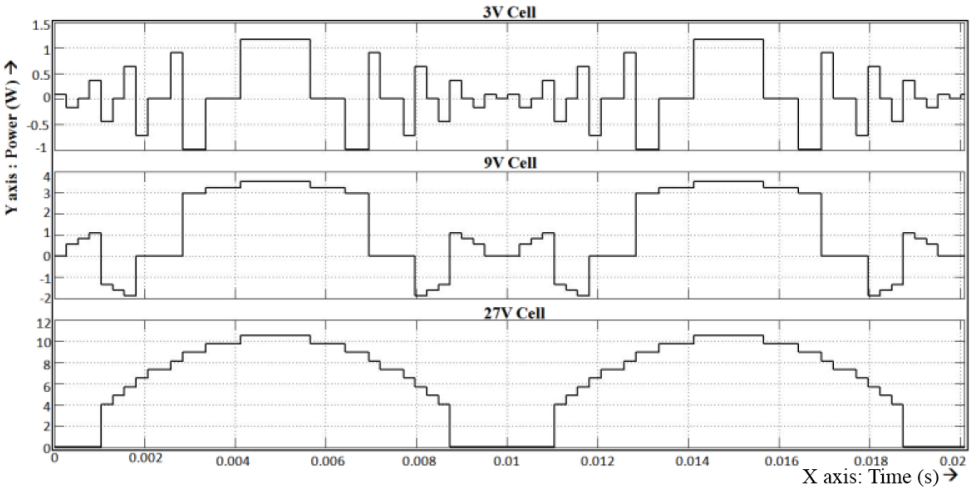


**Figure 15.** Cell-wise power sharing waveforms with NLV-SVC strategy.

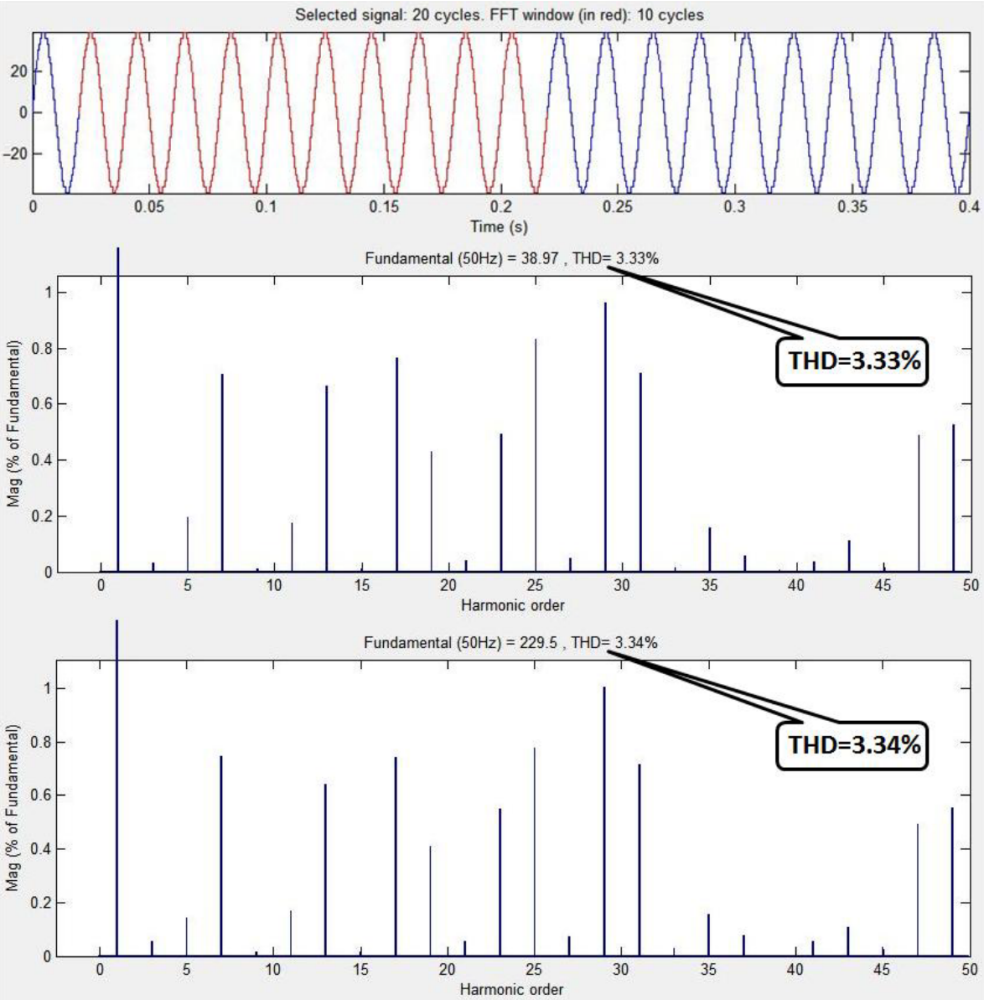


**Figure 16.** Simulated frequency spectrum of voltage signal for NLV-SVC strategy.

The switching pulses and power of the 3 cells are shown in Figures 14 and 15, respectively. Figure 16 shows the spectral analysis of the proposed NLV-SVC strategy-based line-to-line voltage wave of low- and medium-power models.

### 4.2. Experimental results

To implement, compare, and validate the NLV-SVC strategy for 3 cells of the 27-level asymmetrical multilevel inverter with simulation, an experimental model is designed with reference to NVC strategies. The experimental single-phase 3-cell multilevel inverter prototype is shown in Figure 17. Figure 18 shows a close view of the driver circuit and inverter.

A single IGBT with antiparallel diode module FGL40N120ANDC10JJ (1200 V, 40 A) is selected for the design of the H-bridge cells. The prototype is controlled and associated with the use of a high-performance, standalone development platform digital signal processor (DSP) 150 MHz TMS320F28335 from Texas Instruments. The parameters used in the experiment are the same as the parameters of the low-power simulated model.

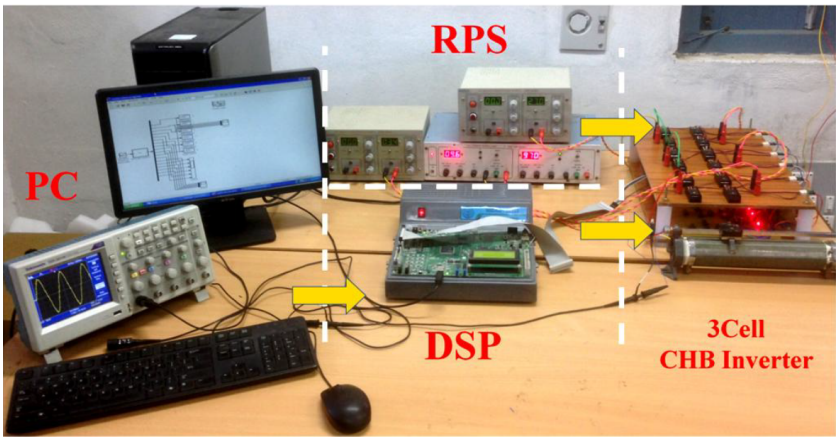


**Figure 17.** Experimental setup of single phase 3-cell CHB multilevel inverter prototype.

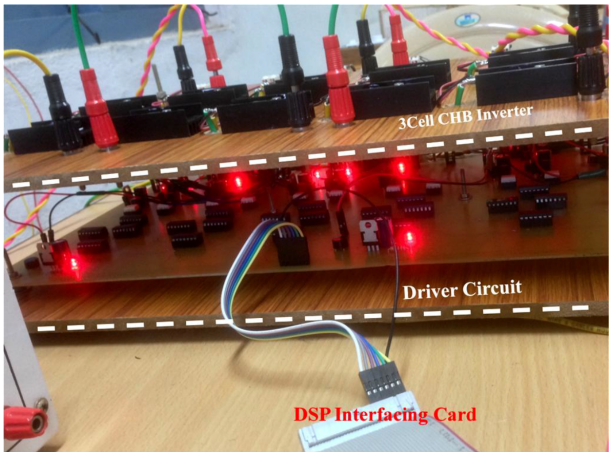


**Figure 18.** Close view of driver circuit and CHB multilevel inverter setup.

The NVC strategy-based 27-level voltage waveforms and spectral analysis are shown in Figures 19–21. Figure 19 illustrates the NVC-based voltage waveform and also shows the duration of the 50 Hz cycle of the NVC modulated 27-level voltage wave. Figure 20 shows a clear view of levels 0–13 of the NVC modulated inverter output voltage wave. Spectral analysis of the NVC modulated inverter output voltage signal is shown in Figure 21, and it is also indicated that the NVC strategy-based voltage signal has 10.45% harmonic distortions.

The proposed NLV-SVC strategy-based 27-level voltage waveforms and spectral analysis are shown in Figures 22–25. Figure 22 illustrates the NLV-SVC-based voltage waveform and also shows the 50 Hz cycle of the NLV-SVC modulated 27-level voltage wave. Comparison of Figures 19 and 22 will provide illustrative information about the better performance of the NLV-SVC modulation-based voltage signal because it has a resemblance to a sinusoidal wave. Figure 23 shows a clear view of levels 0–13 of the NLV-SVC modulated inverter output voltage wave. The spectral analysis of harmonic order for the proposed NLV-SVC and a snapshot of the measured window by Power Analyzer are shown in Figures 24 and 25, respectively.

Table 3 gives a comparison of simulated and experimental values of the NVC and NLV-SVC strategies for the low-power model with load variation R and RL. Figure 26 shows a graphical comparison of spectral analysis for NVC and NLV-SVC.

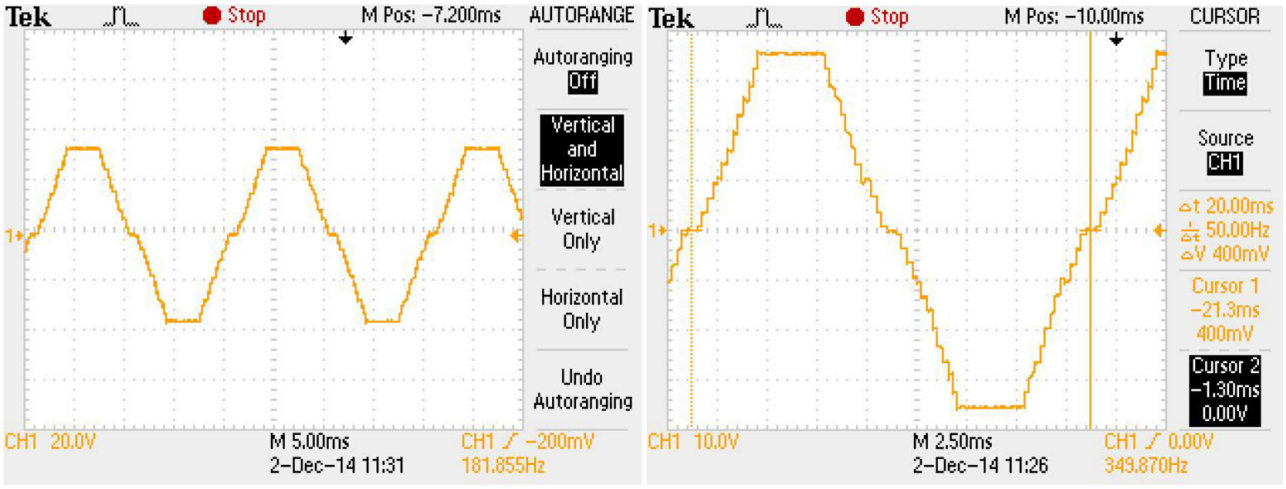


**Figure 19.** Voltage waveform for NVC strategy-based 27-level asymmetrical CHB multilevel, 50 Hz cycle of NVC modulated voltage signal.

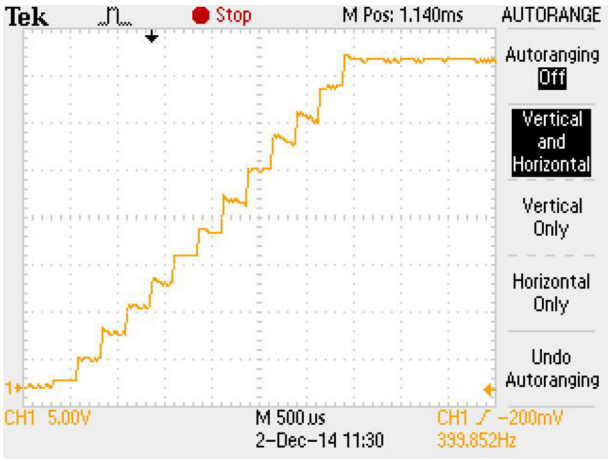


**Figure 20.** Magnified view of levels (0-13) for NVC strategy.

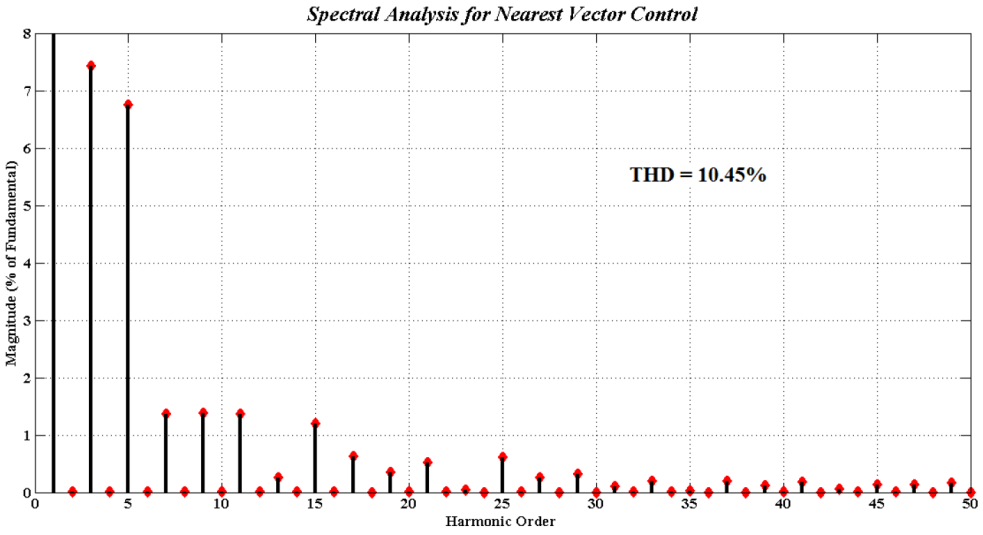


**Figure 21.** Spectral analysis of NVC strategy.

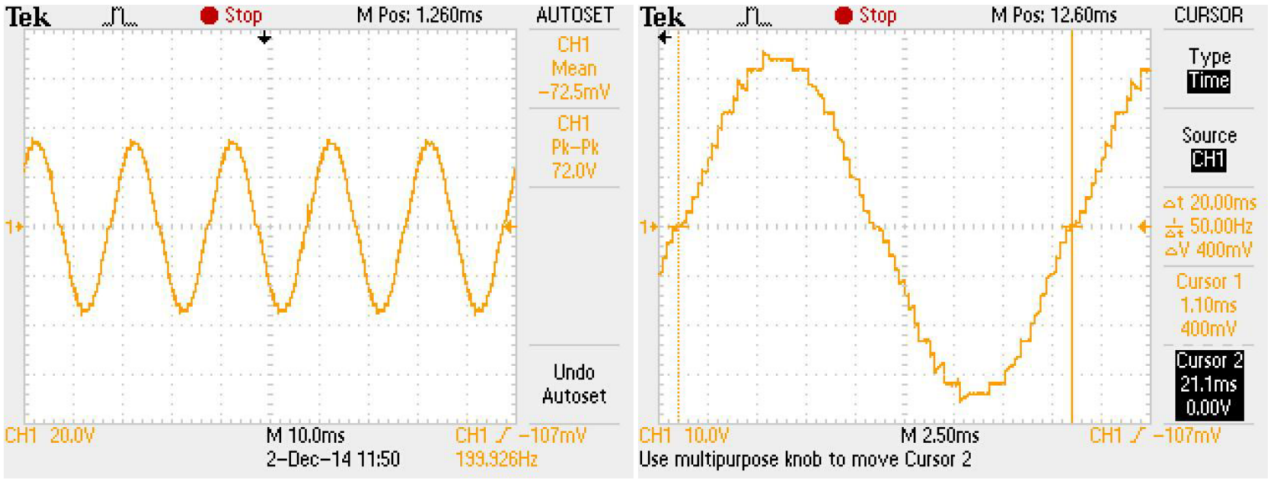


**Figure 22.** Voltage waveform for NLV-SVC strategy-based 27-level asymmetrical CHB multilevel, 50 Hz cycle of NLV-SVC modulated voltage signal.

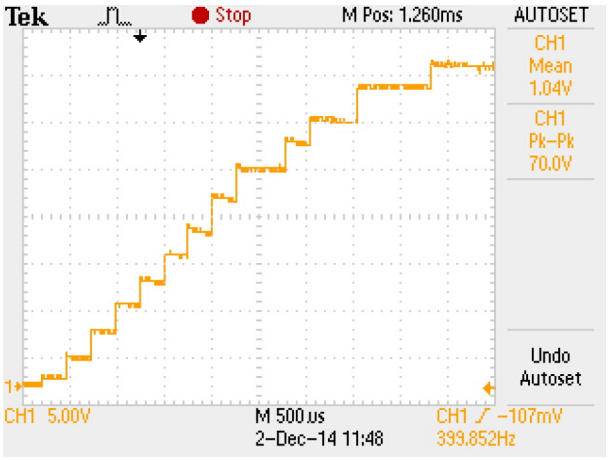


**Figure 23.** Magnified view of levels 0–13 for NLV-SVC strategy.

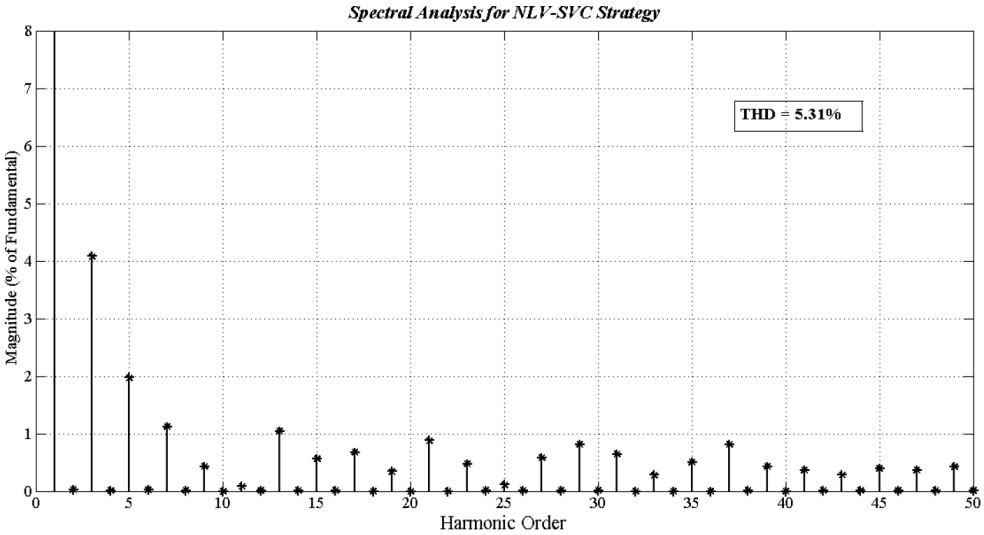


**Figure 24.** Spectral analysis of NLV-SVC strategy.

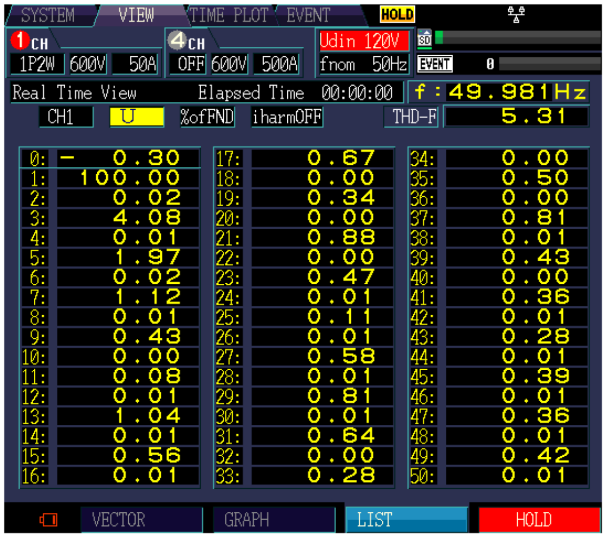


**Figure 25.** Snapshot of power analyzer's harmonic measurement for NLV-SVC strategy.

**Table 3.** Comparison between experimental/simulated values of THD for NVC and NLV-SVC strategies.

| Model parameters | Type of analysis/ modulation strategy | VTHD (%) | |
|---|---|---|---|
| | | R load | RL load |
| 1 − Φ 3-Cell, 27-level Asymmetrical (3:9:27 V) Multilevel inverter with load (R = 10 Ω, L = 25 mH) | Simulation/NVC | 6.55 | 6.55 |
| | Experimental/NVC | 10.45 | 10.40 |
| | Simulation/NLV-SVC | 3.33 | 3.33 |
| | Experimental/NLV-SVC | 5.31 | 5.90 |

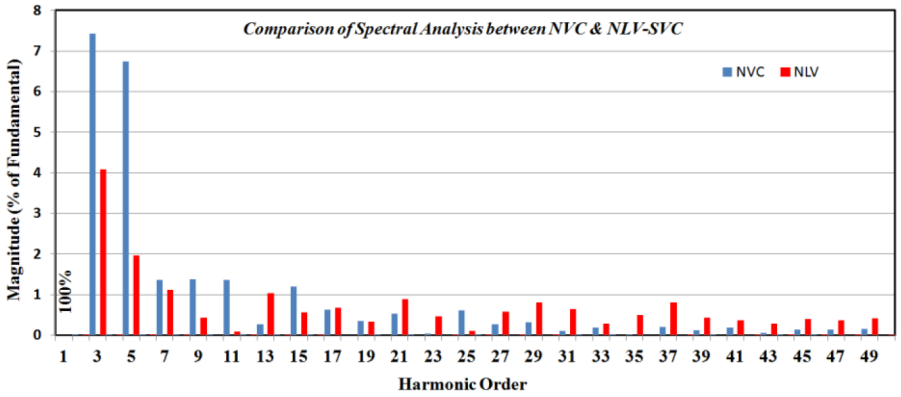


**Figure 26.** Comparison of spectral analysis between NVC and NLV-SVC strategies.

## 5. Discussion

The simulation and experimental results of the 27-level 3-cell asymmetrical cascaded H-bridge multilevel inverter prove the feasibility of the proposed NLV-SVC modulation strategy over NVC in implementation and better performance. The nearest level is approximated at each and every sector's duration to select a proper vector in the proposed strategy. Hence, the harmonic distortions of the NVC are reduced with the new approach, and this control algorithm can be extended to any N-level inverter. Furthermore, the NLV-SVC could be used not only with an AS-CHB multilevel inverter but also with other multilevel inverter configurations compatible with

SVC strategy. The experimental results show the compatibility of NVC and NLV-SVC modulation strategies to be implemented for the 3-cell asymmetrical multilevel inverter in real-time applications.

The variations of performance parameter (THD) values for both NVC and NLV-SVC strategies from simulation to experimentation deviate by about 3.9% and 1.98%, respectively. The NVC strategy-based 27-level voltage waveform has less performance with the reference of THD values measured by the simulation and experimentation than NLV-SVC. Implementation of NLV-SVC for the asymmetrical multilevel inverter exhibits the features of high efficiency, compactness, and high-quality output signal with low THD. Comparison with simulation and experimental results demonstrates the dominance of the proposed NLV-SVC modulation strategy for the multilevel inverter applications than other vector-based strategies.

**Acknowledgments**

The authors gratefully acknowledge the support provided by Jawaharlal Nehru Technological University Kakinada, Andhra Pradesh, and the TEQIP Centrally Sponsored Scheme through Ministry (HRD) of Govt. of India and also Shri Vishnu Engineering College for Women's (Autonomous), Bhimavaram.

## References

[1] Rodriguez J, Franquelo LG, Kouro S, Leon JI, Portillo RC, Prats MAM, Perez MA. Multilevel converters: an enabling technology for high-power applications. P IEEE 2009; 97: 1786-1817.

[2] Malinowski M, Gopakumar K, Rodriguez J, Perez MA. A survey on cascaded multilevel inverter. IEEE T Ind Electron 2010; 57: 2197-2206.

[3] Rodriguez J, Lai JS, Peng FZ. Multilevel inverter: a survey of topologies, control, and applications. IEEE T Ind Electron 2002; 49: 724-738.

[4] Franquelo LG, Rodriguez J, Leon JI, Kouro S, Portillo R, Prats MAM. The age of multilevel converters arrives. IEEE Ind Electron M 2008; 2: 28-39.

[5] Ozpineci B, Tolbert LM, Chiasson JN. Harmonic optimization of multilevel converters using genetic algorithm. IEEE Power Electron Lett. 2005; 3: 92-95.

[6] McGrath BP, Holmes DG, Meynard T. Reduced PWM harmonic distortion for multilevel inverters operating over a wide modulation range. IEEE T Ind Electron 2006; 21: 941-949.

[7] Rabinovici R, Baimel D, Tomasik J, Zuckerberger A. Series space vector modulation for multi-level cascaded H-bridge inverter. IET Power Electron 2010; 3: 843-857.

[8] Mekhilef S, Kadir MNA. Novel vector control method for three-stage hybrid cascaded multilevel inverter. IEEE T Ind Electron 2011; 58: 1339-1349.

[9] Rodriguez J, Bernet S, Wu B, Pontt JO, Kouro S. Multilevel voltage-source-converter topologies for industrial medium-voltage drives. IEEE T Ind Electron 2007; 54: 2930-2945.

[10] Ding K, Cheng KWE, Zou YP. Analysis of an asymmetrical modulation method for cascaded multilevel inverters. IET Power Electron 2011; 5: 74-85.

[11] Perez M, Rodriguez J, Pontt J, Kouro S. Power distribution in hybrid multi-cell converter with nearest level modulation. In: IEEE 2007 International Symposium on Industrial Electronics; 4–7 June 2007; Vigo, Spain. New York, NY, USA: IEEE. pp. 736-741.

[12] Colak I, Kabalci E, Bayindir R. Review of multilevel voltage source inverter topologies and control schemes. Energ Convers Manage 2010; 52: 1114-1128.

[13] Rodriguez J, Pontt J, Correa P, Cortes P, Silva C. A new modulation method to reduced common mode voltages in multilevel inverters. IEEE T Ind Electron 2004; 51: 834-839.

[14] Rodriguez J, Moran L, Correa P, Silva C. A vector control technique for medium-voltage multilevel inverters. IEEE T Ind Electron 2002; 49: 882-888.

[15] Khoucha F, Lagoun MS, Kheloui A, El Hachemi Benbouzid M. A comparison of symmetrical and asymmetrical three-phase h-bridge multilevel inverter for DTC induction motor drives. IEEE T Energy Conver 2011; 26: 64-72.

[16] Panda AK, Suresh Y. Research on cascaded multilevel inverter with single dc source by using three-phase transformers. INT J Elec Power 2012; 40: 9-20.

[17] Kouro S, Bernal R, Miranda H, Silva CA, Rodriguez J. High-performance torque and flux control for multilevel inverter fed induction motor. IEEE T Power Electr 2007; 22: 2116-2123.