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Design of a low-power CMOS operational amplifier with common-mode feedback for pipeline analog-to-digital converter applications

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Abstract: This paper proposes a design of a low-power operational amplifier (op-amp) for pipeline analog-to-digital converter (ADC) applications using a 0.13-μm CMOS process. The folded-cascode topology with NMOS input types is employed for the op-amp design due to a larger output gain compared to PMOS input types. Furthermore, the op-amp is designed with a double detection structure of a common-mode feedback circuit to provide stable feedback voltage. The simulation results show that the proposed op-amp achieved a gain of 64.5 dB and a unity gain bandwidth of 695.1 MHz with a low power consumption of 0.14 mW. In addition, by applying $\pm$1.2 V of input voltage, the output voltage generated by the proposed op-amp design remains at 1.2 V with a constant feedback voltage of 1.3 V. Moreover, the proposed circuit was implemented and simulated successfully in a 1.5-bit per stage pipeline ADC.

Key words: Analog-to-digital converter, fully differential op-amp, low power, low voltage, pipeline

1. Introduction

A pipeline is an important part of an analog-to-digital converter (ADC), and it plays an essential role in applications that require interface between analogs and digital domains. The pipeline architecture covers numerous signals that process applications used in communication, instrumentation, and imaging systems because the architecture is classified as high-speed and high-accuracy [1]. This architecture is designed for power-efficient high-speed conversion of wide bandwidth input signals in the range of 10 to 100 mega samples per second with medium to high resolution bits of around 8- to 14-bits resolution [2]. As discussed in [3], a pipeline ADC is an open-loop architecture with a small inherent latency of between 4 and 6 clock cycles and has a direct relationship with the input signal and the output code. Figure 1 illustrates the architecture of a pipeline ADC, which consists of individual stages such as a low-resolution ADC, digital-to-analog converter (DAC), sample and hold circuit, and amplifier circuit that successively alters the analog signal into the digital signal by converting the data in a pipe-lined manner [1].

An operational amplifier (op-amp) is a core element and the most important integral part of the pipeline architecture. The op-amp has high input and low output impedance that are both used with a single-loop and negative feedback in order to achieve precision signal processing. Generally, the op-amp is divided into several types of topologies such as a telescopic op-amp, folded-cascode op-amp, 2-stage op-amp, and a gain-boosted op-amp, as shown in Figure 2 [4]. In brief, a telescopic op-amp is a simple topology compared to other topologies. Traditionally, the telescopic topology, shown in Figure 2a, is constructed from only one type of transistor in

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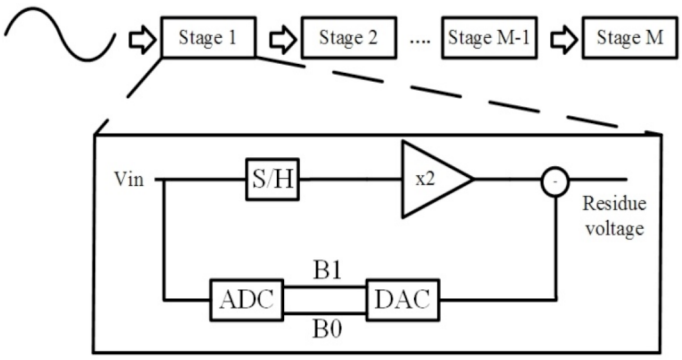

Figure 1. Pipeline ADC architecture [1].

the signal path, which is an NMOS type. This topology provides faster performance with high gain and, in addition, shows lower power consumption and lower noise. However, it requires a higher supply voltage in order to control and to ensure that the input and output of the common mode remain at the same level (an equal value of input and output). Meanwhile, for the folded-cascode topology, shown in Figure 2b, the structure is naturally modified from the telescopic op-amp. Based on the rule of this topology, the folded cascode can be constructed by 2 types of transistor in the signal path, either an NMOS or a PMOS type. This signal path will produce a different op-amp circuit performance. The folded-cascode op-amp commonly produces a higher gain, yet it shows higher power consumption and also higher noise output compared to the telescopic op-amp. However, the folded-cascode op-amp easily controls the input and output of common mode, and it can operate at a low-power voltage supply. Figure 2c shows the topology of a 2-stage op-amp that yields more gain and swing. Essentially, the first stage contains a differential input, which converts the input voltage to current and provides a high gain. The second stage is configured with a simple common-source stage, which converts the current to the voltage output and provides high swing. As for the gain-boosted op-amp, shown in Figure 2d, it is typically utilized to maximize the output impedances as well as to attain high gain [4]. This topology is usually employed in order to reduce problems with stacking among the transistors. However, it has high power consumption and noise and also requires a high voltage supply in order to conduct the op-amp circuit.

2. Circuit implementation

2.1. Design specifications

Based on the requirement of a high-speed and high-accuracy pipeline ADC, the op-amp becomes a primary and delicate design. The specifications of the op-amp for 10- to 12-bit ADC applications are designated in Table 1.

2.2. The proposed circuit design

Based on the design specifications listed in Table 1, a suitable op-amp topology is taken into consideration in order to meet all requirements of the design specifications. As mentioned in [4], a comparable performance of op-amp topologies that represents the folded-cascode topology produces high gain and high speed even though the topology can be operated at a low-voltage supply. Besides this, the topology has also been used to obtain high DC and fast settling with high unity and high gain apart from low power consumption [5–7]. In addition, a common-mode feedback circuit is vital in this op-amp design to stabilize the output that is generated by the op-amp circuit as well as to ensure proper operation of a fully differential op-amp, as discussed in [8–10].

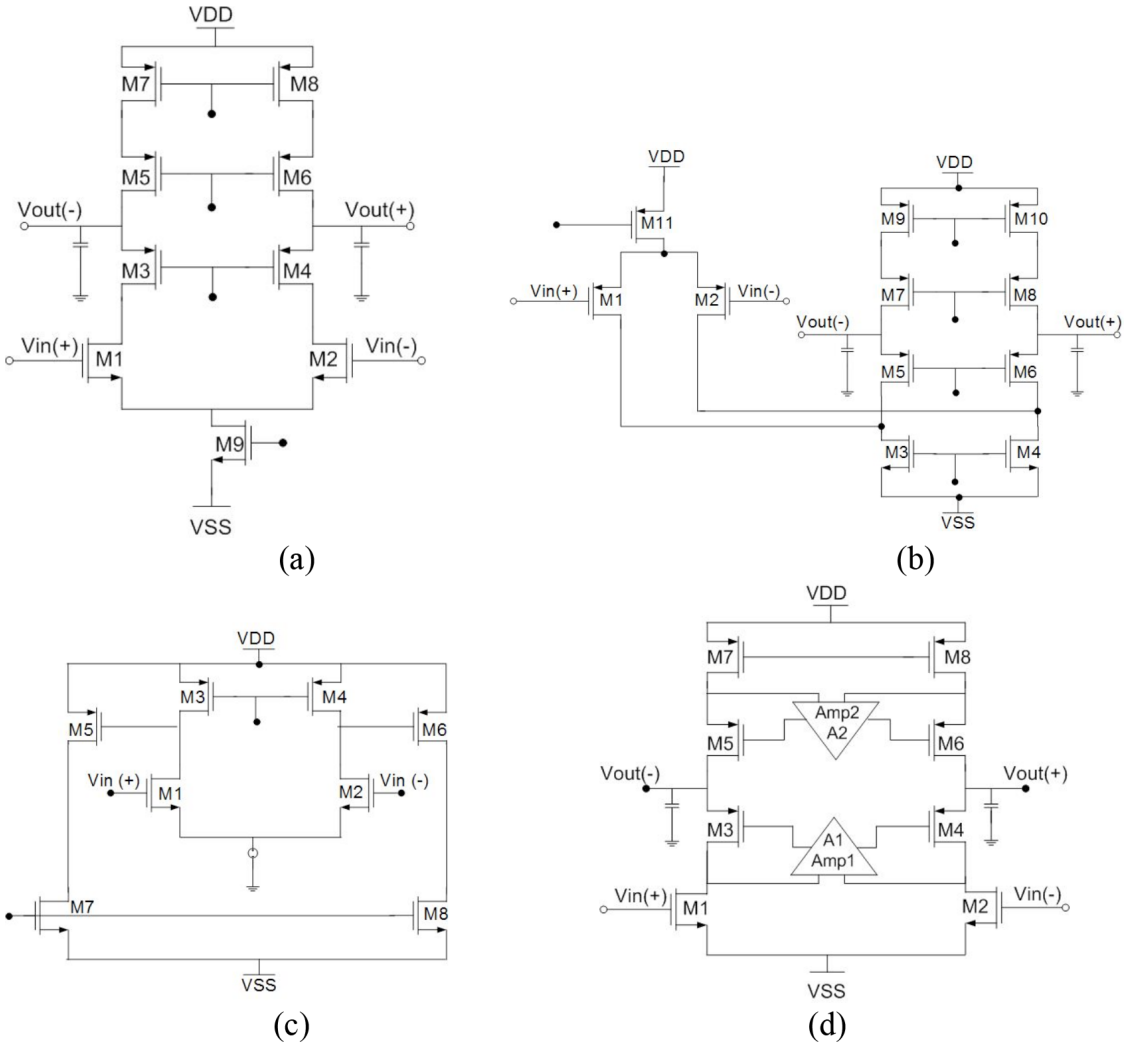

Figure 2. Op-amp topologies [4]: a) telescopic, b) folded cascode with PMOS input, c) two-stage, and d) gain-boosted.

Table 1. Op-amp design specification for pipeline ADC.

Parameter	Value
Voltage supply	±1.8 V
Vin	±1.2 V
Vout	1.2 V
DC gain	> 70 dB
Phase margin	> 50°
Unity gain bandwidth	> 130 MHz

2.2.1. Folded-cascode op-amp

The folded-cascode topology with NMOS input types is a better alternative as a main op-amp design due to the limitation of op-amp specifications because the input types used produce a larger output gain than PMOS input types. Figures 3a and 3b illustrate the folded-cascode op-amp with NMOS topology. The details of this op-amp design are discussed in the following section.

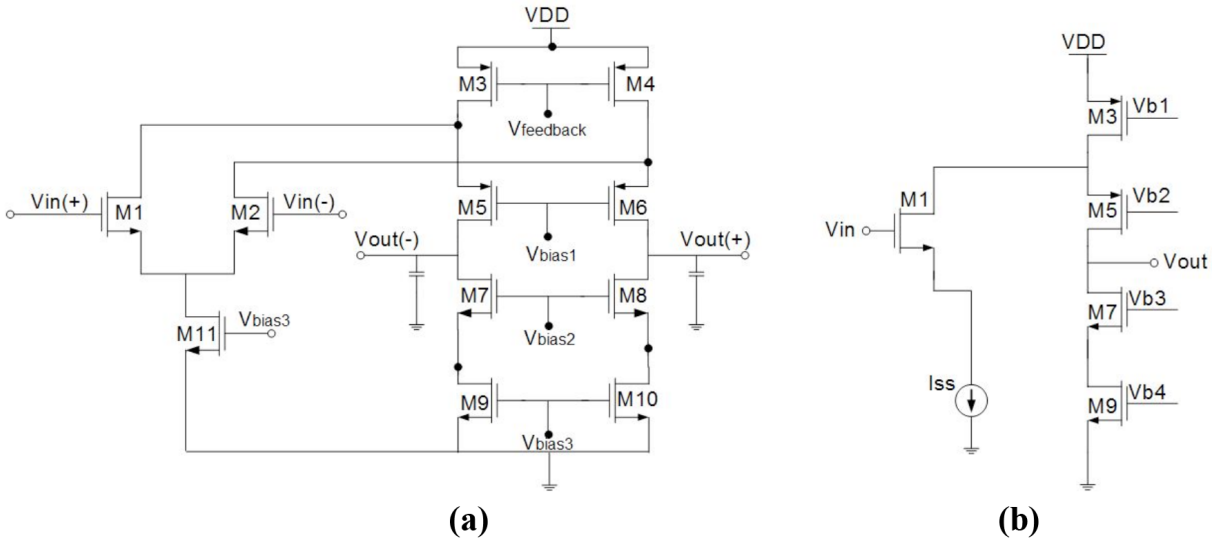

Figure 3. Folded cascode with NMOS input structure: a) complete circuit, b) half circuit.

Referring to Figure 3b, the proposed folded cascode is constructed by considering the half circuit. The essential property of a small-signal analysis, the gain (A_v), is obtained as:

$$A_v = G_m \times R_{out}, \tag{1}$$

where $G_m \approx g_{m1}$ and g_{m1} is a transconductance of the input transistor of M1.

By using Eq. (2), g_m is equal to 816.81 $\times$ 10^{-6} S with 1 pF of capacitive load represented as C_L. R_{out} is shown in Eq. (3):

$$GBW = \frac{g_m}{C_L}, \tag{2}$$

where GBW is a gain bandwidth product of the op-amp.

$$R_{out} = [g_{m5}.r_{o5}.(r_{o1}||r_{o3})]||[g_{m7}.r_{o7}.r_{o9}] \tag{3}$$

When g_m is obtained, the current I_D across the op-amp can be calculated as:

$$I_D = \frac{g_m \times (V_{GS} - V_{th})}{2}, \tag{4}$$

where V_{GS} is gate-source voltage and V_{th} is threshold voltage.

Therefore, the sizing of transistors can be calculated by using Eq. (5) for the NMOS transistor and Eq. (6) for the PMOS transistor:

$$\frac{W}{L} = \frac{(g_m)^2}{2 \times I_D \times \mu_n c_{ox}}, \tag{5}$$

$$\frac{W}{L} = \frac{(g_m)^2}{2 \times I_D \times \mu_p c_{ox}}, \tag{6}$$

where μ_n is the n-type channel mobility, μ_p is the p-type channel mobility, and C_{ox} is the capacitance per gate unit area.

Table 2 summarizes the transistor ratio result obtained with the 'first-cut' method. It should be noted that the minimum length of the thickness oxide transistor is 0.13 μm, and to minimize the channel length modulation, the length of the transistor is set to 3 times the minimum channel length.

Table 2. Calculated transistor ratio of folded cascode.

Transistor	Aspect ratio	Width/W (μm)	Length/L (μm)	I_{Dsat} (μA)
M1–M2	44	1.599	0.39	20
M3–M4	13	1.755	0.39	40
M5–M6	27	14.04	0.39	20
M7–M8	12	1.599	0.39	20
M9–M10	12	31.98	0.39	20
M11	6	7.995	0.39	40

2.2.2. Biasing circuit

A biasing circuit is an important block because of its function in biasing proper voltage in the op-amp structure. As can be seen in Figure 3a, the voltage biases in the folded-cascode architecture are V_{bias1}, V_{bias2}, and V_{bias3}, which are generated from the biasing circuit designed from the wide-swing current mirror, as shown in Figure 4. A current of 20 μA flows across the transistor of V_{bias1}, V_{bias2}, and V_{bias3} as a reference current (I_{ref}). Therefore, the development of this circuit is effectuated by twining the W/L ratio with respect to I_{ref}, and each node voltage is checked at the cascode stage. It should be noted that the resistor (R) is needed as it functions to bias the current, and it commonly serves as a passive component in biasing circuits. Table 3 presents the W/L ratio of each transistor with the related voltage bias (Vbias).

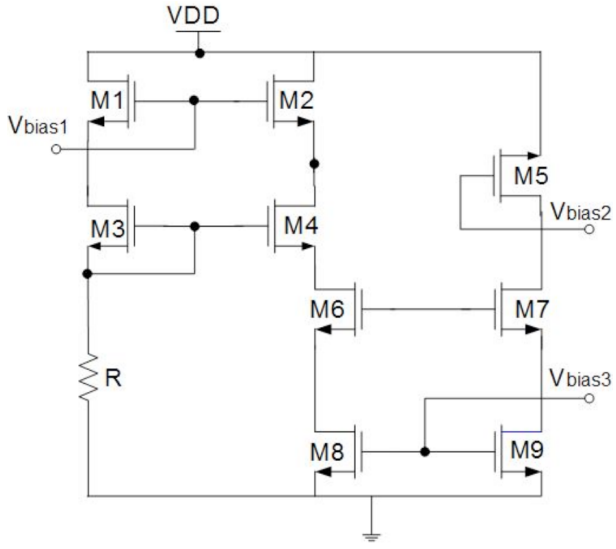

Figure 4. Biasing circuit.

2.2.3. Common-mode feedback circuit

Figure 5a shows a conventional differential difference amplifier (DDA) structure. The transistors of M1 (a) and M1 (b) are modified to be a double detection of $V_{feedback}$ voltage node [11]. A common-mode feedback

Table 3. Biasing circuit performances.

Voltage bias	Transistor	W/L ratio		Voltage (V)	I_{ref} (μA)
		Width	Length		
V_{bias1}	M1–M2	9.35 μm	300 nm	1.00007	20.0003
V_{bias2}	M5	705 nm	300 nm	0.90019	20.0021
V_{bias3}	M8-M9	150 nm	300 nm	0.50012	20.0021

circuit with a modification of a conventional DDA structure, illustrated in Figure 5b, was utilized in this op-amp design. Therefore, the double detection structure provides stable feedback voltage of 1.3 V with 1.2 V input voltage. Moreover, the CMFB structure can also stabilize the 1.2 V output voltage, which is generated by this op-amp circuit. The sizing of each transistor of the CMFB circuit is shown in Table 4.

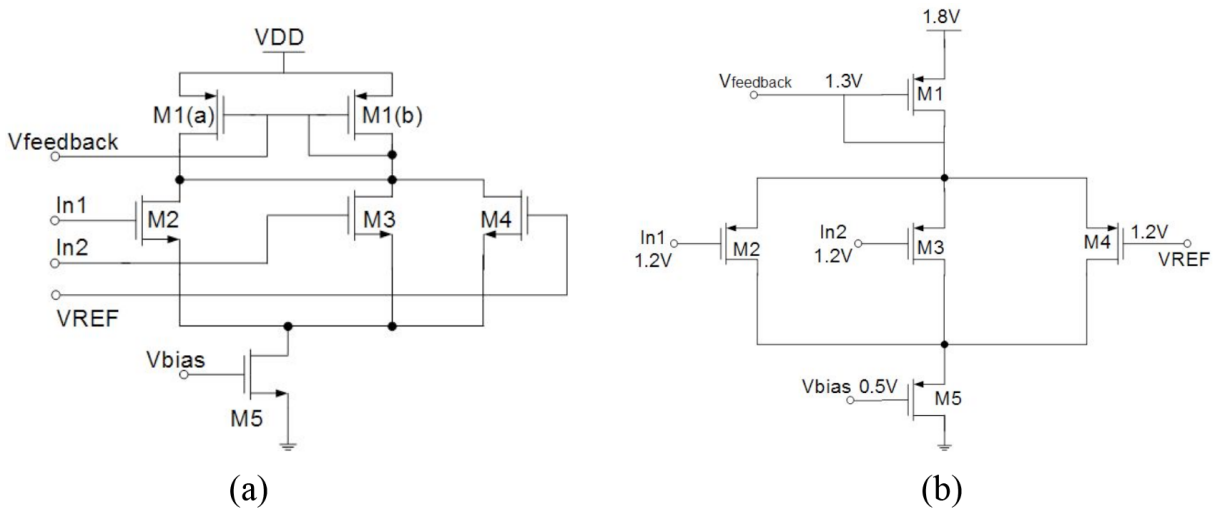

Figure 5. a) Conventional DDA structure [10], b) the proposed CMFB circuit.

Table 4. Transistor sizing in the CMFB circuit.

Transistor	Width (W)	Length (L)	I_{Dsat}
M1	1.0 μm	150 nm	1.00021 μA
M2–M3	785 nm	150 nm	1.00096 μA
M4	800 nm	130 nm	1.00108 μA
M5	2.5 μm	130 nm	1.0077 μA

The completed circuit consisting of biasing and common-mode feedback of the proposed fully differential folded-cascode op-amp is shown in Figure 6. This circuit will later be run through a 1.5-bit per stage pipeline ADC for performance verification.

2.2.4. Integration of folded-cascode op-amp with the CMFB circuit in 1.5-bit per stage ADC

Figure 7 shows the integration of a 1.5-bit per stage pipeline ADC with 3 main circuit blocks. These are the comparator (block A), logic switch (block B), and a residue amplifier (block C). The proposed circuit of the

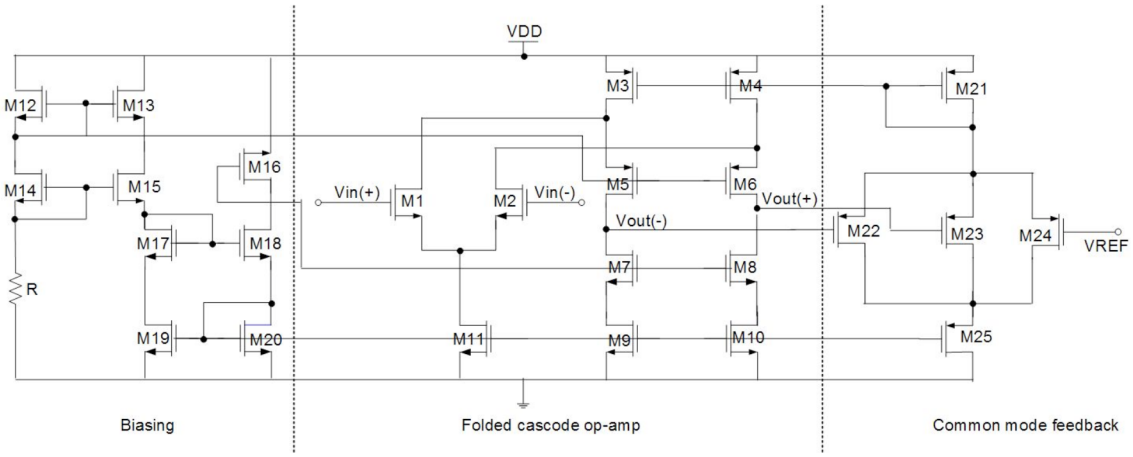

Figure 6. The proposed design of the fully differential folded-cascode op-amp.

folded cascode and CMFB is implemented in the residue amplifier as represented by block C in order to analyze circuit performances. The complete circuit of the residue amplifier is depicted in Figure 8.

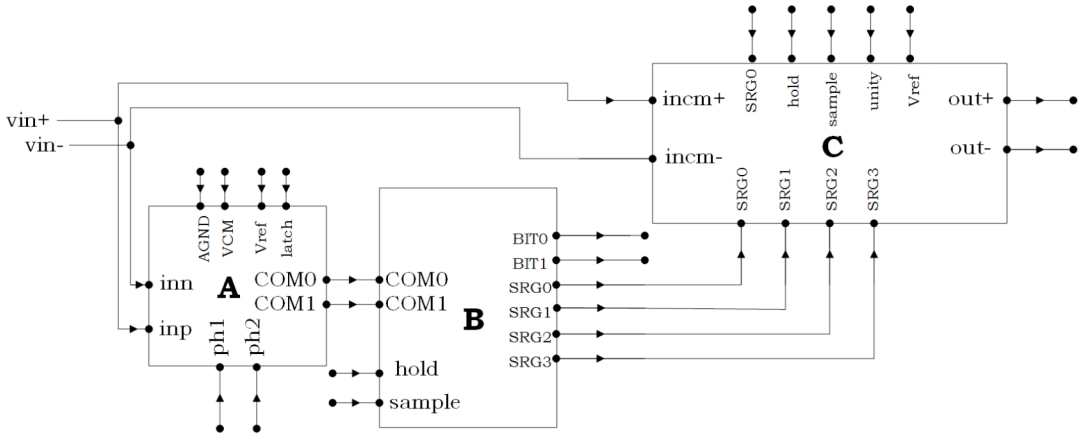

Figure 7. Design implementation of 1.5-bit per stage pipeline ADC.

2.3. Results and discussion

The performance of the proposed circuit design was simulated using a Cadence Virtuoso Spectre Simulator. The process technology is a CMOS 0.13-μm process, and it was powered at 1.8 V voltage supply. The performance of the folded-cascode op-amp is demonstrated based on AC and transient response. From the AC analysis, shown in Figure 9a, the DC gain of the folded cascode of 64.5 dB is obtained with 695.1 MHz unity gain bandwidth (UGB) along 52.5 kHz of cut-off frequency. Meanwhile, the phase margin, as plotted in Figure 9b, is achieved at 68.4° with a 1-pF load capacitor.

Since the parameters of DC gain, UGB, and phase margin become critical in this design, corner analysis was simulated as shown in Figure 10 for 3 potential corners: typical–typical (TT), fast–fast, (FF) and slow–slow (SS). As seen in Figure 10a, DC gain indicates a 4% (SS) and 7% (FF) change from the TT value while the UGB shows different changes between the FF and SS corners from the TT value, which is at 42.7% (SS) and 0.7% (FF), respectively. Therefore, the SS corner of the UGB can be considered as a worst-case scenario for this design. Meanwhile, for the phase margin, depicted in Figure 10b, the value of the FF and SS corners slightly changes from the TT value, which is at 4% (SS) and 1.6% (FF), respectively.

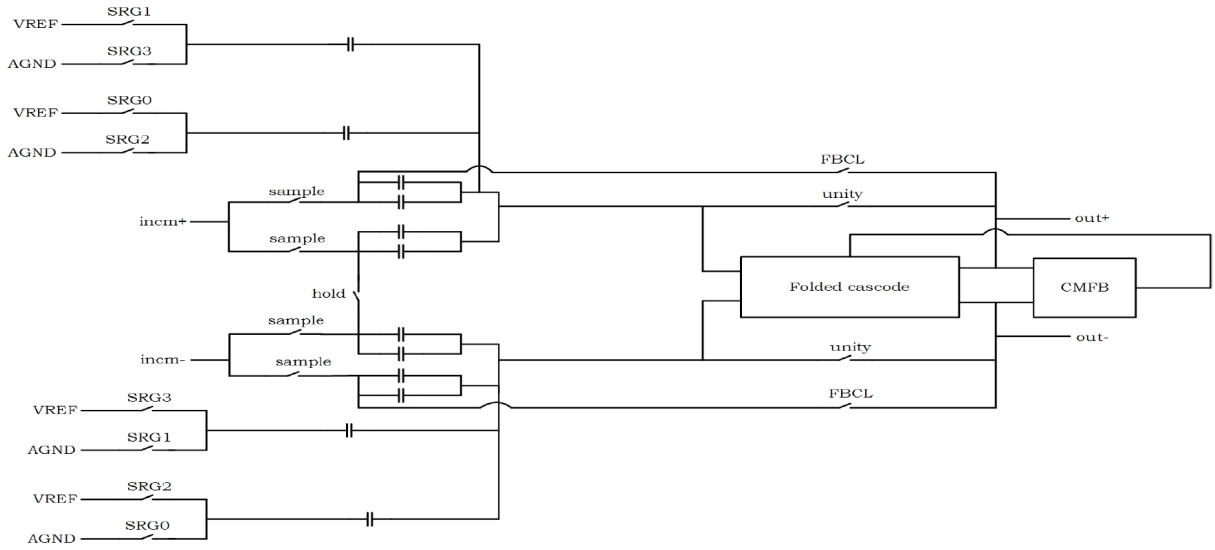

Figure 8. Residue amplifier circuit block.

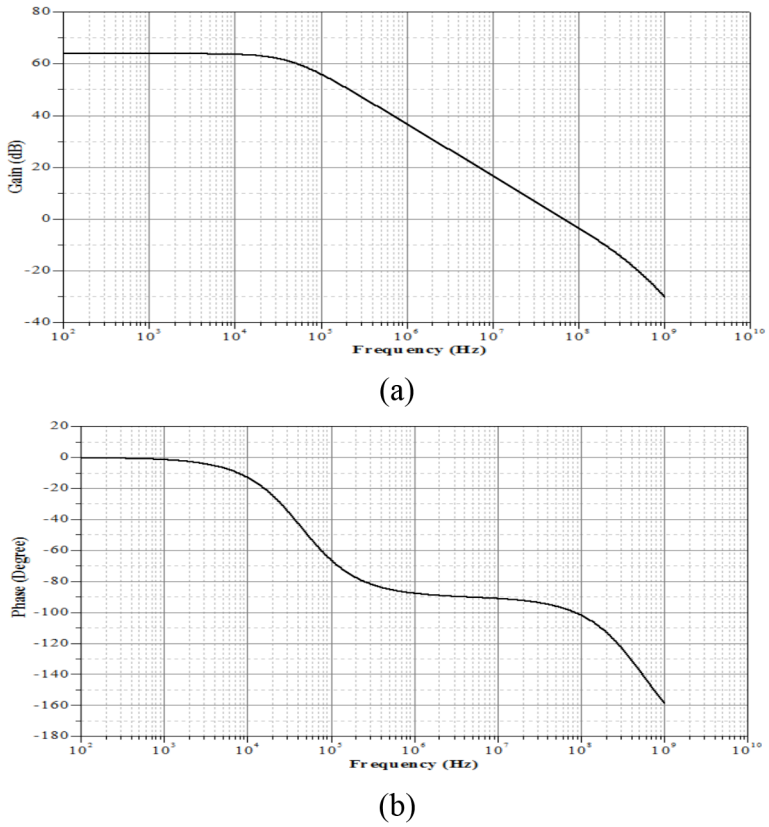

Figure 9. AC analysis: a) DC gain, b) phase margin.

As depicted in Figure 11, the simulated transient analysis result shows that a slew rate of 22.6 V/μs with a settling time of 72.4 ns is obtained.

Figure 12 shows the result of the common mode rejection ratio (CMRR). The CMRR is an important

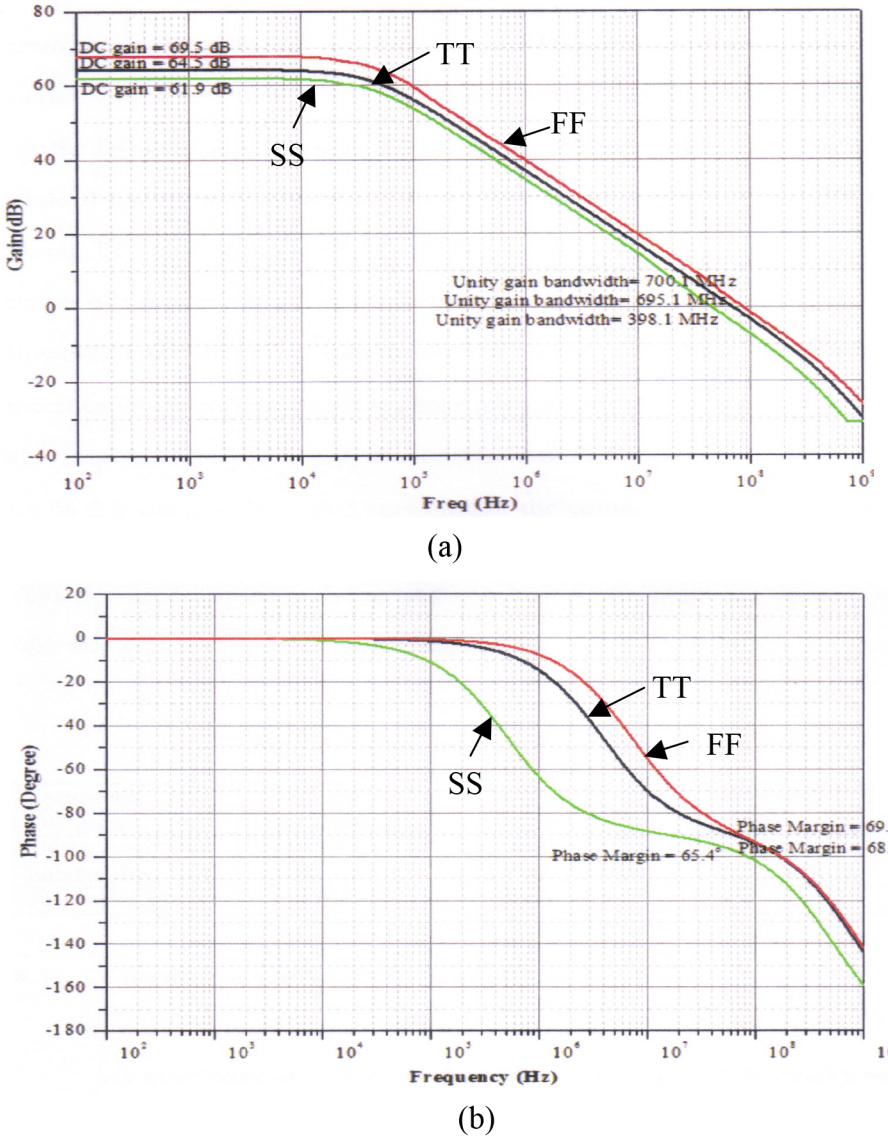

Figure 10. Corner analysis results for the proposed folded cascode op-amp design: a) DC gain and unity gain bandwidth, b) phase margin.

parameter to determine the tendency of the op-amp to reject or cancel out the input-common signals to both inputs. As can be seen, the simulation result indicated that a CMRR of 41.48 dB was achieved.

The main characteristics of the proposed folded-cascode op-amp design are summarized in Table 5. According to the results, the obtained DC gain is a medium gain, which is close to 70 dB. However, the DC gain has little effect on the desired op-amp design because the UGB and the phase margin are still in the range of op-amp design specifications.

Figure 13a outlines the test setup for the CMFB circuit in order to analyze the circuit's performance. The performance of the circuit is illustrated in Figure 13b. According the simulation results, by applying a ± 1.2 V input voltage at In1 and In2, the output voltage that is generated by the proposed op-amp design attains 1.2 V with a constant value of 1.3 V of feedback voltage.

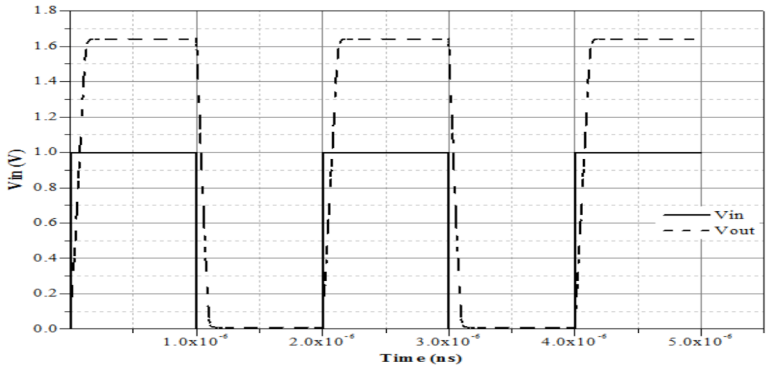

Figure 11. Transient analysis result.

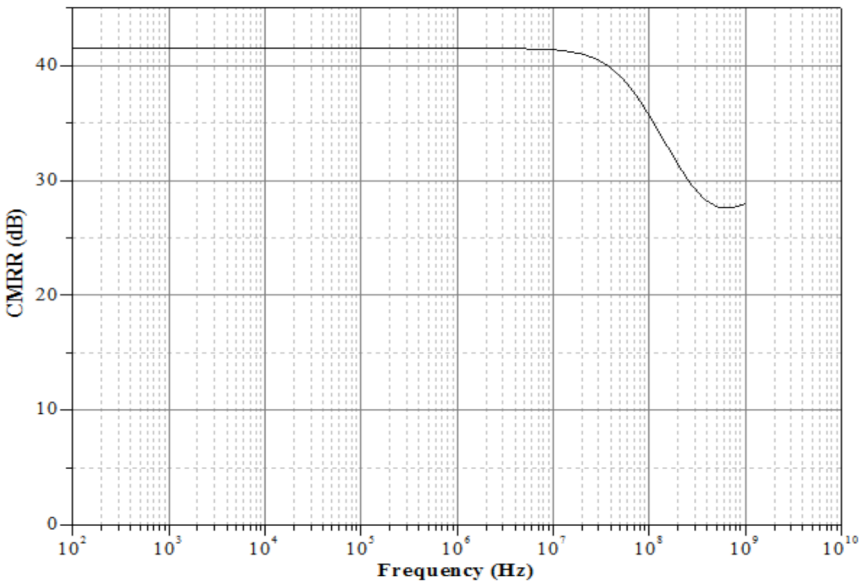

Figure 12. Common mode rejection ratio result.

Table 5. Folded-cascode op-amp performance.

Parameter	Value
DC gain	64.5 dB
Unity gain bandwidth	695.1 MHz
Cut-off frequency	52.5 kHz
Phase margin	68.4°
CMRR	41.48 dB
ICMRR	0.5 V
PSRR	73.15 dB
Slew rate	22.6 V/μs
Settling time	72.4 ns
Output voltage swing	0.4–1.65 V
Power consumption	0.14 mW

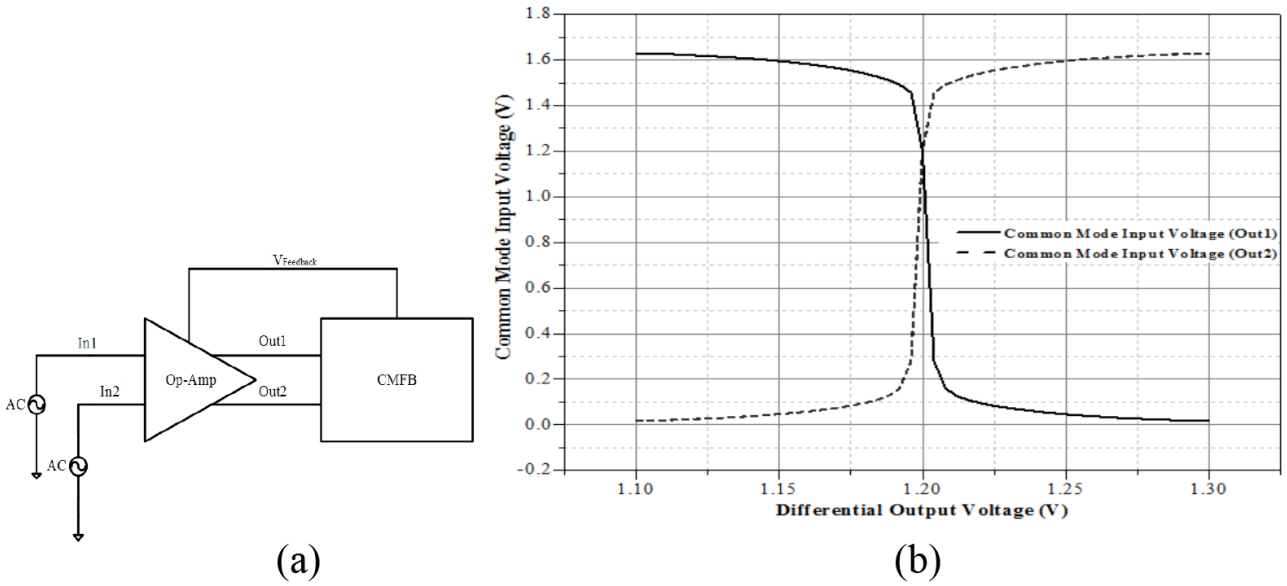

Figure 13. a) Test setup of the CMFB circuit, b) CMFB circuit performance result.

The implementation results of the folded-cascode op-amp with the CMFB circuit are demonstrated by comparing the simulation results with the process information in Table 6.

Table 6. Process information.

No.	Vin	B1	B0	DAC output	Residue output
1.	Vin > Vref/4	1	0	+Vref	2Vin – Vref
2.	−Vref/4 < Vin < Vref/4	0	1	0	2Vin
3.	Vin < −Vref/4	0	0	−Vref	2Vin + Vref

The comparison process is performed by feeding the comparator with the differentiated voltage (v_{diff}) of ($v_{diff} = v_{in+} - v_{in-}$), where the value of V_{in} is between the range of -1.8 V to 1.8 V. The v_{diff} is later compared to $-V_{ref}/4$ in order to perform the 2-bit signal of COM1 and COM0 (Figure 7). However, the value of V_{ref} should be noted as 1.2 V. The simulation results are presented in Figure 14 and are then compared in the same figure to the ideal case. From the transfer function, the switch value between the positive and negative value is generated at an input difference of +0.3 V and -0.3 V. The data of output voltage are only sampled at increment or decrement values of ± 0.1 V at both inputs of Vin+ and Vin–. However, in order to perform the value transition at ± 0.3 V, the value sampling should be small enough to be close to ± 0.3 V (e.g., ± 0.32 V and ± 0.28 V). Therefore, this integration is applied in order to ensure that the folded cascode and the CMFB circuit can provide a comprehensive design for high speed and high gain of the pipeline ADC.

Table 7 summarizes the performance comparison of the op-amp circuit with previously published work on pipeline ADC applications. According to [12], an op-amp circuit with a folded-regulated cascode topology obtains 90.39 dB of DC gain along 700.7 MHz UGB and was utilized in a 10-bit pipeline ADC. However, higher gain is not required for a 10-bit pipeline ADC; thus, the op-amp circuit shows higher power consumption at 3.24 mW. In [15], an op-amp circuit was utilized in a 14-bit ADC application with folded-cascode topology. The op-amp circuit achieved 92.0 dB of DC gain with 1600.0 MHz of UGB, but the op-amp circuit shows

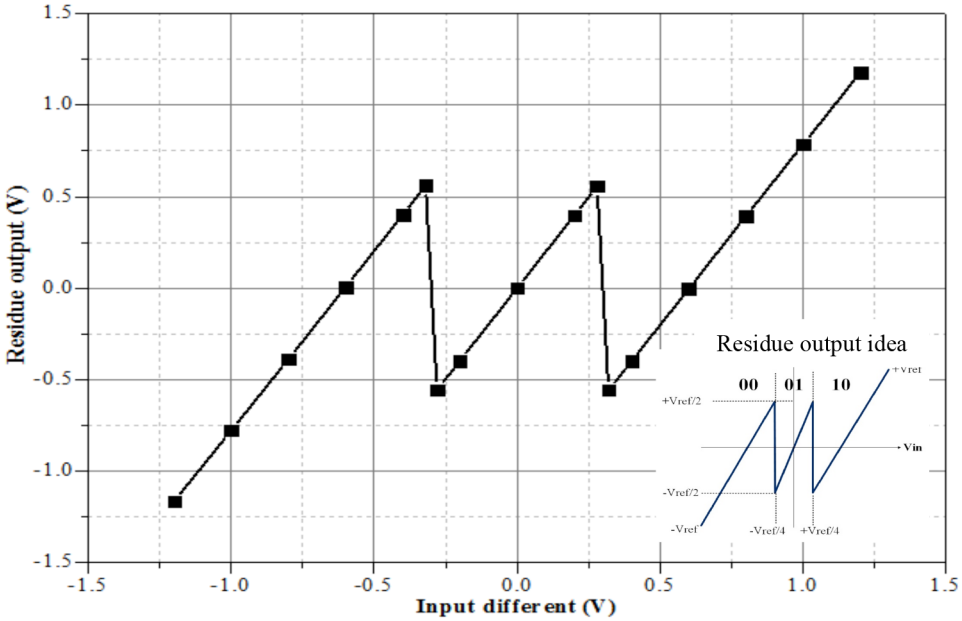

Figure 14. Transfer function of residue output.

higher power consumption compared to [12], which noted 7.8 mW with a voltage supply of 1.8 V. The gain bandwidth results mentioned in [12–16] are higher than those of the proposed work due to the higher gain and because the researcher's design targeted higher resolution (bits). As observed in this work, the proposed op-amp circuit demonstrates the lowest power consumption compared to previous works with comparable parameters. In addition, the proposed op-amp circuit was implemented in a 10-bit pipeline ADC.

Table 7. Comparison performance of the proposed folded-cascode op-amp with previously published work.

References	[12]	[13]	[14]	[15]	[16]	This work
Technology (μm)	0.18	0.13	0.13	0.18	0.18	0.13
Voltage supply (V)	1.8	3.0	1.8	1.8	1.8	1.8
DC gain (dB)	90.39	94.9	91.5	92.0	103.94	64.5
Unity gain bandwidth (MHz)	700.7	414	714.5	1600.0	344.5	695.1
Phase margin (°)	63.85	82.3	62.0	76.0	61.06	68.4
Slew rate (V/μs)	N/A	N/A	N/A	N/A	2883.5	22.6
Settling time (ns)	N/A	6.17	40.0	7.0	N/A	72.4
Power consumption (MW)	3.24	11.0	9.0	7.8	1.0	0.14
Load capacitance (pF)	0.5	2.0	7.5	0.15	1.0	1.0
Resolution (bits)	10	12	14	14	3	10

3. Conclusion

This work describes the design of an op-amp circuit using a folded-cascode topology with NMOS input types for pipeline ADC applications. The proposed op-amp with a designed common-mode feedback is implemented in 0.13-μm CMOS technology. The simulated results show that the op-amp achieves 64.5 dB of gain, 695.1 MHz of UGB, and a phase margin of 68.4° at the 1-pF load capacitor. In addition, the op-amp also provides a 22.6 μs/V slew rate with a settling time of 72.4 ns and also shows less power consumption at 0.14 mW at a voltage

supply of 1.8 V. A common-mode feedback circuit with a double-detection structure is able to fix the output voltage generated by the op-amp at 1.2 V for a constant feedback voltage of 1.3 V. Therefore, the proposed folded-cascode op-amp with CMFB can be used in pipeline ADC applications.

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