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Design optimization of a Ćuk DC/DC converter based on reliability constraints

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Abstract: Recently, power electronic converters have widely been used in various applications. This has led to concerns about the reliability of power converters and, as a result, their optimal design has attracted a lot of attention. However, the reliability-based optimal design of the Ćuk DC-DC converter has not yet been studied. A new methodology is presented here for the optimal design of the Ćuk converter based on reliability constraints. In this study, the converter is designed to minimize power losses in order to maximize the mean time to failure of the converter. A genetic algorithm is used as the optimization technique, resulting in the optimal duty cycle and switching frequency of the converter. Other parameters of the converter are selected to satisfy the desired electrical constraints. Finally, three scenarios along with simulation results are presented to verify the feasibility of the proposed design methodology. In addition, an experimental prototype is implemented to validate the proper operation of the converter.

Key words: Reliability, Ćuk, DC/DC converter, design optimization

1. Introduction

Much attention has recently been paid to the reliability improvement of power electronic devices. The apparent technical requirements of military forces and space programs have resulted in a need for highly improved reliability in machinery components [1]. Expansive implementation of power electronic converters in various applications including military and space programs has led to reliability concerns about power converters. The reliability issue has generated more and more concern in many sectors ranging from industrial fields to research institutes.

The ability of an item to operate a desired function under various conditions for a specified duration of time is defined as reliability, which is often measured by the probability of failure, by the frequency of failure, or in terms of availability. Failure prevention is the basic goal in reliability analysis of power converters. The reliability issue in power electronics can be observed in many ways such as the high-power density product trend or the emergence of high-temperature and reliability-critical applications, which include an increase in electrical and electronic complexity and testing of resource-consuming verification. In this paper, the aim is to improve the reliability of a power electronic device, namely the Ćuk converter, through a proposed reliability-oriented design method.

Lower input current ripple, easy implementation of transformer isolation, lower electromagnetic interference (EMI), the capability to operate in either step-up or step-down mode, and natural protection against the

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inrush current, occurring at start-up or overload, are the main advantages of the Ćuk converter in different applications mentioned in [2–4]. Unlike the single-ended primary inductor (SEPIC) converter, the Ćuk converter contains both continuous input and output currents with a low current ripple. Consequently, the Ćuk converter seems very suitable for applications where continuous input and output currents are required. Ćuk converters are widely used in many applications such as renewable power systems [5–7], battery chargers for electrical vehicles [8,9], communication systems [10,11], and light-emitting diodes and electrical motor drivers [12–14]. As a result, many investigations have focused on Ćuk converters. Several research topics related to the Ćuk converter have previously been considered, including its topology, modeling, control, and efficiency analysis.

A Ćuk converter with power factor correction (PFC) capability feeding a brushless DC (BLDC) motor drive was studied in [15–17]. The converter that was studied can operate over a wide range of speeds, with a unity power factor at AC mains a cost-effective solution for low-power applications. Performance of the PFC Ćuk converter is evaluated in four different operating conditions of discontinuous and continuous conduction mode (CCM), and a comparison is then made to select the best operation mode.

A combination of SEPIC and Ćuk converters was proposed in [18] for DC bipolar networks. Since the SEPIC and Ćuk converters have the same instantaneous duty cycle, the switching node is shared in the combined topology. The key benefit of the combined topology is that synchronization of various switches is not required, and the control terminal is connected to ground, making the design of the gate drive simple.

In [19], three topologies of bridgeless Ćuk converters used as PFC recti?ers were proposed. The proposed topologies were designed to operate in discontinuous conduction mode (DCM) to achieve a nearly unity power factor and low total harmonic distortion of the input current. Zero-current turn-on in the power switches, zero-current turn-off in the output diode, and a simple control circuit are some of the other benefits that the DCM operation gives to the converters. The proposed converters are compared based on ef?ciency, component count, harmonics, gain capability, and driver circuit.

Due to the advantages of the Ćuk converter and its various applications, the reliability of the converter should be improved in some critical ways [20]. Typically, the redundancy method is used to improve the reliability of power converters, and this increases the size and cost of the power converters. However, other methods can also be considered to overcome this issue. The proper design of a power converter and its controller will result in operational benefits, but a faulty design may cause serious stress on and reduce the lifetime of a power electronics device. Therefore, a reliability-oriented design will help the power converter improve its endurance.

The design of a power converter consists of the selection of the proper inductances, capacitors, power switches, diodes, duty cycles, and switching frequency for the desired operation conditions. Several methods were used to design power converters in [21,22].

The research in [23] introduced a complementary gate signal control to get high power efficiency and improve DCM operation EMI noise. On the basis of this control scheme, a 3rd-order model of a bidirectional DC/DC converter for battery charging was proposed, developed, and investigated. A unified controller, which results in smooth mode transition, was designed based on the model. In [24], DC/DC insulated converters were designed using an active voltage clamp. The presented design optimization is for achieving zero-voltage switching modes in the whole operating range, which leads to the reduction of power losses. Moreover, the proposed optimization is applicable for DC/DC Ćuk converters. The use of an active voltage clamp in insulated

DC/DC converters provides several advantages such as limiting the voltage stress due to transformer leakage inductance, reducing commutation losses, and increasing switching frequency.

An optimization among the different input voltages and different core materials of different saturation flux densities was performed in [25] to achieve the minimum weight of a DC/DC Ćuk converter. Therefore, converter weight and power loss were evaluated as a function of the input voltage and flux density. In [26], a new design for sliding-mode controllers was presented for Ćuk converters. The proposed approach has major benefits such as simplicity of control implementation, large-signal stability, small overshoots of all state variables, a short settling time in any operating condition, and transfer capacitor reduction, which enables the converter to not require any decoupling of input and output stages. A new specific control circuit was presented for the DC/DC Ćuk converter in [27]. The authors in this paper analyzed the applied signals to the gate driver of the power MOSFET and subsequently designed a new control system that lets the DC/DC Ćuk converter operate in an ideal manner. In [28], an overall design of a Ćuk DC/DC converter was presented. The example is intended to extend and demonstrate the application of the optimization-enabled simulation in the design of switching converters and propose methods for the designing of suitable objective functions, scaling of the parameters, and imposing of constraints.

However, the reliability of the converter has not been considered in the design procedures of the above-mentioned studies. Heuristic algorithms, on the other hand, can be used when there are several parameters to be optimized [29]. In addition, the controller design might affect the operation of the converter. The converter should operate differently in various load conditions. It is important to note here that some converter parameters, such as capacitors and inductances, are not changeable after implementation. However, the duty cycles (driving signals) of the power switches and the switching frequency might differ during the operation of the converter.

In different load conditions, two variables, the duty cycles (driving signals) of the power switches and the switching frequency, can be optimized offline. The data results can then be used by the controller to improve the converter. In this case, the objective function during optimization will be the reliability or the desired lifetime of the converter.

To the authors' knowledge, to date there has been no research conducted on the reliability analysis or reliability optimization of the Ćuk DC/DC converter. In this study, a new design methodology is proposed to optimize the reliability of the Ćuk converter.

2. Methodology

The methodology used in this study to optimize the reliability of a converter is divided into 7 steps:

1) Calculating the circuit MTTF equation based on the failure rate of each component in the circuit. Each component in the circuit has a specific failure rate that affects the total reliability of the converter. In this step, the MTTF equation of the converter should be calculated by studying these effects. It should be noted that in some topologies, it is not necessary to analyze the effects of all components because some of them are reliable enough and work accurately enough during the desired MTTF time.

2) Evaluating the failure rate of each component (λ), based on its quality and also by considering the environmental conditions of the experiment. Failure rates must be calculated in order to do the reliability analysis of power electronic devices. At this step, the failure rate of each component is calculated and then a detailed analysis is done on the parameters and stress factors that affect the failure rate. According to

the 217Plus reliability prediction model [30], the failure rate equations of switches, diodes, and capacitors are expressed in Table 1.

Table 1. Failure rate equations of the electrical components.

Capacitor	$\lambda_C = \pi_G\pi_C(\lambda_{OB}\pi_{DCO}\pi_{TO}\pi_S + \lambda_{EB}\pi_{DCN}\pi_{TE} + \lambda_{TCB}\pi_{CR}\pi_{DT}) + \lambda_{SJB}\pi_{SJDT} + \lambda_{EOS}$
Diode	$\lambda_D = \pi_G(\lambda_{OB}\pi_{DCO}\pi_{TO}\pi_S + \lambda_{EB}\pi_{DCN}\pi_{TE} + \lambda_{TCB}\pi_{CR}\pi_{DT}) + \lambda_{SJB}\pi_{SJDT} + \lambda_{EOS}$
Switch	$\lambda_S = \pi_G(\lambda_{OB}\pi_{DCO}\pi_{TO}\pi_S + \lambda_{EB}\pi_{DCN}\pi_{TE} + \lambda_{TCB}\pi_{CR}\pi_{DT}) + \lambda_{IND}$

It can be concluded from Table 1 that the failure rate of a component is always affected by three important factors: the quality factor, the environmental stress factor, and the temperature stress factor. The quality factor is related to the materials used in the construction of a component. Frequently, this is determined by the manufacturer of the device. Another important factor is the environmental stress factor, which is dependent on environmental conditions of the place where the device is used. The most important factor that affects λ is the temperature stress factors, which indicate the effect of temperature on all components. The reason that the temperature factor is most important is that in some components like diodes and switches, the temperature factor is affected not only by temperature but also by the device's power losses. Therefore, the power losses of the device should be considered in the calculation of its failure rate.

3) Calculating the power losses of the components such as switches and diodes because their power losses affect their failure rates and, in the end, affect total reliability. The variable electrical parameters of the circuit (duty cycle and switching frequency), which affect total reliability, should also be determined. Optimization will be done on these parameters, and the final value of the components will be computed by using said parameters.

4) Calculating equations indicating the value of each component in the circuit based on the variable parameters that are determined in step 3.

5) Setting the MTTF. The MTTF should be considered desirable.

6) Optimizing variable electrical parameters of the circuit with the genetic algorithm for the given MTTF in step 5. In this step, the genetic algorithm is applied to select the key parameters of the DC/DC Ćuk converter. The key variables of the converter here are the duty cycle and the switching frequency. In various conditions, the optimal duty cycles and the switching frequencies may be different. Therefore, these variables can be calculated in several desired conditions. Other parameters of the DC/DC converter, such as the inductances and the capacitors, are chosen to satisfy the defined constraints.

7) Calculating circuit components by replacing the optimized parameters achieved from step 6 in the equations that were calculated in step 4. Figure 1 shows the flowchart of the proposed methodology. In the next section, a design example will better illustrate the methodology.

3. Design example

The strategy described in Section 2 is exemplified by the DC/DC Ćuk converter shown in Figure 2.

1) Calculating the MTTF equation:

At first, it is assumed that the inductors are reliable enough and there is no need to calculate them in the reliability of the converter. Since the converter is not very complicated, it is clear that if one of the components

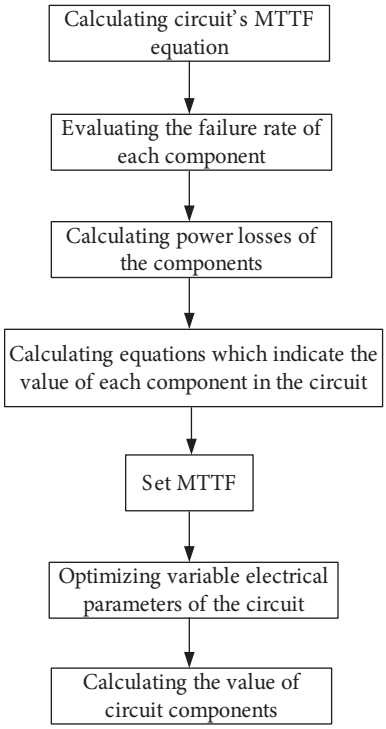


Figure 1. Flowchart of the proposed methodology.

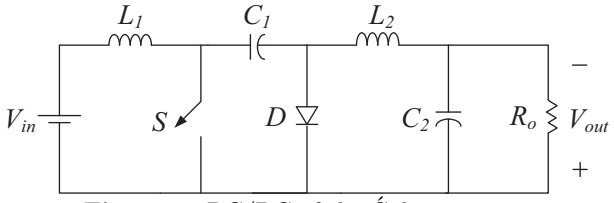


Figure 2. DC/DC of the Ćuk converter.

fails to function, the total performance of the converter will not have the expected performance, so the MTTF equation of the converter is as follows:

$$MTTF = \frac{1}{\lambda_t} \tag{1}$$

where λ_t is the sum of the component failure rates used in the topology, which is expressed by:

$$\lambda_t = \lambda_S + \lambda_D + \lambda_{C_i} + \lambda_{C_o} \tag{2}$$

2) Evaluating and analyzing the failure rate equations:

As previously mentioned, we need the failure rate equations of the components in the last step. According to Table 1, in order to calculate the failure rate equations, the λ and π_T factors have to be evaluated. In this DC/DC converter, aluminum electrolytic capacitors are used. In addition, the diode and switch types are MUR1560 and MOSFET IRF740, respectively. Therefore, the value of the λ parameters (λ_{OB}, λ_{EB}, λ_{TCB}, and λ_{IND}) in Table 1 can be easily found with the 217Plus reliability prediction model.

It should be noted that all stress factors except temperature stress factors (π_{TO}, π_{TE}, π_{DT}, and π_{SJDT}) are assumed as 1 in this calculation. The π_T or the temperature factors of the components can be calculated with the expressions listed in Table 2, where T_R is the junction temperature rise above the ambient operating temperature (T_{AO}). Therefore, the junction temperature is equal to:

Table 2. Temperature factors.

π_T	π_{TO}	π_{TE}	π_{DT}	π_{SJDT}
Capacitor	$\exp[\frac{-Ea_{op}}{8.617*10^{-5}}*(\frac{1}{T_{AO}+273}-\frac{1}{298})]$	$\exp[\frac{-Ea_{nonop}}{8.617*10^{-5}}*(\frac{1}{T_{AE}+273}-\frac{1}{298})]$	$(\frac{T_{AO}-T_{AE}}{DT_1})^2$	$(\frac{T_{AO}-T_{AE}}{44})^{2.26}$
Diode & Switch	$\exp[\frac{-Ea_{op}}{8.617*10^{-5}}*(\frac{1}{T_{AO}+T_R+273}-\frac{1}{298})]$	$\exp[\frac{-Ea_{nonop}}{8.617*10^{-5}}*(\frac{1}{T_{AE}+273}-\frac{1}{298})]$	$(\frac{T_{AO}+T_R-T_{AE}}{DT_1})^2$	$(\frac{T_{AO}+T_R-T_{AE}}{44})^{2.26}$

$$T_j = T_{AO} + T_R \tag{3}$$

The parameter T_R can be calculated as:

$$T_R = \theta_{JA} P_{Loss} \tag{4}$$

where θ_{JA} is the junction-to-ambient thermal temperature and P_{Loss} is the dissipated power by the diode:

$$T_R = \theta_{JC} P_{Loss} \tag{5}$$

where θ_{JC} is the junction-to-case thermal temperature. If this option is used, T_{AO} should be replaced by T_C, the component case temperature, in the above equation for π_{TO}. The first formula will be used, and the value of θ_{JA}, the junction-to-ambient temperature, is shown in Table 3. The value of T_{AO}, the ambient temperature, is assumed to be 25 °C both for diode and switch in this case study.

Table 3. Junction-to-ambient temperature.

Component	θ_{JA}
Diode (MUR1560)	73
Switch (IRF740)	62

Finally, it can be observed in Eqs. (4) and (5) that T_R is related to the dissipated power. Thus, it can be concluded that the power loss of the diode and switch should be evaluated for the calculation of their failure rate. Power loss analysis of a converter is important for the reliability analysis of a power electronics device.

3) Calculating power loss:

For calculation of the power losses of the DC/DC Ćuk converter, Figure 3 is considered as an equivalent circuit of the converter. As seen in Figure 3, only the power losses of the switch and diode will be calculated. The evaluation of power loss in this converter is done in CCM, so it is assumed that the inductor currents are ripple-free.

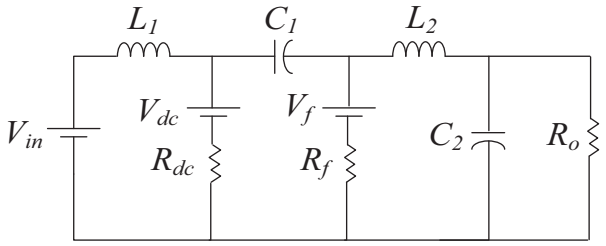


Figure 3. Equivalent circuit of the DC/DC Ćuk converter.

a) Diode: In Figure 3, R_f and V_f are the forward resistance and threshold voltage of the diode, respectively. Assuming ripple-free current for inductors, the diode current can be approximated by:

$$\begin{aligned} i_D &= \begin{cases} 0 & 0 < t < DT_S \\ I_o + I_{in} & DT_S < t < T_S \end{cases} \\ &= \begin{cases} 0 & 0 < t < DT_S \\ \frac{I_o}{1-D} & DT_S < t < T_S \end{cases} \end{aligned} \tag{6}$$

The average and RMS values of the diode current are:

$$\begin{aligned} I_{D_{ave}} &= \tfrac{1}{T_s}\int_0^{T_S} i_D dt \\ &= \tfrac{1}{T_s}\int_{DT_S}^{T_S} \tfrac{I_O}{1-D} dt = I_O \end{aligned} \tag{7}$$

$$\begin{aligned} i_{Drms} &= \sqrt{\tfrac{1}{T_s}\int_0^{T_S} i_D^2 dt} \\ &= \sqrt{\tfrac{1}{T_s}\int_{DT_S}^{T_S} \left(\tfrac{I_O}{1-D}\right)^2 dt} = \tfrac{I_O}{\sqrt{1-D}} \end{aligned} \tag{8}$$

The total power loss in diode is then evaluated by:

$$p_{Loss_{Diode}} = p_{Loss_{R\,f}} + p_{Loss_{V\,f}} \tag{9}$$

$$\begin{aligned} p_{Loss_{Diode}} &= R_f i^2_{D_{rms}} + V_f I_D \\ &= (\tfrac{R_f}{R_o(1-D)} + \tfrac{V_f}{V_o}) P_o \end{aligned} \tag{10}$$

b) Switch: According to [1], the power loss of the switch is divided into two parts: conduction and switching losses. The total power loss of switch is equal to:

$$p_{Loss_{Switch}} = p_{Loss_{Conduction}} + p_{Loss_{Switching}} \tag{11}$$

$$\begin{aligned} p_{Loss_{Switch}} = \; & [u_{ds0}.I_{Sav} + r_{ds}.i^2_{Srms}] \\ & + \tfrac{1}{2} u_{ds} I_{Sav} f_S \left[t_{c(on)} + t_{c(off)}\right] \end{aligned} \tag{12}$$

where u_{ds0} and u_{ds} represent the power switch on-state and off-state zero-current drain-source voltages, and R_{ds} is the drain-source on-state resistance. The switching frequency is f_s, and $t_{c(on)}$ and $t_{c(off)}$ are the power switch turn-on and turn-off transition times, respectively (Figure 4). It should also be noted that u_{ds} is the power switch drain-source voltage when the switch is off. As seen in Figure 2, it is obvious that this voltage is equal to V_{ci} and is calculated as:

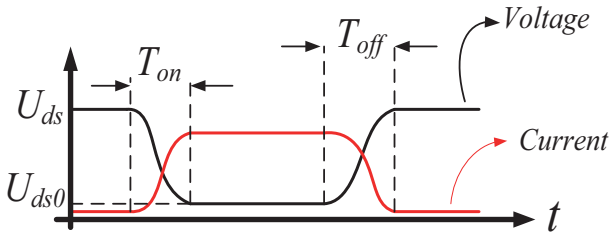


Figure 4. Switching time of the power switch.

$$u_{ds} = V_{ci} = \frac{V_o}{D} \tag{13}$$

The switch current with the aforementioned assumption can be approximated by:

$$\begin{aligned} i_S &= \begin{cases} I_o + I_{in} & 0 < t < DT_S \\ 0 & DT_S < t < T_S \end{cases} \\ &= \begin{cases} \frac{I_o}{1-D} & 0 < t < DT_S \\ 0 & DT_S < t < T_S \end{cases} \end{aligned} \tag{14}$$

I_{Save} and I_{Srms} are the average and RMS values of the switch current expressed as follows:

$$\begin{aligned} I_S &= \tfrac{1}{T_S}\int_0^{T_S} i_S dt \\ &= \tfrac{1}{T_S}\int_0^{DT_S} \tfrac{I_O}{1-D} dt = \tfrac{D}{1-D} I_O \end{aligned} \tag{15}$$

$$\begin{aligned} i_{Srms} &= \sqrt{\tfrac{1}{T_S}\int_0^{T_S} i_S^2 dt} \\ &= \sqrt{\tfrac{1}{T_S}\int_0^{DT_S} \left(\tfrac{I_O}{1-D}\right)^2 dt} = \tfrac{\sqrt{D}}{1-D} I_O \end{aligned} \tag{16}$$

For the conduction and switching losses, we have:

$$P_{conduction} = \frac{D}{(1-D)}\left(\frac{r_{ds}}{R_o(1-D)} + \frac{V_{dso}}{V_o}\right)P_o \tag{17}$$

$$p_{switching} = \frac{D^2}{2(1-D)}(T_{C_{on}} + T_{C_{off}}) f_s P_o \tag{18}$$

At the end, the total power loss on a power MOSFET can be expressed by:

$$\begin{aligned} P_{Loss_{switch}} &= \tfrac{D}{(1-D)}\left(\tfrac{r_{ds}}{R_o(1-D)} + \tfrac{V_{dso}}{V_o}\right)P_o \\ &+ \tfrac{D^2}{2(1-D)}(T_{C_{on}} + T_{C_{off}}) f_s P_o \end{aligned} \tag{19}$$

It is obvious from the power loss equations (Eq. (10) and Eq. (19)) that the switching frequency (f_s) and duty cycle (D) are acting as variable parameters, so they should be controlled and optimized for the given MTTF in the following steps.

4) Evaluating equations that indicate the value of components in the circuit:

In this step, equations related to the component values should be calculated based on the variable parameters D and f_s; therefore, they are listed in Table 4. As seen in Table 4, these equations consist of D, f_s, load resistance, and the constants $\alpha, \beta, \delta, \eta$.

Table 4. Equations of component values.

Component	Equation	Ripple
L_i	$(1-D)^2 R_O * (f_s D\alpha)^{-1}$	$\alpha = \frac{\Delta I_{Li}}{I_{in}}$
L_o	$(1-D) R_o * (f_s \beta)^{-1}$	$\beta = \frac{\Delta I_{Lo}}{I_o}$
C_i	$D * (R_o f_s \eta)^{-1}$	$\eta = \frac{\Delta V_{ci}}{V_O}$
C_o	$\beta * (8 f_s R_o \delta)^{-1}$	$\delta = \frac{\Delta V_{co}}{V_O}$

As mentioned before, D and f_s are the variable parameters, R_o is the load resistance, and $\alpha, \beta, \delta, \eta$ are the ripple percentages. In this study, the maximum inductor current ripple is chosen to be equal to 10% of maximum inductor current. Similarly, the maximum capacitor voltage ripple is chosen to be equal to 10% of maximum capacitor voltage. Therefore, these constants are assumed to be 10% in this paper, except in the 3rd scenario that will be described later. These equations are calculated by using the inductor currents and capacitor voltages.

5) Setting the MTTF:

The selected MTTF is 7 years or 61,325 h.

6) and 7) Optimizing variable electrical parameters and calculating the values of circuit components

In these steps, the variable parameters should be optimized for the desired MTTF and optimal point of the DC/DC converter. Furthermore, by substituting these optimized variable parameters in the equations that were evaluated in step 4, the values of circuit components should be calculated.

In this paper, MATLAB software is used to simulate the optimization process. In order to verify the validity of the proposed methodology, three scenarios are studied, each of which has five missions. They will be described in the following section.

3.1. First scenario

In the first scenario, it is assumed that the ripple coefficients and load resistance are constant. For different values of injected power to the load, D and f_s are optimized in the MATLAB simulation software. Finally, by applying these results to the equations found in the previous section, the proposed DC/DC converter is designed. Accordingly, in this scenario $\alpha, \beta, \delta, \eta$ and load resistance are assumed as 10% and $10\,\Omega$, respectively. For the different values of injected power shown in Table 5, separate simulations are then performed. Therefore, the optimized values of variable parameters D and f_s are expressed in Table 5. Moreover, as shown in Table

6, the components of the Ćuk converter are designed for the desired MTTF by using the optimized variable parameters seen in Table 5.

Table 5. Optimized variable parameters for the first scenario.

$_{Po}$	f_s	D
50 W	2.148e+004	0.648
70 W	2.381e+004	0.518
90 W	1.740e+004	0.389
110 W	2.111e+004	0.259
130 W	1.488e+004	0.125

Table 6. Values of circuit components for the first scenario.

P_o	L_i	L_o	C_i	C_o
50 W	890 μH	1.64 mH	30 μF	580 nF
70 W	1.88 mH	2.02 mH	21.62 μF	526 nF
90 W	5.51 mH	3.51 mH	22.1 μF	718 nF
110 W	10.04 mH	3.51 mH	14.6 μF	592 nF
130 W	41.16 mH	5.88 mH	8 μF	840 nF

3.2. Second scenario

In the second scenario, for the constant values of injected power and ripple coefficients, along with the use of different types of loads, the DC-DC converter will be designed. In the other words, based on the load, the converter is designed assuming the MTTF.

Therefore, $\alpha, \beta, \delta, \eta$ and injected power are considered as 10% and 90 W, respectively. Simulation results are then provided for the different resistive loads listed in Table 7, as well as the optimized values of variable parameters. In addition, by substituting the optimized values of D and f_s, indicated in Table 7, in the equations that were evaluated in step 4, the values of the components for the Ćuk converter are calculated in Table 8.

Table 7. Optimized variable parameters for the second scenario.

$_{Ro}$	f_s	D
10 Ω	1.911e+004	0.389
15 Ω	1.789e+004	0.583
20 Ω	2.343e+004	0.679
25 Ω	2.458e+004	0.736
30 Ω	1.691e+004	0.775

Table 8. Values of circuit components for the second scenario.

R_o	L_i	L_o	C_i	C_o
10 Ω	5.51 mH	3.51 mH	22.1 μF	718 nF
15 Ω	2.5 mH	3.5 mH	20 nF	466 nF
20 Ω	1.3 mH	2.74 mH	14 nF	267 nF
25 Ω	1 mH	3.9 mH	12 nF	203 nF
30 Ω	1.16 mH	4 mH	15 nF	246 nF

3.3. Third scenario

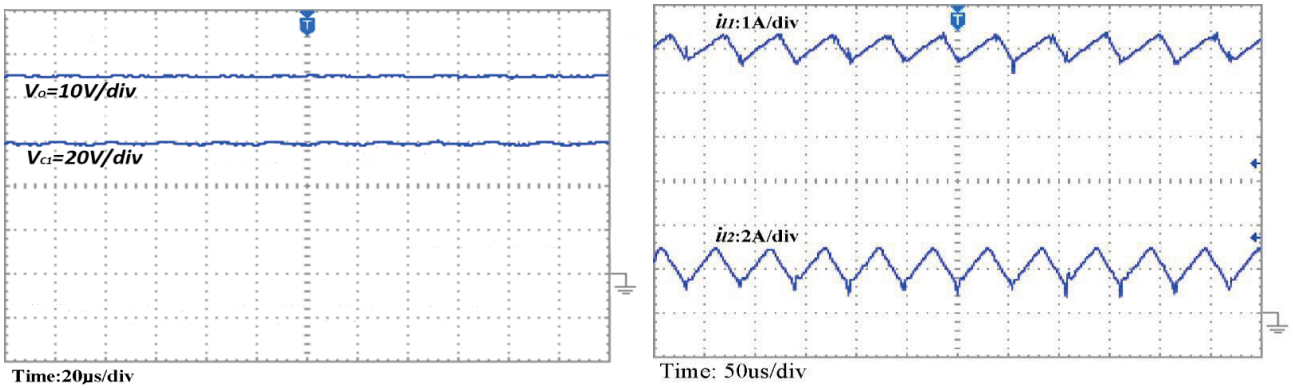
Finally, in the third scenario, for the same loads and feeding power with different values of ripple coefficients, the DC/DC converter can be designed. In this scenario, the injected power and load resistance are equal to 90 W and 10 Ω for all missions. Therefore, only the optimization results for the 90-W and 10-Ω load is required. As the component values have direct relationship with the ripple coefficients, the converter could be designed for the recommended ripple value for each mission (see Table 9). It should be noted that these coefficient values themselves could be different for each component, but for simplicity's sake they are assumed identical in each mission here.

Table 9. Values of circuit components for the third scenario.

$\alpha, \beta, \delta, \eta$	L_i	L_o	C_i	C_o
5%	11.02 mH	7.02 mH	44.2 μF	718 nF
10%	5.51 mH	3.51 mH	22.1 μF	718 nF
15%	3.67 mH	2.34 mH	14.7 μF	718 nF
20%	2.75 mH	1.75 mH	11.05 μF	718 nF

4. Experiment results

An experimental prototype is provided to validate the proper operation of the optimized Ćuk converter. The prototype is implemented to a fixed output power of 90 W. The value of resistive load for the experimented topology is selected as 25 Ω. Therefore, the components that are calculated in second scenario (Table 8) are used during the implementation. It is important to note here that the capacitors are selected at 10 nF and 200 nF. The input voltage is 15 V and the output voltage is 45 V. The experimental results are shown in Figure 5. The capacitor voltages and inductor currents are also shown in this figure. The experimental results validate a suitable operation of the converter. The reliability-based design of a power electronic device will satisfy all of the requirements of these devices.



(a) (b)

Figure 5. Experimented waveforms of the DC/DC Ćuk converter: a) the capacitor voltage waveforms and b) the inductor current waveforms.

5. Conclusion

With the increasing need for reliable power electronic devices, this paper presents a new methodology to optimize the reliability of the Ćuk DC/DC converter. In the proposed methodology, the power losses of the converter are minimized in order to maximize the MTTF of the converter. A genetic algorithm was implemented as the optimization technique, and the optimal duty cycle and switching frequency of the converter were found based on the reliability constraints. The capacitors, inductances, and other parameters of the converter were selected to satisfy the desired electrical constraints of the converter. Simulation and experimental results were presented to validate the feasibility of the proposed design methodology.

Nomenclature

λ_{OB}	Base failure rate, operating
λ_{EB}	Base failure rate, environmental
λ_{TCB}	Base failure rate, temperature cycling
λ_{SJB}	Base failure rate, solder joint
λ_{EOS}	Failure rate, electrical overstress
λ_b	Base failure rate
π_G	Reliability growth failure rate multiplier
π_C	Capacitance failure rate multiplier
π_{DCO}	Failure rate multiplier for duty cycle, operating
π_{TO}	Failure rate multiplier for temperature, operating
π_S	Failure rate multiplier for stress
π_{DCN}	Failure rate multiplier, duty cycle, nonoperating
π_{TE}	Failure rate multiplier, temperature–environmental
π_{CR}	Failure rate multiplier, cycling rate
π_{DT}	Failure rate multiplier, delta temperature
π_{SJDT}	Failure rate multiplier, solder joint delta temperature
π_T	Temperature factor
π_Q	Quality factor
π_E	Environmental factor
T_{AO}	Ambient temperature, operating (°C)
T_{AE}	Ambient temperature, nonoperating (°C)
DT_1	Constant
T_R	The component temperature rise above the ambient
T_{AO}	Operating temperature
T_j	Junction temperature
Ea_{op}	Activation energy, operating
Ea_{nonop}	Activation energy, nonoperating
θ_{JA}	Junction to ambient thermal temperature
θ_{JC}	Junction to case thermal temperature

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