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Significant insights into the operation of DC-link voltage control of a shunt active power filter using different control algorithms: a comparative study

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Abstract: A comparative study between a conventional DC-link voltage control algorithm (CDVCA) and a self-charging DC-link voltage control algorithm (SDVCA) is presented. It focuses on the principle operation of both algorithms and their impacts on the performance of a shunt active power filter (SAPF) operation. All analyses are based on the step response of DC-link voltages under different start-up times of the SAPF and different initial DC-link voltage values. Other considered parameters are the ripple factor (RP) of DC-link voltages, estimated and measured DC-link charging currents, and total harmonic distortion (THD) value of supply currents. Thus, this study provides new insights into the operation of DC-link voltage control using different control algorithms. According to the simulation results, the SAPF using the SDVCA has shown better performance than using the CDVCA. By using the SDVCA, the charging process of a DC-link capacitor starts almost instantaneously. Additionally, the overshoot, settling time, and RF of DC-link voltages are reduced. Other than that, THD values of supply currents are improved, by generating low ripple of estimated DC-link charging currents. Experimental validation of the SAPF using the SDVCA is also presented.

Key words: Conventional DC-link voltage control, harmonic compensation, self-charging DC-link voltage control, shunt active power filter

1. Introduction

Shunt active power filters (SAPFs) are globally accredited as the most effective tools in suppressing multiple harmonic currents simultaneously. These filters are used to inject specific compensation currents for harmonic current cancellation. Consequently, the shape of distorted supply currents can be reformed to be fully sinusoidal wave shapes. The compensated supply currents consist of almost fundamental components.

The operation of SAPFs depends fully on their control algorithms for current control and DC-link voltage control. However, the current research trends are more concerned with designing or improving current controllers (i.e. fuzzy-adaptive hysteresis controller [1]), voltage controllers (i.e. type-2 fuzzy-proportional-derivative (fuzzy-PD) controller [2], approximated fuzzy-PD controller [3], and proportional-integral (PI) controller with particle swam optimization [4]), and developing new methods of generating SAPFs' reference currents (i.e. ANN-based phase locking [5], ANN based p-q theory [6], and Fryze current computation method [7]). Therefore, this work

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only concentrates on the principle operation, advantages, and disadvantages of different DC-link voltage control algorithms.

DC-link voltage control is normally conducted using a simple control algorithm with a voltage controller such as a PI controller [8] and fuzzy-PD controller [9]. Frequently, a control signal of any voltage controller can be defined using two different variables. First, it is assumed as the peak amplitude of instantaneous SAPF reference currents [10,11]. Second, it is defined as the peak amplitude of instantaneous DC-link charging currents [12–15]. Other than that, the control signal can also be presumed as the required instantaneous power for charging DC-link capacitors of SAPFs [4,7].

Despite using different definitions of the control signal, all the aforementioned algorithms are generally designed based on an assumption approach. According to [7,10,15], all the above-mentioned variables are assumed based on the type of reference current generation algorithm used by SAPFs. To the best of our knowledge, there is no explicit study on the effect of using different voltage control algorithms on the quality of DC-link voltages (in terms of ripple factor (RF) values). Moreover, there is no explanation on how voltage control algorithms can affect the performance of SAPFs. Therefore, this study will examine those concerns. Moreover, since the voltage control based DC-link charging current estimation algorithm is preferable to the other 2 algorithms, this work focuses on that particular algorithm only. It will be referred to as a conventional DC-link voltage control algorithm (CDVCA).

Another DC-link voltage control algorithm, namely a self-charging DC-link voltage control algorithm (SDVCA), is presented in [16–18]. Unlike the CDVCA, the control signal of the SDVCA's voltage controller is used in a self-charging equation for calculating the peak amplitude of instantaneous DC-link charging currents. However, most researchers are less familiar with the SDVCA; there is no exposure on the benefit of using the algorithm. Therefore, it limits the SDVCA implementation.

In the present work, a comparative study between the CDVCA and the SDVCA is conducted. It focuses on the step response of DC-link voltages under different start-up times of a 3-phase 3-wire SAPF. Other parameters such as RF of DC-link voltages, estimated and measured DC-link charging currents, and THD value of supply currents are analyzed further. Furthermore, this work provides detailed explanations on both control algorithms and their impacts on the performance of SAPFs.

This paper is organized in 5 sections. Section 2 explains 2 types of DC-link voltage control algorithms, Section 3 contains the simulation results, Section 4 presents the experimental results, and Section 5 concludes all contributions of the work.

2. DC-link voltage control algorithms

Commonly, a SAPF comprises a single-level or multilevel bridge inverter with 1 or 2 DC-link capacitors. In order to work properly, the SAPF must be able to maintain constant DC-link voltage for the whole of its operation. Otherwise, DC-link voltages may increase and exceed the rated voltage of DC-link capacitors. In this work, a 3-phase 3-wire voltage source inverter (VSI) with a single DC-link capacitor is employed as a SAPF. The SAPF and its control algorithm are shown in Figure 1.

A constant DC-link voltage can be achieved by regulating the energy of DC-link capacitors. The energy w can be represented as

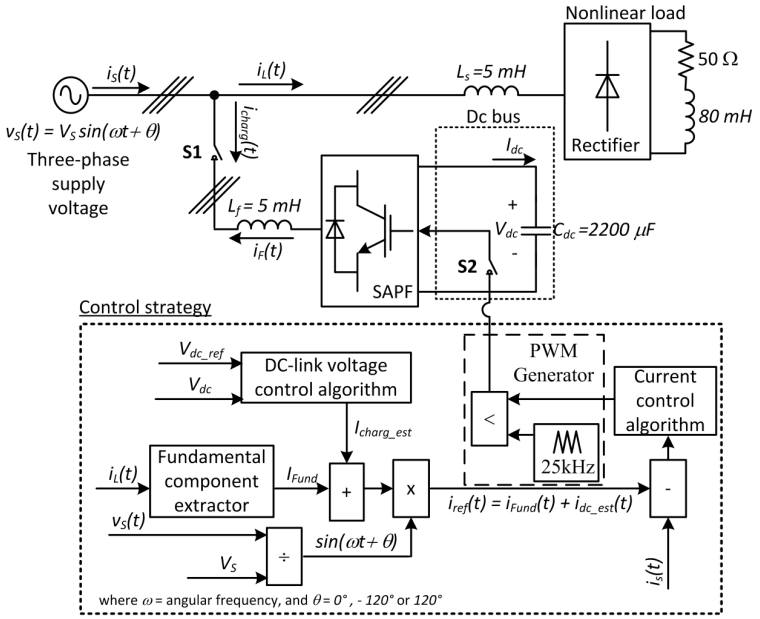

Figure 1. SAPF with the proposed control algorithm.

$$w = \int_{\tau=-\infty}^{\tau=t} P(\tau)d\tau = c_{dc}\int_{\tau=-\infty}^{\tau=t} V_{dc}(\tau)\frac{dV_{dc}(\tau)}{d\tau}d\tau = \frac{C_{dc}}{2}V_{dc}^2$$
$$= 3\int_{\tau=-\infty}^{\tau=t} v_S(\tau) i_{charg}(\tau)\, d\tau, \tag{1}$$

where P is the instantaneous power, c_{dc} is the capacitance value of DC-link capacitors, V_{dc} is the DC-link voltage, $v_S(t)$ is the instantaneous supply voltage, and $i_{charg}(t)$ is the instantaneous SAPF charging current. Since power systems supply fixed supply voltages, P can be regulated by adjusting $i_{charg}(t)$. Thus, both the CDVCA and the SDVCA are designed for estimating the peak amplitude of $i_{charg}(t)$.

According to Figure 1, the summation of the estimated amplitude I_{charg_est} of $i_{charg}(t)$ and the extracted fundamental component I_{Fund} of the instantaneous load current $i_L(t)$ represents the instantaneous reference current $i_{ref}(t)$ of the SAPF. In this work, I_{Fund} is extracted using an ANN-based harmonic extraction algorithm [16,17].

2.1. Conventional DC-link voltage control algorithm

Figure 2 shows a block diagram of the CDVCA. In this algorithm, a voltage controller is used for minimizing the error signal $e_c(t)$ between the measured V_{dc} and the reference DC-link voltage V_{dc_ref}. Then the control signal $\delta e_c(t)$ is assumed as I_{charg_est} [1,2,19,20]. In this work, a PI controller is utilized as the voltage controller. Therefore, I_{dc_est} can be represented as

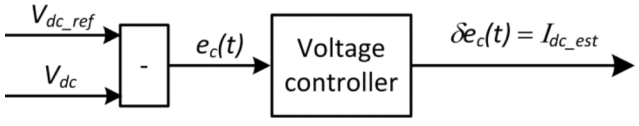

Figure 2. SAPF with the proposed control algorithm.

$$I_{charg\_est} = \delta e_c(t) = K_p e_c(t) + K_i \int_{\tau=-\infty}^{\tau=t} e_c(\tau) d\tau$$
$$= K_p (V_{dc\_ref} - V_{dc}) + K_i \int_{\tau=-\infty}^{\tau=t} (V_{dc\_ref} - V_{dc}) d\tau, \quad (2)$$

where K_p is the proportional gain and K_i is the integral gain of the PI controller.

2.2. Self-charging DC-link voltage control algorithm

In contrast to the CDVCA, the SDVCA is constructed based on Eq. (1). Since DC-link capacitors require a half cycle $T/2$ for the charging process [16–18], based on Eq. (1), P can be written as

$$\int_0^{T/2} 3\, V_{S,rms} I_{charg,rms} \cos\theta dt = c_{dc} \int_{V_{dc}}^{V_{dc\_ref}} V_{dc} dV_{dc}, \quad (3)$$

where $V_{S,rms}$ is the root-mean-square (RMS) supply voltage and $I_{charg,rms}$ is the RMS SAPF charging current. Eventually, Eq. (3) can be represented as

$$\frac{3}{2} V_S I_{charg} \cos\theta T = \frac{c_{dc}}{2} \left(V_{dc\_ref}^2 - V_{dc}^2\right), \quad (4)$$

where V_S is the peak amplitude of $v_S(t)$ and I_{charg} is the peak amplitude of $i_{charg}(t)$. Since the phase θ between $v_S(t)$ and $i_{charg}(t)$ is controlled to be 0° (unity power factor),

$$I_{charg\_est} = I_{charg} = \frac{c_{dc}\left(V_{dc\_ref}^2 - V_{dc}^2\right)}{3V_S T} = \frac{c_{dc} f \left(V_{dc\_ref}^2 - V_{dc}^2\right)}{3V_S}, \quad (5)$$

where f is the operating frequency of power systems and it is either 50 Hz or 60 Hz. Eq. (5) is named a self-charging equation [16–18].

A block diagram of the SDVCA is illustrated in Figure 3. In this algorithm, a voltage controller is used to minimize the error $e_s(t)$ between the square value of V_{dc} and the square value of V_{dc_ref}. Then the control signal $\delta e_s(t)$ of the voltage controller is utilized in the self-charging equation. Furthermore, if the same PI controller is employed as the voltage controller, then

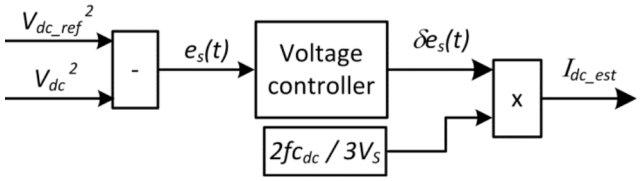

Figure 3. Block diagram of the SDVCA.

$$I_{charg\_est} = \frac{2}{3V_S} c_{dc} f \delta e_s(t) = \frac{2}{3V_S} c_{dc} f \left(K_p e_s(t) + K_i \int e_s(t) dt\right)$$
$$= \frac{2}{3V_S} c_{dc} f \left[K_p \left(V_{dc\_ref}^2 - V_{dc}^2\right) + K_i \int V_{dc\_ref}^2 - V_{dc}^2 dt\right] \quad (6)$$

3. Simulation results and analyses

The SAPF, CDVCA, and SDVCA are simulated using MATLAB/Simulink. In this work, the SAPF is connected to a 3-phase 400-V, 50-Hz power system. The same PI controller is implemented in both the CDVCA and the SDVCA, for achieving justified analysis. Gain values of the PI controller are tuned based on the optimum performance of the SAPF using the CDVCA. Both K_p and K_i values are tuned using a tuning algorithm for regulating the SAPF's DC-link voltage.

$$K_p = 2\sqrt{2}\pi f c_{dc} \text{ and } K_i = c_{dc}\left(2\pi f\right)^2 \tag{7}$$

A detailed explanation about this tuning algorithm is presented in [20].

In the present work, the SAPF performance with the respective voltage control algorithms is analyzed in 4 different conditions. Each condition is distinguished by the action of switches S1 and S2. In all cases, V_{dc_ref} is 1250 V.

3.1. Case 1 (both S1 and S2 are closed at $t = 0$; $K_p = 0.3$ and $K_i = 1$)

In this condition, the operation of both power system and SAPF starts simultaneously. Therefore, the initial value of V_{dc} is 0.

Figure 4 shows step responses of DC-link voltages with the SAPF using both algorithms. According to the figure, the initial charging time t_{caj} using the CDVCA is lower than that using the SDVCA; t_{caj} refers to the time that the DC-link capacitor C_{dc} starts charging. The charging process of the SAPF starts at 2.7 ms using the CDVCA and at 0.7 ms using the SDVCA. Other than that, the C_{dc} using the CDVCA experiences a much faster rising time than using the SDVCA. It takes 50 ms using the CDVCA and 500 ms using the SDVCA to increase V_{dc} from 800 V to 1125 V. Moreover, before V_{dc} reaches 800 V, the C_{dc} using the CDVCA exhibits very high voltage fluctuation, and this situation does not occur with the use of the SDVCA. Consequently, the overshoot of V_{dc} using the CDVCA is 7% higher than using the SDVCA: 1357 V using the CDVCA and 1263 V using the SDVCA. However, the settling time t_{set} using both algorithms is similar: t_{set} is 1.7 s. Instead, RF of V_{dc} using the CDVCA is higher than using the SDVCA: 0.062% using the CDVCA and 0.055% using the SDVCA; these values are obtained by dividing the peak-to-peak value of V_{dc} with the average value of V_{dc}. In this case, V_{dc} behavior can be explained using the measured DC-link current waveform.

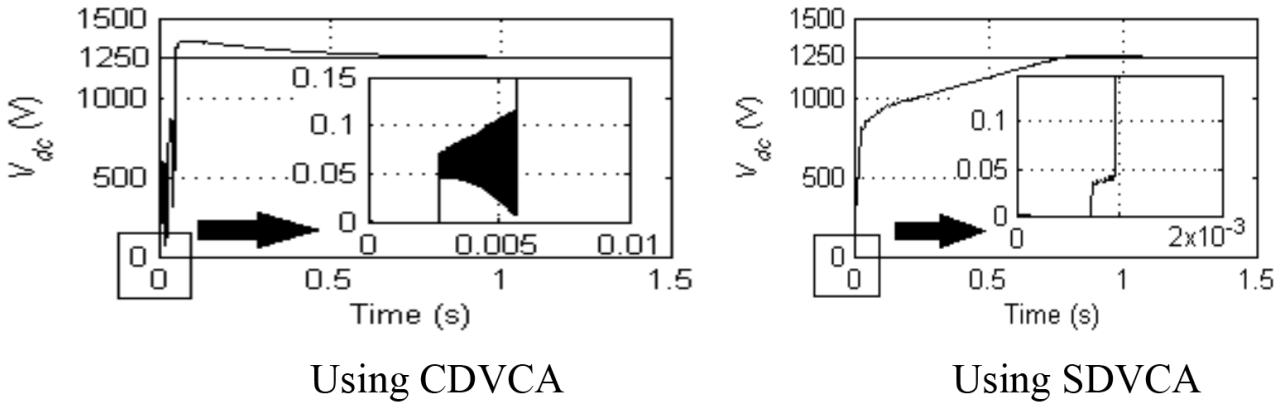

Figure 4. Step responses of V_{dc} in Case 1.

Waveforms of DC-link currents using both algorithms are shown in Figure 5. Since both currents show similar waveforms during the steady-state condition, the following explanation gives emphasis on the property of both DC-link currents before reaching the steady-state condition. In the figure, the negative sign of DC-link current refers to the charging process of C_{dc} where the SAPF draws $i_{charg}(t)$, and the positive sign of DC-link current refers to the discharging process of C_{dc} where the SAPF injects the instantaneous compensation current $i_F(t)$. Based on the figure, the SAPF using the CDVCA starts to draw DC-link current at 2.7 ms. However, it takes only 0.7 ms using the SDVCA, hence explaining the low initial t_{caj} using the CDVCA. Moreover, the SAPF using the CDVCA draws 4 times higher DC-link current than using the SDVCA. Thus, it clarifies the high rising time of V_{dc} using the CDVCA. Furthermore, the SAPF using the CDVCA needs to draw and inject DC-link current from or to the power system, therefore resulting in very high V_{dc} fluctuation across C_{dc}. In addition, it can be seen that the SAPF using the CDVCA keeps increasing its DC-link current although V_{dc} has reached its set-point (SP), consequently increasing the overshoot of V_{dc}.

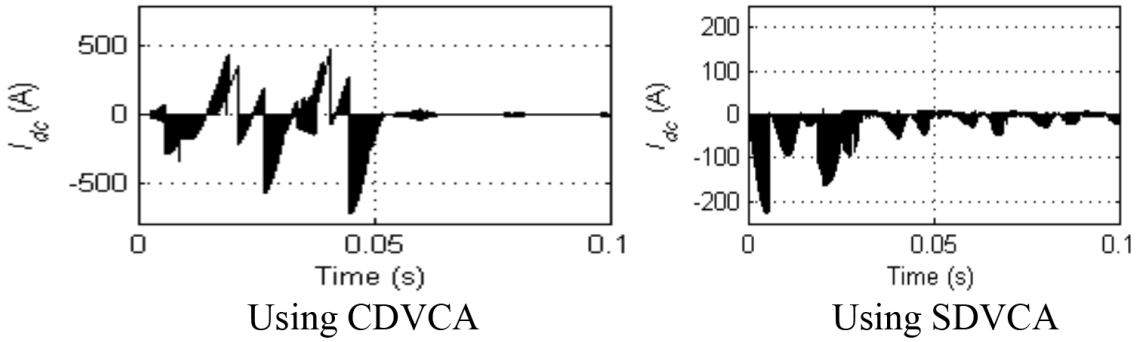

Figure 5. Measured DC-link current in Case 1.

Waveforms of I_{charg_est} using both algorithms are shown in Figure 6. Note that I_{charg_est} has an opposite polarity from the measured DC-link current. It refers to the instantaneous current supplied by the power system. In the figure, I_{charg_est} from 0 to 0.05 s using the CDVCA is 15 times higher than using the SDVCA. It is because I_{charg_est} corresponds directly to the change of V_{dc}. In contrast, the SDVCA computes an almost constant I_{charg_est} during the same time interval, hence explaining the low rise time of I_{charg_est}. Moreover, when V_{dc} reaches the SP, the CDVCA is still estimating positive I_{charg_est} while the SDVCA starts to reduce the I_{charg_est} value. Consequently, these situations affect the overshoot of V_{dc}. Furthermore, during the steady-state operation, I_{charg_est} using the CDVCA has higher ripples than using the SDVCA. Since I_{charg_est} is a part of the reference current, it will affect THD values of both reference current and $i_S(t)$. According to simulation results, the THD value of the reference current using the CDVCA is higher than using the SDVCA: 0.34% using the CDVCA and 0.21% using the SDVCA. Subsequently, the SAPF using the CDVCA results in higher THD value of $i_S(t)$ than using the SDVCA. THD values using the CDVCA and SDVCA are 3.33% and 3.17%, respectively. All related waveforms are presented in Figure 7.

3.2. Case 2 (S1 is closed at $t = 0.5$ s and S2 is closed at $t = 0$; $K_p = 0.3$ and $K_i = 1$)

In this condition, the operation of both power system and SAPF starts consecutively. The power system is firstly started and it is followed by the SAPF. The starting time t_{start} of the SAPF is determined by the action of S1. At this moment, the initial value of V_{dc} is 0.

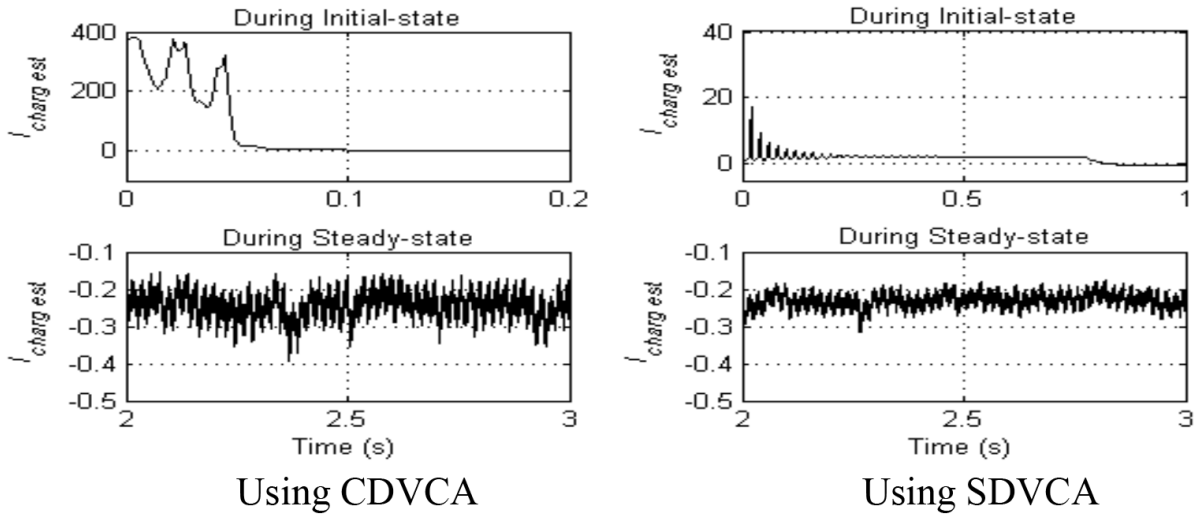

Figure 6. Estimated DC-link charging current in Case 1.

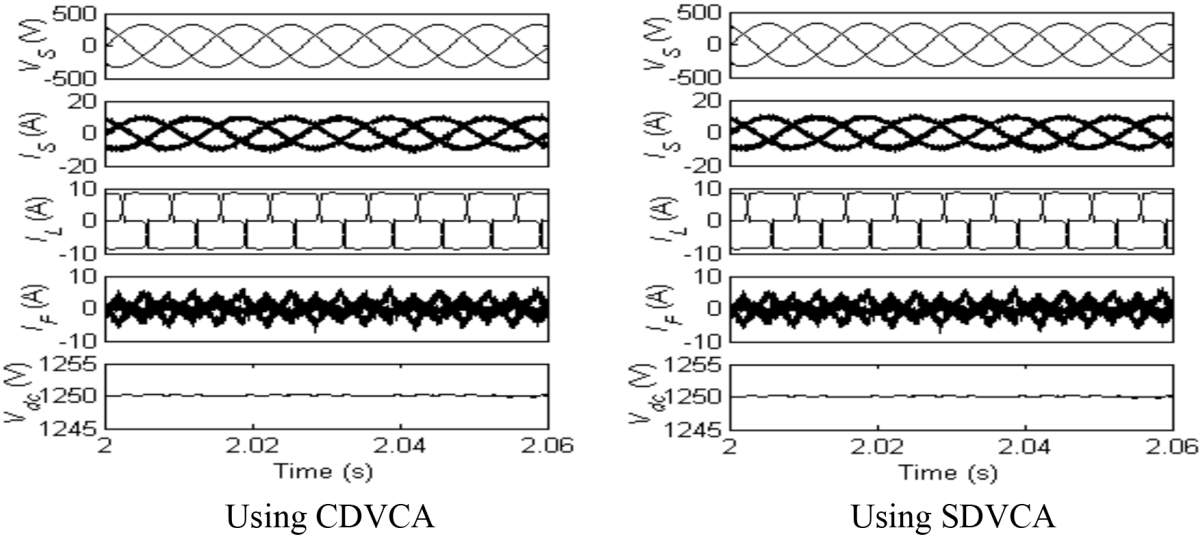

Figure 7. Waveforms of selected parameters in Case 1.

Figures 8 and 9 show step responses of V_{dc} and waveforms of selected parameters, respectively. According to both figures, the SAPF using either the CDVCA or the SDVCA has shown different responses with respect to t_{start}. Apparently, the SAPF using the CDVCA is unable to regulate its V_{dc} value. On the other hand, it does not encounter V_{dc} control problem when it implements the SDVCA. This scenario happens due to the instability of the PI controller, and it can be resolved by lowering the K_i value. However, based on the aforementioned result, it can be confirmed that the CDVCA is not compatible to work with a fast voltage controller. Moreover, the unstable PI controller has contributed to high current flow in the SAPF, halting the harmonic compensation process. Instead, the SAPF using the SDVCA displays quite similar behavior as its performance in Case 1. Furthermore, it can be stated that the SAPF that operates in Case 2 has faster t_{set} (1.65 s) than its operation in Case 1 (1.7 s). Nevertheless, the THD value of $i_S(t)$ is higher than the THD value in Case 1: 3.21% in Case 2 and 3.17% in Case 1.

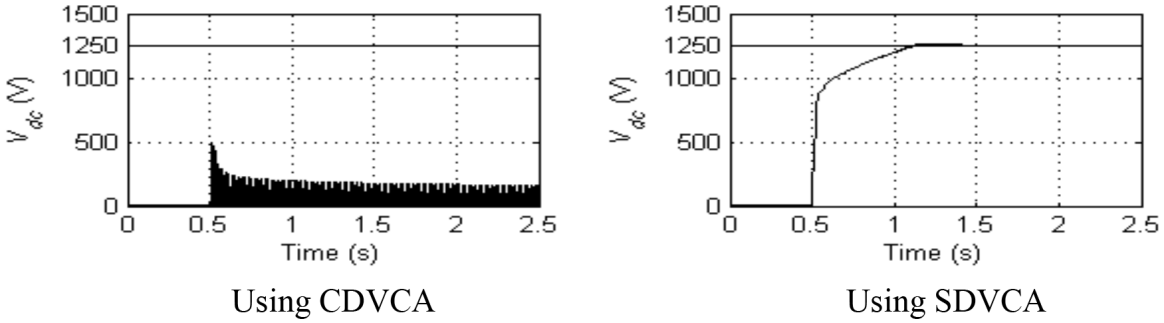

Figure 8. Step responses of V_{dc} in Case 2.

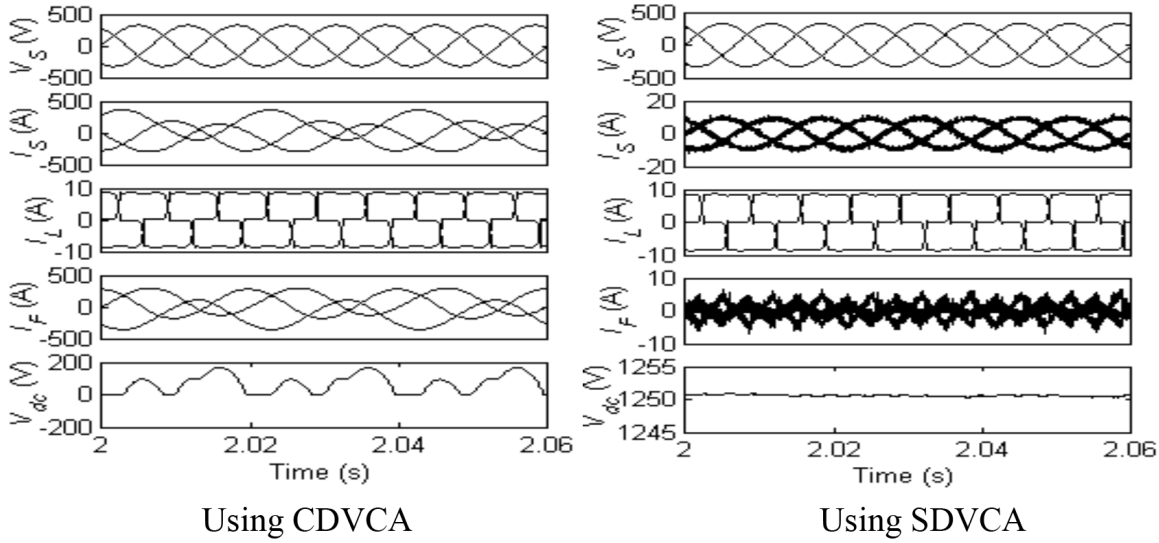

Figure 9. Waveforms of selected parameters in Case 2.

3.3. Case 3 (S1 is closed at $t = 0$ and S2 is closed at $t = 0.5$s; $K_p = 0.3$ and $K_i = 1$)

Similar to Case 2, the operation of both power system and SAPF starts consecutively. However, in this case study, t_{start} is determined by the action of S2. In this case, the SAPF is able to draw current from the power system, and therefore increase its initial V_{dc} from 0 to a certain voltage value.

Unlike in Case 2, the SAPF using the CDVCA is able to regulate its V_{dc} and perform its designated operation. Step responses of V_{dc} are depicted in Figure 10. However, its C_{dc} experiences 70% higher overshoot of V_{dc} (2129.5 V) than V_{dc_ref}. Moreover, t_{set} is 30% longer than the t_{set} in Case 1: 2.25 s in Case 3 and 1.7 s in Case 1. The THD value of $i_S(t)$ is also higher than the THD value in Case 1: 3.36% in Case 3 and 3.33% in Case 1. Instead, the SAPF using the SDVCA exhibits similar behavior as in Case 1 and Case 2. In this case study, the overshoot of V_{dc} is 1262.5 V, the settling time is 1.62 s, and the THD value of $i_S(t)$ is 3.23%.

3.4. Case 4 ((a) both S1 and S2 are closed, and (b) S1 is closed at $t = 0.5$ s and S2 is closed at $t = 0$; $K_p = K_{p\_old} = 0.3$ and $K_{i\_new} = 0.51$)

Lastly, both Case 1 and Case 2 are once again conducted using a new K_i value. Step responses of V_{dc} for Case 4a and Case 4b are presented in Figures 11a and 11b, respectively. Based on both figures, the SAPF using

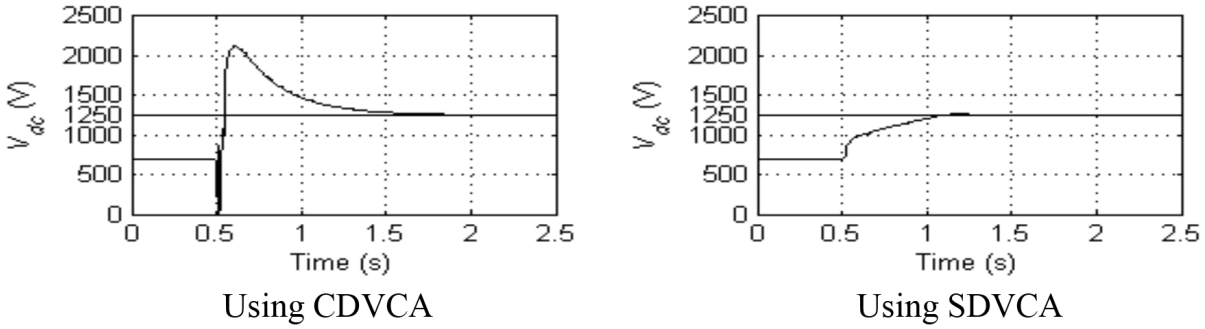

Figure 10. Step responses of V_{dc} in Case 3.

either the CDVCA or the SDVCA is able to regulate its V_{dc} value. However, in Case 4b, the C_{dc} using the CDVCA experiences 98% higher overshoot of V_{dc} (2470.2 V) than V_{dc_ref}. Furthermore, it can be observed that the C_{dc} experiences longer t_{set} than using the previous K_i value: 3 s in Case 4a, 4.8 s in Case 4b, and 1.7 s in Case 1. It is because the new PI controller has lower K_i value than the previous cases, hence decelerating the response time of the PI controller. On the other hand, the SAPF using the SDVCA shows similar behavior as in Case 1 and Case 2. Moreover, it is able to achieve the same t_{set} in both conditions. In this case, t_{set} is 2.7 s and it is about 1 s longer than the previous t_{set}.

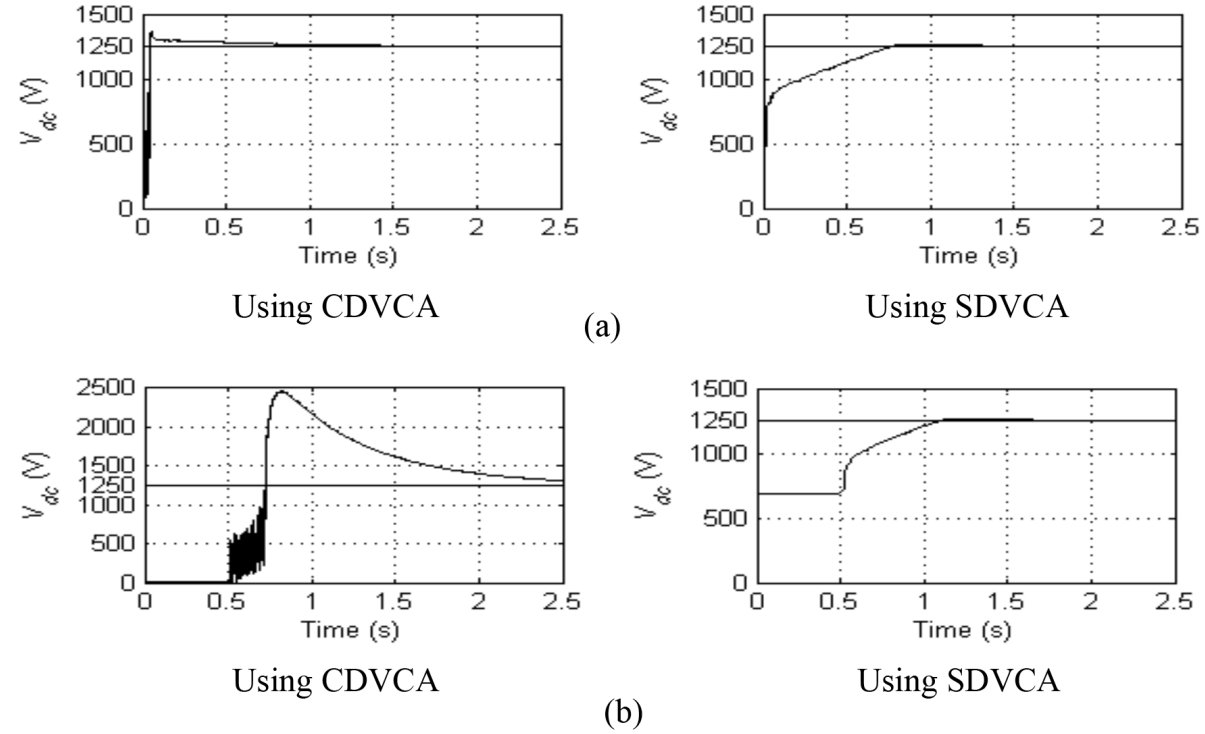

Figure 11. Step responses of V_{dc} using a new K_i value; (a) for Case 1 and (b) for Case 2.

Overall, these case studies provide important insights into the operation of V_{dc} control using both the CDVCA and the SDVCA. Obviously, the operation of V_{dc} control using the CDVCA is fully dependent on tuning gains of the PI controller and parameters of the power system and the SAPF. Therefore, in all 4 cases,

the SAPF exhibits different step responses of V_{dc}. Moreover, it can be identified that the CDVCA is suitable to work with a slow PI controller, for stabilizing the V_{dc} control process. Additionally, the generated I_{dc_est} has also increased the THD value of the SAPF's reference current. Consequently, it is lowering the effectiveness of the SAPF operation in compensating harmonic currents. As a result, the THD value of compensated $i_S(t)$ increases.

In contrast, the operation of V_{dc} control using the SDVCA is not directly affected by tuning gains of the PI controller. It is because the SDVCA considers other parameters such as c_{dc} and V_S. Consequently, the SAPF shows similar step response of V_{dc} in all cases. Furthermore, it can be confirmed that the operation of the SDVCA is compatible with a fast PI controller. Hence, it can improve the SAPF's dynamic operation. Moreover, the SDVCA is able to generate lower THD value of I_{dc_est}, therefore reducing the THD value of the SAPF's reference current and increasing the efficiency of the SAPF.

4. Experimental results

This experimental work focuses on the operation of the SAPF using the SDVCA only; it demonstrates better performance than using the CDVCA. Code Composer Studio (CCS) v3.3 is employed to write and compile the SAPF's control algorithms in C language, and build it in DSP TMS320F28335. Figure 12 shows experimental results for per-phase waveforms only (phase a). From the figure, it can be seen that the SAPF has successfully regulated constant value of V_{dc}. At the same time, the shape of the compensated $i_{Sa}(t)$ has resumed to almost fully sinusoidal and the THD value equals 4.88%.

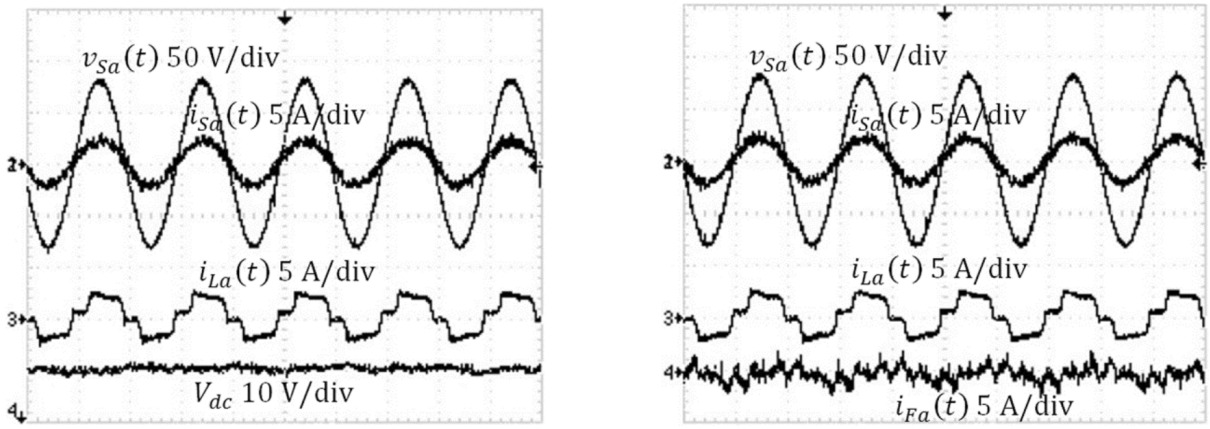

Figure 12. Experimental results using the SDVCA.

5. Conclusion

The CDVCA and the SDVCA are successfully implemented in the 3-phase 3-wire SAPF. According to the presented results and analyses, it can be concluded that the SDVCA performs better than the CDVCA, starting the charging process in a very short period; reducing the overshoot, t_{set}, and RF of V_{dc}; generating low ripple of estimated DC-link charging current; and maintaining the SAPF's performance regardless of its t_{start} and initial V_{dc} value. Since the SDVCA is able to reduce the overshoot and RF of V_{dc}, a low rating of C_{dc} can be utilized. Hence, it reduces the construction cost of the SAPF. Moreover, unlike the CDVCA, the SDVCA is compatible to work with a fast voltage controller, thus improving the dynamic response of the SAPF. Eventually, the SDVCA can be claimed to be the most suitable V_{dc} control algorithm since it helps to further reduce the THD value of $i_S(t)$.

Acknowledgments

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