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Performance enhancement of a dynamic voltage restorer

Latha Pappath VASUDEVAN*, Valsalal PRASAD
Department of Electrical Engineering, College of Engineering Guindy, Anna University, Chennai, India

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Abstract: Custom power devices are widely employed to mitigate power quality issues affecting critical loads. The dynamic voltage restorer is one of the custom power devices designed to inject a voltage in series with line to present a pure sinusoidal voltage of the desired RMS value to the sensitive loads, if the supply side is affected by voltage disturbances. The design and implementation of a DVR with a quasi-impedance source inverter and variable structure control is discussed in this paper. The voltage boosting ability of a quasi-impedance (Z) source inverter is used here to improve the performance of the DVR with reduced energy storage. The control system designed based on variable structure control effectively supports the DVR with good dynamic response, even under parameter variations. Performance of the proposed system in a single phase network is evaluated against the conventional DVR system using MATLAB simulation studies. An experimental model of the proposed system was developed to validate the simulation results. Implementation of the proposed DVR in a 3 phase distribution system is investigated with the help of simulation studies.

Key words: Custom power devices, dynamic voltage restorer (DVR), quasi Z source inverter, variable structure control

1. Introduction

Voltage sags and swells are major power quality events in the distribution system, subjecting sensitive loads to operate under high risk. Utility customers such as medical equipment, factory automations, and manufacturing units of semiconductor devices incur huge operational and production losses due to the vulnerability of their critical loads to power-supply disturbances [1–3]. Events such as short circuits in the upstream power transmission line or parallel power distribution line connected to the point of common coupling (PCC), inrush currents in the line due to the starting of large machines, sudden changes in loads, energizing of transformers etc. or switching operations in the grid give rise to voltage disturbances in the line. According to the IEEE 1159-2009 standard, voltage sag is defined as a "decrease in magnitude of 0.1 p.u. to 0.9 p.u. in the RMS voltage, at system frequency and with the duration of half a cycle to 1 min" [3,4]. Custom power devices are employed to mitigate the power quality issues [5]. A dynamic voltage restorer (DVR) presents an ideal power electronic interface to restore the voltage waveform quality at the load side terminals whenever the quality of the supply side voltage suffers. Voltage compensation strategies and control techniques of the DVR are widely discussed in the literature [6–8].

The DVR injects an appropriate compensating voltage, generated by an inverter, through a series transformer connected to the load end of the line. A lead acid battery or any other energy source or the line to which the DVR is connected provides the required energy for the compensation [5–10]. Although novel solid state switches have brought down the size and cost of the inverter used in a DVR, still it is bulky, heavy,

*Correspondence: lathadinesh2@yahoo.com

and costly due to the energy storage element and series transformer. Hence there is a need to reduce the storage energy requirement for voltage compensation.

Widely used controllers in DVR are conventional controllers based on classical control theory or modern control theory. They require precise mathematical linear models and their performance suffers from parameter variation [5–10]. Variable structure controllers work effectively without the need for accurate mathematical models. Sliding mode controllers belong to the class of variable structure controllers. They perform better in nonlinear systems with the range of parameter variation to ensure stability and satisfactory reaching conditions are known [11–14]. Sliding mode controllers are simple to implement in highly variable structures like converters and provide stable and robust operation. Sliding mode controllers to regulate the voltage source inverters in custom power devices are discussed in the literature [12,13].

The voltage rating of the battery used as energy storage and the nonlinear structure of the control system are the limiting factors affecting the performance of a conventional DVR, apart from special circuits to detect the voltage disturbances [15]. Conventional DVRs use voltage source inverters (VSIs) to convert the DC power into AC power, which is to be fed to the primary of the series injection transformer. Quasi Z source converters have found wide acceptance due to their reduced component use, simple control strategies, and buck boost capabilities [16–18]. The proposed DVR uses a quasi Z source inverter to maintain the required voltage for compensation and a sliding mode controller for faster dynamic response. The design, evaluation, and implementation of the proposed DVR in a single phase system are carried out first, in order to investigate its feasibility in three phase systems.

2. Salient features of the proposed DVR

A schematic diagram of a conventional dynamic voltage restorer in single phase systems connected in series with a sensitive load is shown in Figure 1. A single phase DVR consists of a voltage source inverter, which is fed from a battery, a passive filter, an injection transformer, and a proportional plus integral controller to regulate the inverter output voltage. The proposed DVR employs a quasi Z inverter fed from a battery to generate the required voltage for compensation and a sliding mode controller for the regulation of inverter output voltage. Among the various voltage compensation techniques [19], pre-sag compensation is used in this system.

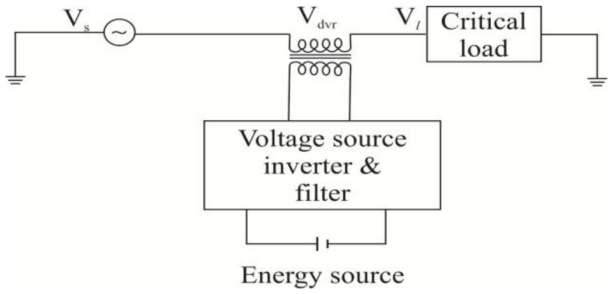

Figure 1. Structure of a DVR.

A phasor diagram of the compensation strategy employed here is shown in Figure 2. The variables after the sag are indicated by dashed quantities $(V_s^{'},\ V_l^{'},\ V_{dvr}^{'},\ I_l^{'})$. The quantities prior to the sag are represented by V_s, V_l, and I_l. The phase angle of the load voltage is preserved in this compensation scheme. A phase locked loop (PLL) synchronized with the load voltage gets locked as soon as a disturbance occurs and this in turn restores the phase angle of the load voltage. Real and reactive powers are injected by the DVR, depending on the depth of the sag.

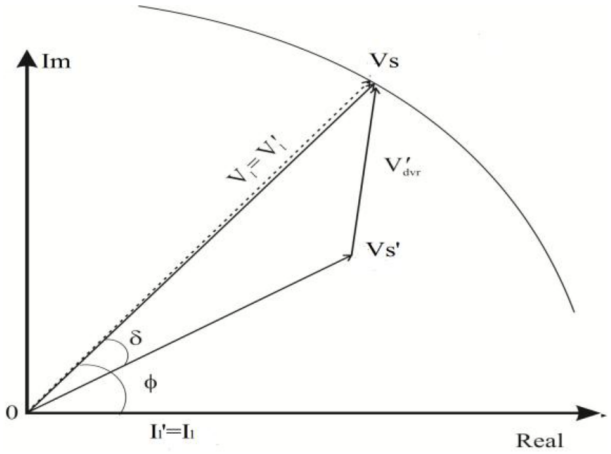

Figure 2. Pre-sag compensation phasor diagram.

The real power rating of the DVR is given by

$$P_{DVR} = P_{load} - P_{grid}, \tag{1}$$

where δ is phase jump during sag and φ is the load phase angle.

$$P_{DVR} = V_l\, I_l \cos\phi - V_s^{'} I_l \cos(\phi - \delta) \tag{2}$$

$$V_{DVR} = \sqrt{2}\sqrt{V_l^2 + V_s'^2 - 2V_l V_s' \cos\delta} \tag{3}$$

The phase angle of injected voltage is

$$\angle V_{DVR} = \tan^{-1} \frac{V_l \sin\phi - V_s^{'} \sin(\phi - \delta)}{V_l \cos\phi - V_s' \cos(\phi - \delta)} \tag{4}$$

In the proposed DVR, a PLL synchronized with load voltage is used to implement the pre-sag compensation.

2.1. Quasi Z source inverter

The heart of the DVR is the inverter capable of injecting the required voltage through a series transformer to the load end. The circuit topology of the quasi Z source inverter employed here is shown in Figure 3. The distinguishing feature of this inverter is the insertion of shoot through states along with the normal active states. During the shoot through states, either both switches of the same leg or all the four switches of the inverter are turned on simultaneously, leading the output voltage of the inverter to 0 V. This effectively gives rise to a voltage boost at the output terminals.

A brief description of the operation of the quasi Z source inverter is given here. In a switching cycle of period T, if T_0 is considered the shoot through period, the remaining duration T_1 is the active state of the inverter.

Thus

$$T = T_0 + T_1 \tag{5}$$

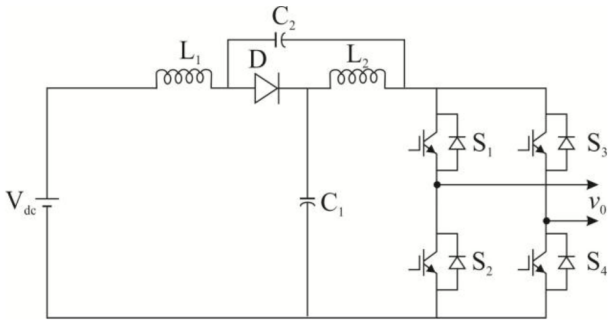

Figure 3. Single phase quasi Z source inverter.

The shoot through duty ratio

$$D = \frac{T_0}{T} \tag{6}$$

On analyzing the equivalent circuits of the quasi Z source inverter during the shoot through states and the active states, it has been found that

$$V_{c_1} = \frac{V_{dc}(1-D)}{1-2D} \tag{7}$$

$$V_{c_2} = \frac{V_{dc}D}{1-2D} \tag{8}$$

The peak DC link voltage is given as

$$\hat{v}_0 = \frac{V_{dc}}{1-2D} = BV_{dc}, \tag{9}$$

where 'B' is the boost factor, $\frac{\hat{v}_0}{V_{dc}} = B \geq 1$. The peak of the output phase voltage of the inverter is

$$\hat{V}_{ac} = M\frac{\hat{v}_0}{2} \tag{10}$$

where M is the modulation index.

Using Eqs. (9) and (10), the peak of the inverter output voltage can be expressed as

$$\hat{V}_{ac} = MB\frac{V_{dc}}{2} \tag{11}$$

It is evident that, compared with the traditional VSI, with voltage relationship $\hat{V}_{ac} = M\frac{V_{dc}}{2}$, the output voltage of a quasi Z source inverter can be stepped up or down by selecting an appropriate boost factor B. This enables the use of a lower rated battery as the energy source for the DVR, thus bringing down the cost and size.

The DVR operation is also limited by the capacity of the inverters, saturation of the series transformer, and the control bandwidth. The cutoff frequency of the LC output filter determines the control bandwidth of the DVR systems and the attenuation of switching ripple from the inverter output. Although infinite combinations of L and C values exist for a given cutoff frequency, considering the size and cost factor of inductance, the filter elements are designed.

2.2. Variable structure control of the DVR

The schematic block diagram of the proposed DVR is shown in Figure 4. It consists of a reference voltage calculator, variable structure controller, DC voltage source, quasi Z source converter, and LC filter. The output of the LC filter is connected to the line through a transformer. This section develops a model for the design of the variable structure controller for the DVR. The design of a sliding mode controller, which is a form of variable structure control, involves the following three main tasks.

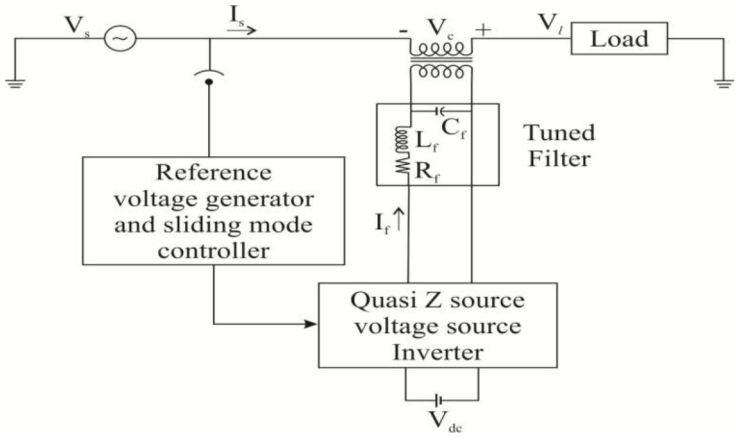

Figure 4. Block diagram configuration of the proposed DVR.

i. Design of a sliding surface,

ii. Checking the existence of sliding mode and a reaching condition, and

iii. Determination of the control law.

The control block diagram of the proposed DVR is depicted in Figure 5. The state space representation of the DVR with reference to Figure 5 can be written as

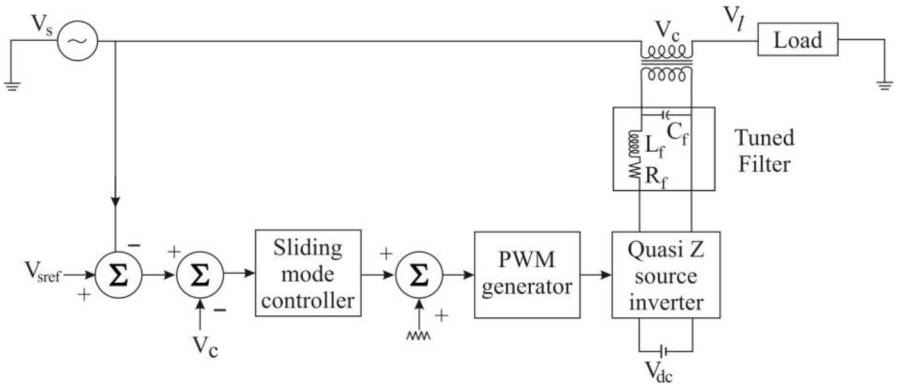

Figure 5. Control block diagram of the proposed DVR for single phase systems.

$$\frac{d}{dt}\begin{bmatrix} v_c \\ i_f \end{bmatrix} = \begin{bmatrix} 0 & 1/C_f \\ -1/L_f & -R_f/L_f \end{bmatrix}\begin{bmatrix} v_c \\ i_f \end{bmatrix} + \begin{bmatrix} -1/C_f & 0 \\ 0 & -1/L_f \end{bmatrix}\begin{bmatrix} i_s \\ \delta(t)V_{dc} \end{bmatrix} \tag{12}$$

where i_f and i_s are filter inductor current and source current, respectively. $\delta(\mathrm{t})$ is the switching function of the inverter, which can be either 1 or –1.

2.2.1. Design of the sliding surface

A sliding surface, which is directly affected by the switching law, will control the output voltage of the inverter. From (12), it is seen that, since the first time derivative of the output, $(dv_c/dt) = (i_f - i_s)/C_f = \theta$, is free from the control input $\delta(\mathrm{t})\mathrm{V}_{dc}$, the second derivative must be calculated

$$\begin{bmatrix} \dot{v}c \\ \dot{\theta} \end{bmatrix} = \begin{bmatrix} \theta \\ \frac{-Rf}{L}\theta - \frac{1}{LfCf}vc - \frac{Rf}{LfCf}is - \frac{1}{Cf}\frac{dis}{dt} + \frac{1}{LfCf}\delta(t)Vdc \end{bmatrix} \tag{13}$$

The phase canonical form (13) shows that as the second derivative of the output variable depends on the control input $\delta(\mathrm{t})\mathrm{V}_{dc}$, no further time derivative is required. Taking the tracking error as $e_{v_c} = v_c^{ref} - v_c$, a sliding surface $\rho(e_{v_c}, t)$, is chosen such that

$$\rho(e_{v_c}, t) = k_1 e_{v_c} + k_2 \frac{de_{v_c}}{dt} = 0, \tag{14}$$

where the constants k_1 and k_2 are chosen so that a linear combination of the tracking error and its derivative approaches zero. Eq. (14) represents a surface in the error space and is called the sliding surface.

2.2.2. Checking the existence of sliding mode operation

The existence of the operation in sliding mode implies that $\rho(e_{v_c}, t) = 0$. Moreover, if $\dot{\rho}(e_{v_c}, t) = 0$, the control system insures that the system stays in this regime. For co- existence of the above two conditions, the switching law must ensure that

$$\rho(e_{v_c}, t)\dot{\rho}(e_{v_c}, t) < 0 \tag{15}$$

This satisfies the stability condition for the system in sliding mode.

The fulfillment of this inequality ensures the convergence of the system trajectories to the sliding surface $\rho(e_{v_c}, t) = 0$, since in either of the following cases the surface approaches zero.

(a) If $\rho(e_{v_c}, t) > 0$ and the derivative $\dot{\rho}(e_{v_c}, t) = 0$, or

(b) If $\rho(e_{v_c}, t) < 0$ and $\dot{\rho}(e_{v_c}, t) > 0$, the tracking error will move towards the surface $\rho(e_{v_c}, t)$. As this shows that as $\rho(e_{v_c}, t)$ converges to zero, the trajectories in the system space are forced into the sliding surface and the condition (15) is called the sliding mode existence condition.

2.2.3. Checking the reaching condition

The fulfillment of $\rho(e_{v_c}, t)\dot{\rho}(e_{v_c}, t) < 0$ as $\rho(e_{v_c}, t)\dot{\rho}(e_{v_c}, t) = (1/2)\dot{\rho}^2(e_{v_c}, t)$ implies that the system state always approaches the sliding surface.

2.2.4. Determination of the control law

After verifying the existence condition, the switching law for the IGBT devices can be devised as

$$\delta(t) = \begin{cases} 1 & for \quad \rho(e_{v_c}, t) > 0 \\ -1 & for \quad \rho(e_{v_c}, t) < 0 \end{cases} \tag{16}$$

In an ideal sliding mode controller, at infinite switching frequency, state trajectories are directed towards the sliding surface and move exactly along the discontinuity surface. As power converter switching frequency is in the finite range, a typical implementation features a comparator with hysteresis 2ε, where switching occurs at $|\rho(e_{v_c}, t)| > \varepsilon$. With this hysteresis comparator the switching law modifies to (17)

$$\delta(t) = \begin{cases} 1 & for \quad \rho(e_{v_c}, t) > \varepsilon \\ -1 & for \quad \rho(e_{v_c}, t) < -\varepsilon \end{cases} \tag{17}$$

In order to achieve fixed frequency operation, a triangular wave with frequency slightly greater than the maximum variable frequency is added to the sliding mode controller output [14].

2.2.5. Robustness of the controller

Since the sliding surface and switching do not depend on system operating point, load, circuit parameters, power supply, and the converter dynamics, operating in sliding mode is robust.

3. Control strategy for the proposed DVR

The control block diagram of the proposed DVR for a single phase network is shown in Figure 5. The reference voltage V_{cref} to be injected by the DVR is obtained by subtracting the reference source voltage and actual source voltage. Using a PLL, a sine template is generated, which is then multiplied by the peak of the supply reference voltage to obtain the reference supply voltage. The actual DVR injected voltage is then subtracted from the reference DVR voltage to obtain the error signal, which is then processed by the sliding mode controller. The sliding mode controller parameters k_1 and k_2 are appropriately chosen tuned. The output of the sliding mode controller is the reference signal for the PWM generator of the inverter. There are a number of methods available to obtain the shoot through states in a quasi Z source inverter. The simple boost modulation method is used here in which the shoot through states are obtained when a constant amplitude signal is combined with the triangular carrier PWM signals.

4. Simulation results and discussion

Observations derived from the simulation studies performed in the MATLAB SIMULINK platform on both the conventional and proposed DVR in single phase systems are presented along with the simulation results of the proposed DVR in three phase systems. Table 1 shows the system parameters used for the simulation studies on the proposed and conventional DVRs along with the system parameters of the experimental model of the proposed one for single phase systems. The battery storage to support the conventional DVR is found to be 300 V, as compared to 70 V needed for the proposed one, to mitigate the same duration and depth of voltage disturbances. The supply voltage, injected voltage by the DVR, and the load voltage waveforms of the conventional and proposed DVRs are depicted in Figures 6 and 7, respectively. The systems are subjected to 60% voltage sag during 0.05 s to 0.2 s and a voltage swell of 30% during 0.3 s to 0.45 s. The DVR responds by injecting appropriate voltages to maintain the desired voltage profile at the load end. The PI controller and sliding mode controller performances are reflected in the waveform quality and response of the respective DVRs. Simulation studies were conducted on both DVRs for various operating conditions to evaluate the efficacy of the sliding mode controller and the adequacy of the quasi Z source inverter with a reduced DC source to support the DVR operation. The systems are subjected to supply voltage sag of 50% at a constant current of 5 A, and connected to different types of loads such as resistive, R-L, resistive with a rectifier, etc. The load voltage and

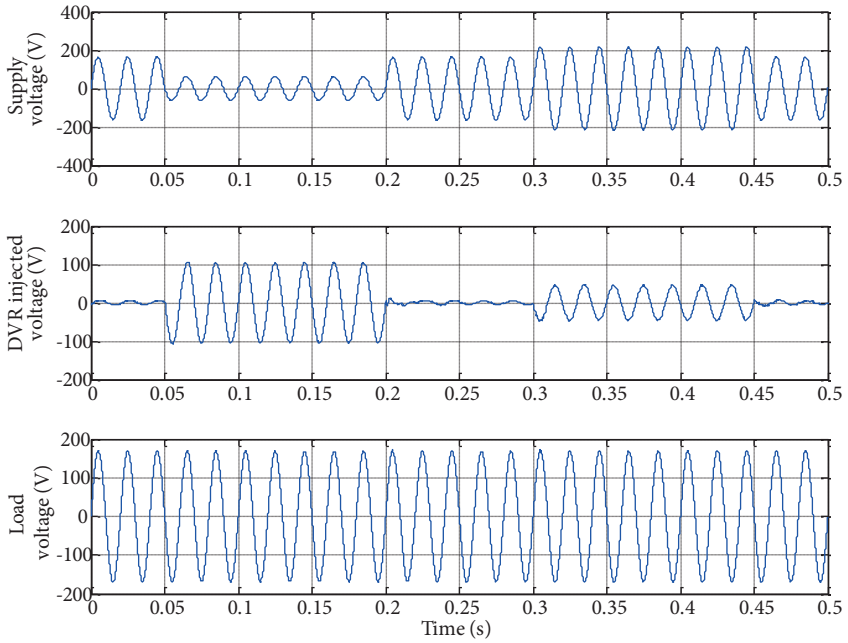

Figure 6. Simulation results for conventional DVR.

THD for all the different load scenarios are shown in Table 2. The observations on the performance of the DVRs when the system is subjected to 50% sag at various load currents with the load being a resistive one connected through a full wave rectifier is summarized through a graph in Figure 8. The results of studies conducted in the systems at fixed loading and different sag conditions of the supply voltage are presented via a graph in Figure 9. They show that the conventional DVR causes an increase in THD along with a decrease in RMS load voltage as the load current increases, whereas the proposed DVR maintains the RMS load voltage at the desired level with reduced THD for the variation in the load. These observations clearly indicate the robustness of the proposed DVR in maintaining the desired voltage profile with much reduced THD over the conventional one.

Table 1. System parameters for the simulation and experimental study of the proposed DVR and conventional DVR.

System parameters (single phase system)	Proposed DVR (simulation study)		Conventional DVR (simulation study)	Proposed DVR (experimental study)
Source voltage	120 V		120 V	120 V
Frequency	50 Hz		50 Hz	50 Hz
Injection transformer	1:1, 1 kVA		1:1, 1 kVA	1:1, 1 kVA
Load	R-L		R-L	R-L
DC source battery	70 V, 10 Ah		300 V, 10 Ah	70 V, 10 Ah
Inverter switching frequency	10 kHz		10 kHz	10 kHz
Quasi Z source impedance	L	400 μH	-	380 μH
	C	500 μF	-	500 μF
Filter	R	0.2 Ω	1 Ω	0.5 Ω
	L	2.5 mH	40 mH	2.5 mH
	C	20 μF	100 μF	20 μF

A study was conducted on the DVRs to understand the efficacy of the quasi Z source inverter to effectively implement a DVR capable of withstanding deep voltage sags of longer duration, with reduced energy storage.

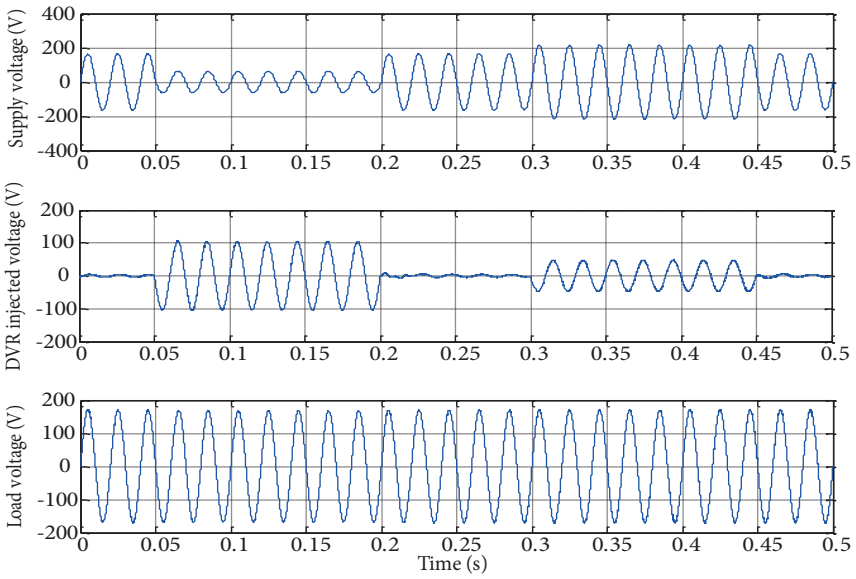

Figure 7. Simulation results for the proposed DVR.

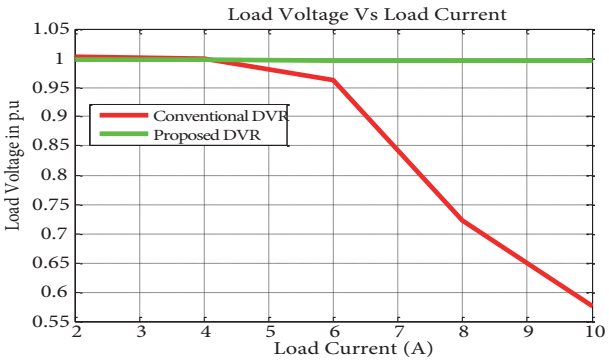

Figure 8. Voltage compensation capability of the two DVRs for different loadings.

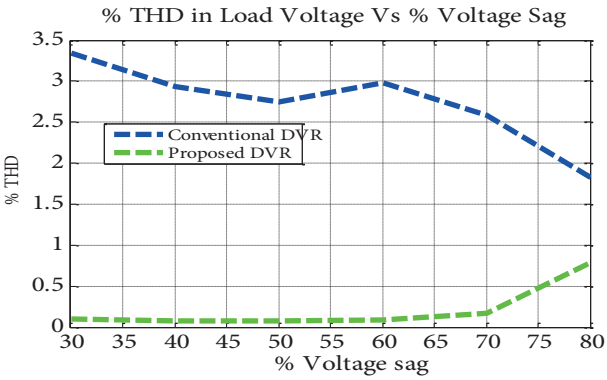

Figure 9. %THD in the load voltage of DVRs for various sag conditions.

Table 2. Performance of the DVRs for different types of load at 50% sag, 5 A.

Types of load	Conventional DVR		Proposed DVR	
	THD %	Load voltage (pu)	THD %	Load voltage (pu)
R Load	2.75	0.988	0.08	0.9966
RL Load	4.81	0.9641	0.09	0.9966
Nonlinear load R type	2.56	0.9886	0.08	0.9966
Nonlinear load RL type	5.03	0.9543	0.13	0.9966

Table 3 shows the minimum battery voltage required to mitigate different levels of voltage sags for both types of DVRs when supplying similar loads. It was observed that although the battery voltage requirement increases in both cases as the depth of the sag increases, the rating of the battery needed for the proposed DVR is only around 25% of that required for the conventional one. The adequacy and effectiveness of the quasi Z source inverter used here is evident from these simulation results.

Table 3. Simulation results showing minimum battery voltage required to mitigate different %voltage sags for the proposed and conventional DVRs.

%voltage sag	Proposed DVR		Conventional DVR	
	Minimum battery voltage required (V)	%THD in DVR injected voltage	Minimum battery voltage required (V)	%THD in DVR injected voltage
10%	20	0.16	180	1.2
30%	25	0.28	190	2.1
50%	35	0.32	200	2.29
70%	50	0.42	220	1.98
90%	60	0.87	280	2.09

As a practical distribution network consists of three phase systems, the performance of the proposed DVR in a three phase network is studied in MATLAB SIMULINK environment as shown in Figure 10. The system supply voltage is 400 V (line to line) connected to an R-L load. It makes use of three single phase inverters connected to a single LC network that form a three phase quasi Z source inverter and are connected to the primaries of three single phase injection transformers. Three sliding mode controllers independently generate the reference voltage for the PWM generators of the gating circuits of IGBT switches. The system parameters are shown in Table 4. Performance of the DVR, when one of the line voltages is subjected to voltage sag of 60% from 0.1 s to 0.2 s and subsequently a 30% swell from 0.25 s to 0.3 s is depicted in Figure 11. It shows that the proposed DVR performs effectively both in single phase and three phase systems. Figure 12 shows the simulation results when the system is subjected to 40% sag in all three phases from 0.1 s to 0.2 s and a 25% swell in all phases from 0.25 s to 0.3 s. These results imply that the proposed DVR is capable of mitigating major power quality issues of voltage sag and swell experienced in three phase distribution networks.

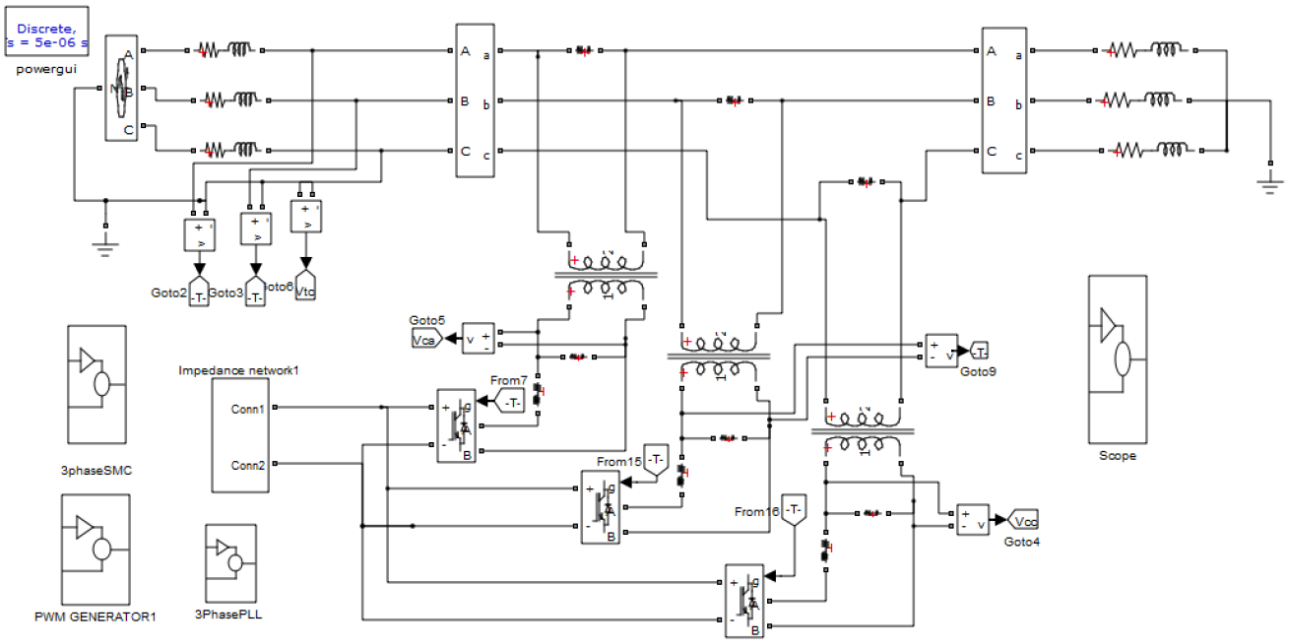

Figure 10. SIMULINK configuration of the proposed DVR in three phase systems.

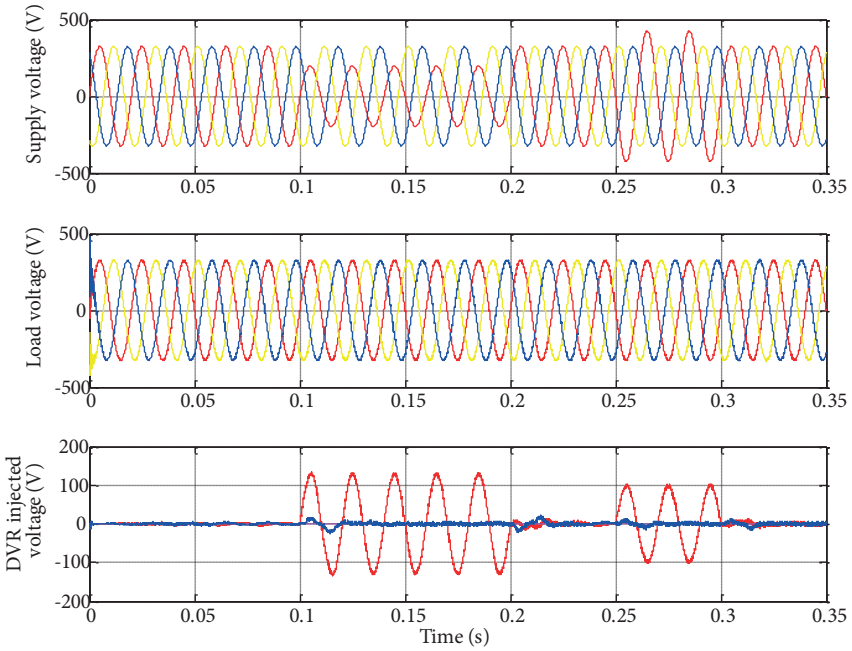

Figure 11. Simulation results of the proposed DVR for single phase sag and swell.

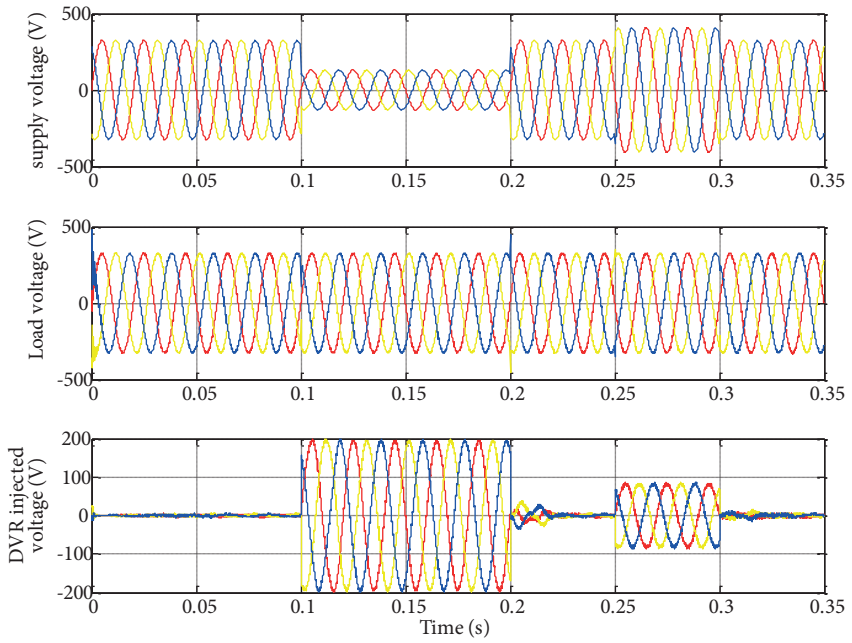

Figure 12. Simulation results of the proposed DVR for three phase sag and swell.

5. Experimental validation of the proposed DVR

An experimental model was set up for the proposed DVR in a single phase system as shown in Figure 13. The experimental platform was built around SPARTAN 3ADSP, which comprises MATLAB SIMULINK GUI for FPGA implementation (XC 3sd1800a-4fg676) of the control loop.

Two sets of experimental observations taken for voltage sag and swell are shown in Figures 14 and 15, respectively. The supply voltage, DVR injected voltage, and load voltages are measured by a precision power

Table 4. System parameters for the simulation study of the proposed DVR in a three phase system.

Source voltage	400 V	
Frequency	50 Hz	
Injection transformer	3 single phase transformers 1:1, 230 V, 1.5 kVA	
Load	Three phase R-L load	
DC source battery	200 V, 20 Ah	
Inverter switching frequency	10 kHz	
Quasi Z source impedance network	L	1 mH
	C	1 mF
Filter circuits (3 Nos)	R	0.3 Ω
	L	4 mH
	C	20 μF

Figure 13. Experimental setup.

analyzer (PPA). Figure 13 depicts the measured source voltage (U_1), injected DVR voltage (U_5), and load voltage (U_6), when a sag of 25% is applied in the source voltage, using a single phase autotransformer. As the supply voltage from the state electricity board contains some amount of harmonics, the results on THD does not match closely the simulation results. Performance of the DVR when a voltage swell of 25% occurs in the system is shown in Figure 15. It shows that the DVR injects around 25% of supply voltage in appropriate phase so that the load voltage is maintained at the desired level of 120 V. A comparative analysis of the experimental results with simulation results of the proposed DVR, for similar disturbances in supply voltage, is tabulated in Table 5. It is evident that both the results closely match each other with respect to the load voltage profile.

Table 5. Comparison of simulation and experimental results for the proposed DVR.

	Simulation results			Experimental results		
PQ event	Source voltage(V)	Injected voltage(V)	Load voltage(V)	Source voltage(V)	Injected voltage(V)	Load voltage(V)
25% voltage sag	90.36	30.48	120.12	90.4	30.06	120.01
16% voltage sag	101.17	19.76	120.19	101.25	18.35	119.1
17% voltage swell	140.97	19.84	120.46	140.72	20.722	119.8
25% voltage swell	150.57	29.35	120.46	150.98	31.88	119.4
Rated voltage	120.49	1.77	120.37	120.4	1.439	119.24

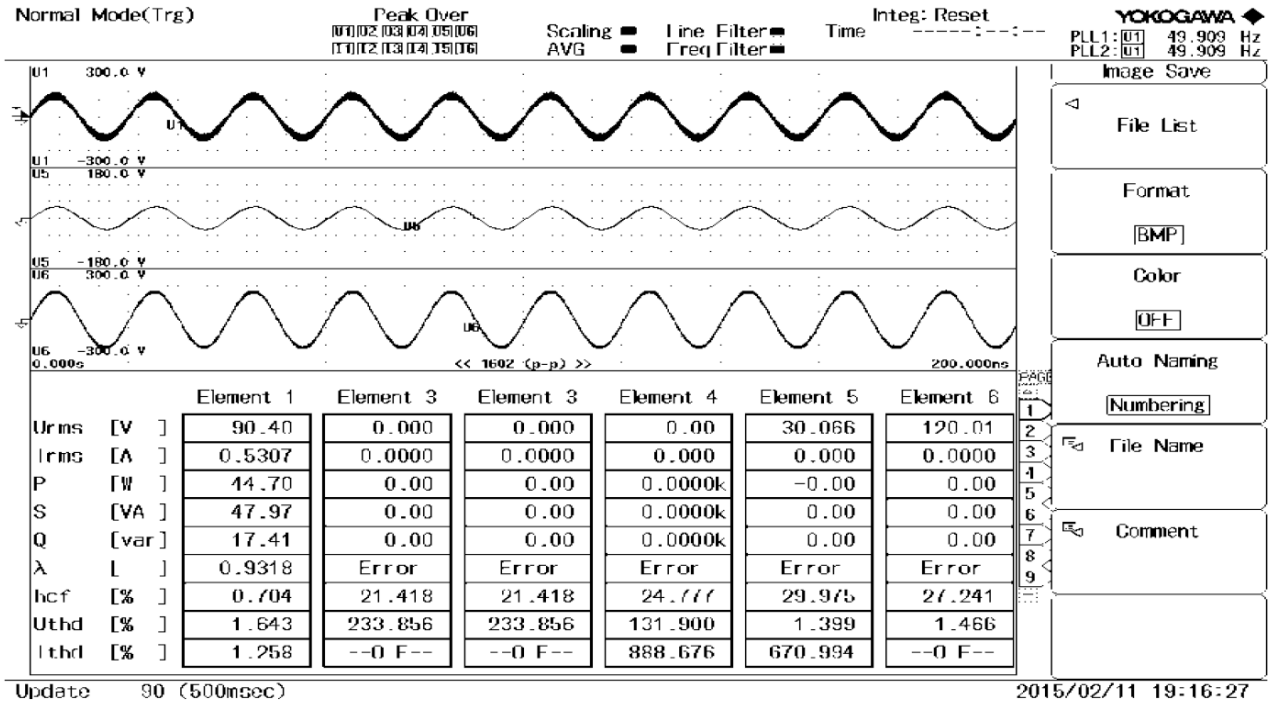

Figure 14. Experimental results for 25% voltage sag.

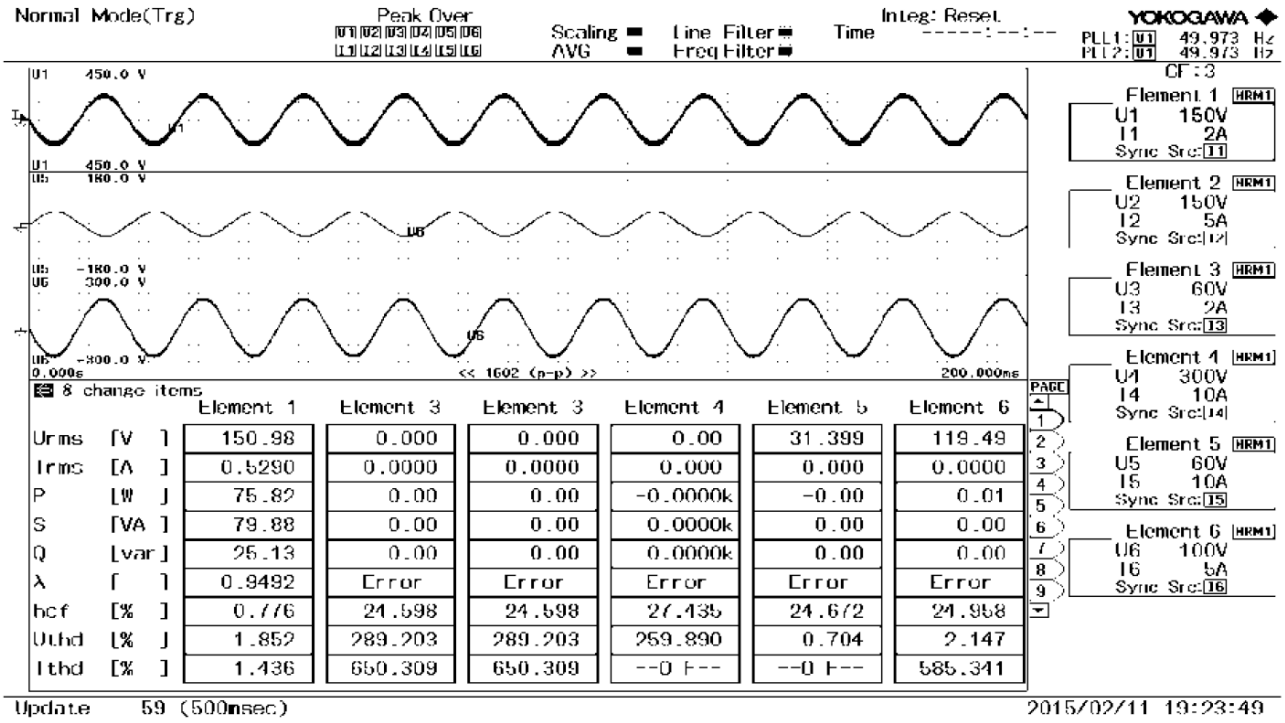

Figure 15. Experimental results for 25% voltage swell.

6. Conclusion

The design, development, and fabrication of a quasi Z source inverter based single phase DVR with variable structure control is presented. The voltage boosting ability of the quasi Z source inverter is fully utilized in the design. The proposed DVR is capable of injecting appropriate voltages even when the distribution system is subjected to deep voltage sags, without the need to have an energy source of higher rating. Variable structure control is successfully implemented, which gives good dynamic response during sag and swell conditions. The performance of the proposed DVR is analyzed against the conventional DVR. The proposed DVR performs robustly with reduced THD in the load voltage while keeping the stored energy requirement low. The simulation and experimental results of the proposed model were found to be closely matching within the limitations of the experimental setup. Simulation studies performed on a three phase system show the efficacy of the proposed DVR in practical distribution networks.

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