Turkish Journal of Electrical Engineering & Computer Sciences

http://journals.tubitak.gov.tr/elektrik/

Research Article

Turk J Elec Eng & Comp Sci
(2017) 25: 2399 – 2409

doi:10.3906/elk-1512-8

A CNFET full adder cell design for high-speed arithmetic units

Mokhtar MOHAMMADI GHANATGHESTANI[1], **Behnam GHAVAMI**[2,*], **Honeya SALEHPOUR**[1]
[1]Department of Computer Engineering, Science and Research Branch, Islamic Azad University, Tehran, Iran
[2]Shahid Bahonar University of Kerman, Kerman, Iran

Received: 02.12.2015 • **Accepted/Published Online:** 20.09.2016 • **Final Version:** 29.05.2017

Abstract: Carbon nanotube field-effect transistors (CNFETs) utilize an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure, which holds great promise for the future of integrated circuits. In this paper, a full adder cell based on a parallel design using CNFETs is presented. The main objective of designing this full adder cell is to reduce critical path delay in CNFET-based adder circuits. The proposed design positively affects speed and power consumption by shortening the data path. In order to evaluate the proposed design, several simulations were performed with different load capacitors, frequencies, and temperatures using HSPICE in 32-nm CMOS and 32-nm CNFET technologies. The proposed full adder cells were compared with five other full adder cells using 4-bit ripple carry adder (RCA) and 8-bit RCA circuits with power consumption, speed, and power delay product parameters. The obtained results indicate that the proposed design is faster than other designs due to a shortened data path. The results of the simulations confirm the higher efficiency of the proposed full adder cell with respect to other designs.

Key words: Arithmetic circuits, critical path delay, CNFET, full adder cell, nanoscale, speed

1. Introduction

In digital computers, arithmetic circuits are responsible for the main activities in data processing. These circuits provide the results required for solving arithmetic problems by receiving and processing the data. Other arithmetic operations can be adjusted using the four main arithmetic operations, and scientific problems may be solved by using numerical calculation methods. In reduced instruction set computers, arithmetic instructions are reduced and, as a result, integrate fewer arithmetic circuits. The other instructions are calculated by the existing circuits using numerical calculation methods. Meanwhile, addition is one of the main arithmetic circuits and other arithmetic circuits can use the addition operation. In many systems, the adders determine the overall efficiency of the system. All these cases can be important reasons for designing and improving adder circuits [1,2].

The structure of the full adder cell directly affects the efficiency of adder circuits. A full adder cell is a circuit with three inputs and two outputs. The outputs are equal to the addition of the inputs. The RCA circuit is formed by adding two n-bit numbers, such as A and B, and consists of n full adder cells. A_i and B_i are the ith bits of the two numbers A and B. They carry input (C_{in}) that derives from the previous full adder and enter it as the input of the ith full adder cell. Sum output and carry output (C_{out}) is the addition result

*Correspondence: ghavami@uk.ac.ir

of these three inputs. The equations related to the outputs of a full adder cell can be defined as in Eqs. (1) and (2) [3].

$$Sum = A_i \oplus B_i \oplus C_{in} \tag{1}$$

$$C_{out} = A_i B_i + A_i C_{in} + B_i C_{in} \tag{2}$$

RCAs have less hardware overhead than parallel adders, but the main defect of RCAs is their high delay because the data path is too lengthy. Hence, finding solutions to shorten the data path delay in these adders is deemed of value. Achieving this goal is the main reason for presenting a new full adder cell based on a parallel structure in this paper. In an n-bit RCA, data path delay is equal to the delay of the full adders contained in n full adder cells. However, when using the proposed full adder cells in an n-bit RCA circuit, the delay in its data path is equal to the sum of the delay of one adder cell and $(n - 1)$ 2-to-1 multiplexers. In the proposed design, multiplexers are used so that the delay is equal to one transistor. Consequently, the RCA delay will be equal to the sum of the delays of one full adder cell and $(n - 1)$ transistors. The simulation results of the implemented adder using the proposed full adder cell confirm this point.

The rest of this paper is organized as follows: CNFET technology is reviewed in Section 2 and previous works in Section 3. In Section 4, the proposed full adder cell will be presented. Simulation results and a comparison of the proposed design with other designs are provided in Section 5. Finally, a conclusion is given in Section 6.

2. CNFET review

CNFETs show considerable advantages compared to MOSFET transistors. P-type and N-type CNFETs have equal mobility. Hence, the sizing of transistors in complex circuits based on CNFET technology will be simpler than MOSFET technology. The CNFET is one of the promising successors to MOSFETs due to its unique electrical characteristics, such as ballistic transport and low OFF-current, which enable high-speed and low-power circuit designs [4].

Figure 1a is a schematic diagram of a CNFET. In CNFETs, carbon nanotubes are applied as transistor channels. Two types of CNFETs that are widely used are Schottky barrier (SB-CNFET) and MOSFET-like CNFET transistors. In SB-CNFETs, a carbon nanotube is connected directly to the source and drain, and a SB-CNFET is created in their connections. Drawbacks to SB-CNFETs include bipolar features that limit the usage of these transistors in traditional CMOS-like types. This connection restricts transconductance in the ON status; therefore, it reduces Ion/Ioff by a relative amount [5]. A schematic diagram of a SB-CNFET is illustrated in Figure 1b. Figure 1c shows another schematic diagram of CNFETs that behave more like MOSFET transistors. These types of transistors are known as MOSFET-like CNFETs. Unlike SB-CNFETs, these transistors are unipolar and they are more scalable than SB-CNFETs. They also decrease the OFF leakage current and have higher ON current in the source-to-channel junction because of their lack of a Schottky barrier [6].

The threshold voltage of the CNFETs is computed through Eqs. (3) and (4). The threshold voltage of these transistors indicates a reverse relationship with the diameter of carbon nanotubes (D_{CNT}). In Eqs. (3) and (4), n_1 and n_2 are the chirality of CNT, E_g depicts the band gap, e is the unit electron charge, a equals the carbon-to-carbon atom distance (0.249 nm), and V_π equals 3.033 eV and is the carbon $\pi - \pi$ bond energy

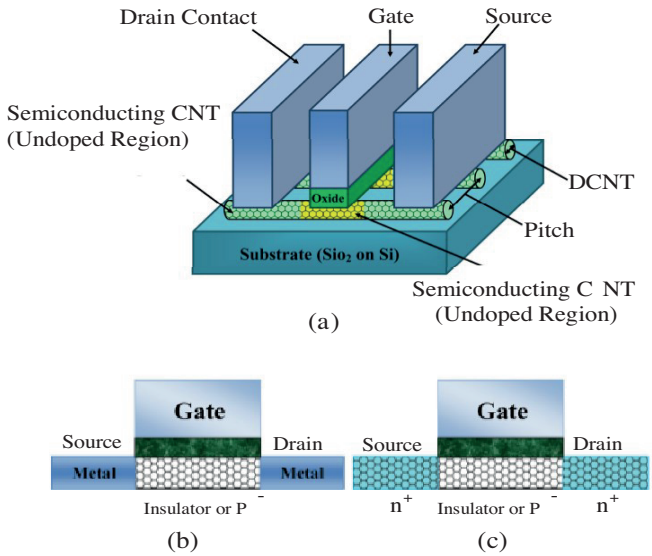

Figure 1. a) CNFET transistor, b) Schottky barrier (SB), c) MOSFET-like CNFET.

in the tight bonding model.

$$V_{th} \cong \frac{E_g}{2e} = \frac{\sqrt{3}}{3} \frac{a \times V_\pi}{e \times D_{CNT}} \cong \frac{0.43}{D_{CNT}\,(nm)} \tag{3}$$

$$D_{CNT} = \frac{a \times \sqrt{n_1^2 + n_2^2 + n_1 n_2}}{\pi} \cong 0.0783 \times \sqrt{n_1^2 + n_2^2 + n_1 n_2} \tag{4}$$

The width of the transistor is a factor that is very important in its efficiency. Eq. (5) reveals the width of a CNFET. N is the number of carbon nanotubes. The parameter pitch indicates the distance between the centers of the two carbon nanotubes. Meanwhile, W_{min} represents the minimum width of the gate in 32-nm technology, and this happens when the transistor includes one carbon nanotube [7].

$$W_{gate} = MAX(W_{min},\, (N-1)\, Pitch + D_{CNT}) \tag{5}$$

3. Previous works

Several methods have been introduced for designing a full adder cell. Some of them are faster and others have lower power consumption. Hence, the power delay product (PDP) parameter is used and compares them so that there is a tradeoff between the delay and power consumption parameters of the circuit. In this section, some new full adders are selected in CNFET and CMOS technologies.

The first full adder cell to be studied here is the minority function and bridge-style full adder (MBFA) presented in [8]. Its circuits are shown in Figure 2. This design is implemented based on the combination of minority function and bridge design. It includes 3 capacitors and 16 transistors. The critical path of the circuit contains 4 transistors and one capacitor, which leads to an increase in circuit delay. The complement of C_{out} is created by a capacitor network and a CMOS inverter gate. The sum output is then created using the complement of C_{out} output and a bridge design.

A CNFETFA-1 full adder cell was presented in [9]. Its circuit is shown in Figure 3. This design uses a capacitor network to create a minority function. This circuit consists of 12 transistors and 3 capacitors. Its

critical path includes 3 transistors and one capacitor. Applying pass transistor logic causes the complement sum output signal to lack full swing and increases the static power consumption.

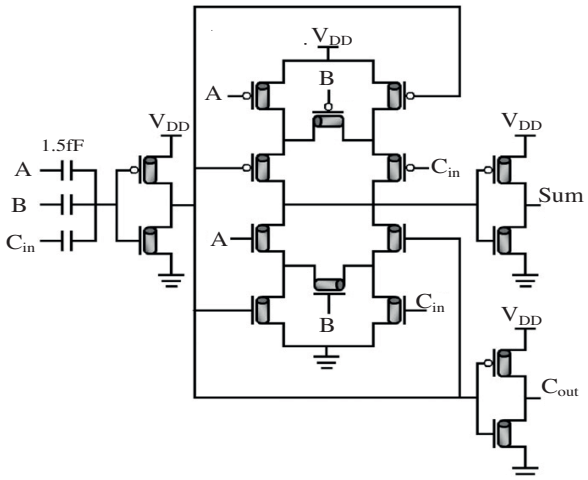

Figure 2. MBFA cell presented in [8].

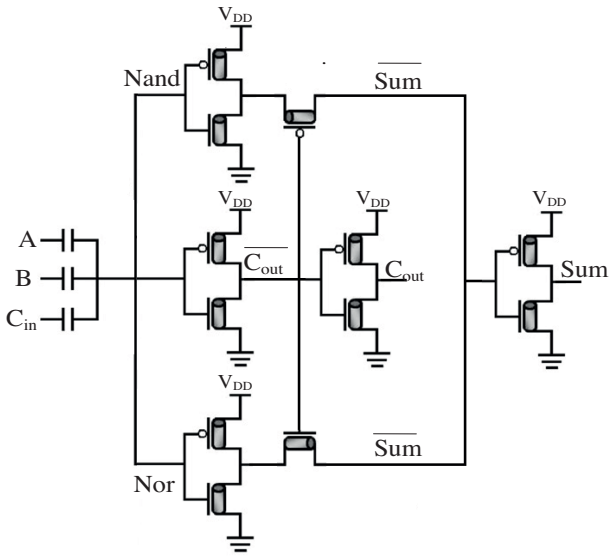

Figure 3. CNFETFA-1 cell presented in [9].

The next circuit is a CNPTL full adder, presented in [10]. The circuit of this full adder cell is shown in Figure 4. This circuit is made up of 20 transistors. There is a symmetric structure in this design and it does not use complement input signals. Since this circuit uses only 2 transistors in its critical path, it is quite speedy. However, since there is no direct path between the power supply and the earth in the sum production circuit, it has relatively low power consumption. The problem with this circuit is that using pass transistor logic causes the output voltage to lack full swing. In other words, the driving capability is low. Therefore, this circuit will have a very high delay when it is used in large adders.

The other design is CNFETFA-2, which was presented in [11]. The circuit of this full adder cell is shown in Figure 5. This design is composed of 3 modules. The first module implements XOR/XNOR functions. They are created using two symmetric output modules, C_{out} and Sum. This design includes 28 transistors. Its critical path contains 4 transistors. Hence, it is very slow. In addition, since it uses pass transistor logic, the method has low driving capability. One of its advantages is that it has low power consumption.

The last full adder cell that is discussed here is CLRCLFA, presented in [12]. The circuit of this full adder cell is shown in Figure 6. This design is based on CMOS technology and incorporates 12 transistors. The outputs lack full swing since pass transistor logic is used and can cause low driving capability and long propagation delay. Table 1 shows the important properties of these full adder cells.

Table 1. Specifications of previous full adder cells.

Full adder cells	Delay	Power consumption	Critical path	Number of transistors	Number of capacitors
MBFA	Low	Low	4 transistors + 1 capacitor	16	3
CNFETFA-1	Low	High	3 transistors + 1 capacitor	12	3
CNPTLFA	Medium	Low	2 transistors	20	0
CNFETFA-2	Medium	Low	4 transistors	28	0
CLRCLFA	High	Medium	3 transistors	12	0

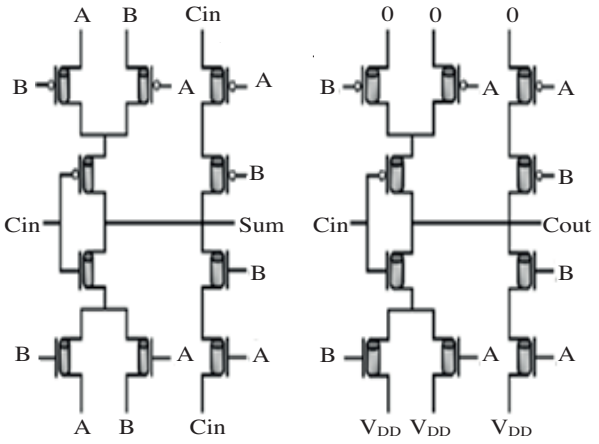

Figure 4. CNPTLFA cell presented in [10].

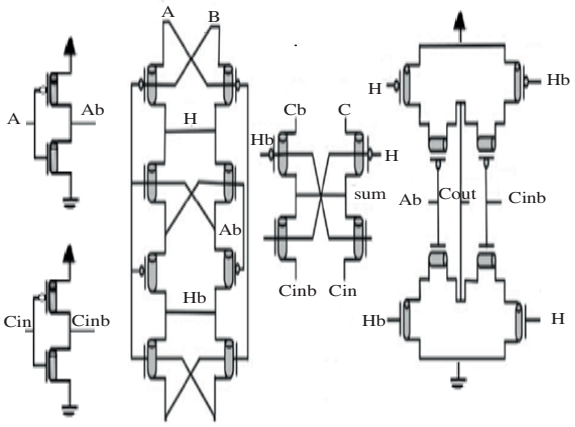

Figure 5. CNFETFA-2 cell presented in [11].

4. The proposed full adder cell

The proposed technique for reducing critical path delay in adder circuits is using a parallel structure in designing full adder cells. The structure of this parallel design is based on a block diagram, as shown in Figure 7. In this structure, the addition of two input bits of A and B, with 0 and 1, is calculated in parallel. The C_{in} input bit determines which addition result should be carried to the multiplexer gates. If C_{in} is 0, then the operation will be A + B + 0; otherwise, A + B + 1 will be taken to the output. It seems the proposed design is similar to carry-skip adders. However, the proposed design is imposed on the full adder cell.

As shown in Figure 8, RCA circuits are implemented based on the proposed structure for full adder cells. After obtaining the C_{in} bit in each full adder except the first full adder, only one of $A_i + B_i + 0$ or $A_i + B_i + 1$ needs to be calculated before transfer to the multiplexer output. Therefore, without any dependence on the delay of a full adder cell, the delay from the presence of each full adder cell on the critical path of the adder circuit will be equal to the delay of a 2-to-1 multiplexer. Hence, in the n-bit RCA circuit based on the proposed structure, the delay of the critical path will be equal to the sum of the delay of one full adder cell and $(n - 1)$ 2-to-1 multiplexers.

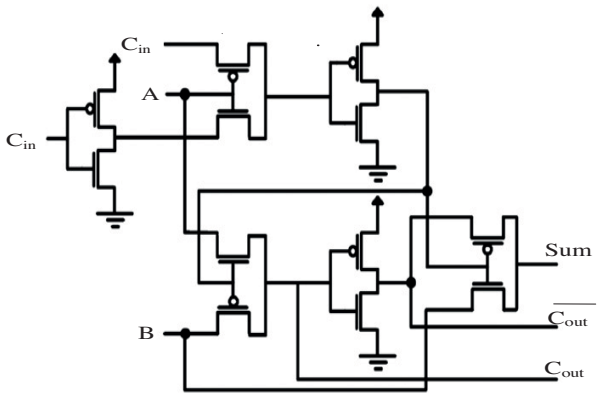

Figure 6. CLRCLFA full adder cell presented in [12].

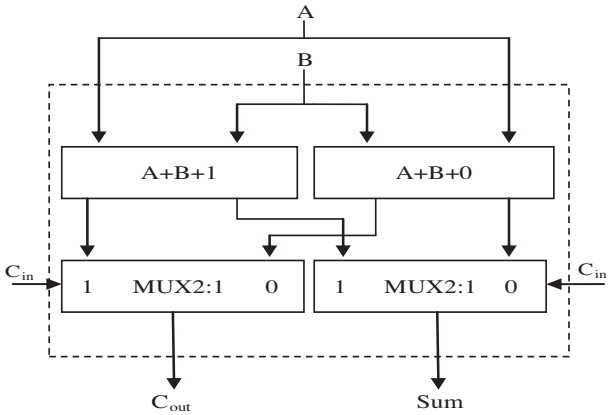

Figure 7. The block diagram for the proposed full adder cell.

In order to design a full adder cell based on the parallel structure in Figure 7, some equations should be extracted for the C_{out} and sum outputs so that their input (C_{in}) is a determining one. This means that by

regarding the value of the C_{in} bit (0 or 1), we should be able to determine what relationship exists between the A and B inputs to supply the proper logic for the C_{out} and sum outputs. Table 2 is used to obtain these equations. Based on this table, if $C_{in} = 0$, then the sum output will be equal to $\overline{(A \times B)} \times (A + B)$, and if $C_{in} = 1$, then the sum output will be equal to $\overline{\overline{(A \times B) \times (A + B)}}$. Therefore, C_{in} determines the sum output. Likewise, for the output C_{out}, if $C_{in} = 0$, then C_{out} will be equal to (A × B), and if $C_{in} = 1$, then C_{out} will be equal to (A + B). Thus, C_{in} can determine the value of C_{out}. According to the explanations here, Eqs. (6) and (7) for C_{out} and sum are as follows:

Table 2. The truth table for the proposed full adder cell.

A	B	C_{in}	A × B	A + B	C_{out}	Sum
0	0	0	0	0	0	0
0	0	1	0	0	0	1
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	0	1
1	0	1	0	1	1	0
1	1	0	1	1	1	0
1	1	1	1	1	1	1

$$Sum = \overline{C_{in}} \times \left[\overline{(AB)} \times (A+B)\right] + C_{in} \times \overline{\left[\overline{(AB)} \times (A+B)\right]} \tag{6}$$

$$C_{out} = \overline{C_{in}} \times (A \times B) + C_{in} \times (A+B) \tag{7}$$

The circuit of the proposed full adder cell at gate level, based on Eqs. (6) and (7), is shown in Figure 9 and its circuit at the transistor level is shown in Figure 10. In this design, the OR and AND circuits are designed based on transmission gates and NOT gates are designed based on CMOS logic. Using CMOS logic and transmission gates has the advantage of full swing outputs. If the outputs have full swing, they will have a higher driving capability that leads to a higher speed of data movement along the critical path in the adder circuit.

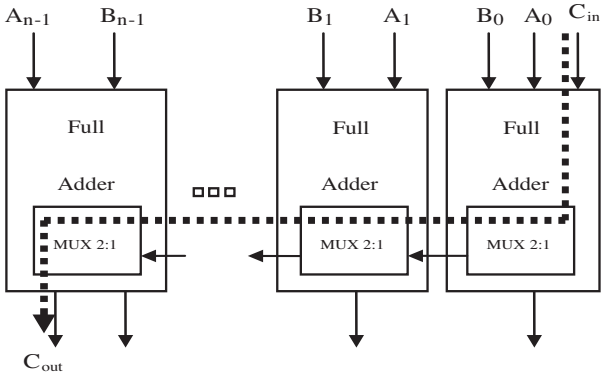

Figure 8. n-bit RCA block diagram based on the proposed design.

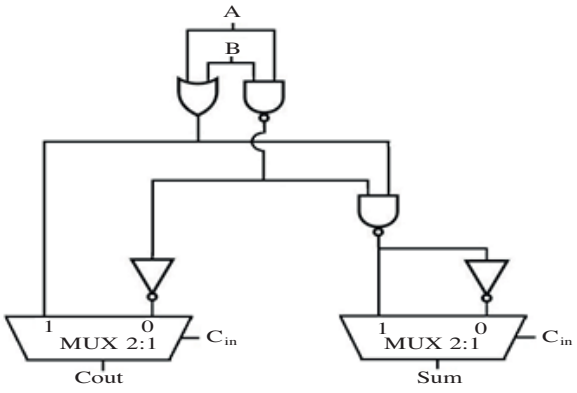

Figure 9. Gate-level circuit of the proposed full adder cell.

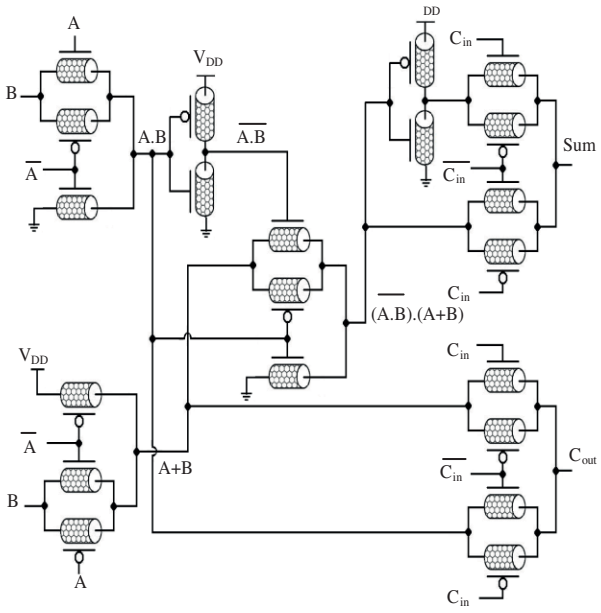

Figure 10. Transistor-level circuit of the proposed full adder cell.

5. Simulation results

A comprehensive simulation was carried out through the Synopsys HSPICE simulator software under different environmental conditions in order to study and compare the design parameters of the different circuits. The CMOS-based circuits were simulated with 32-nm CMOS technology and CNFET-based circuits were simulated with the 32-nm library model used in [13] and [14] based on CNFET technology. In Table 3, important parameters of this model are described.

Table 3. CNFET model parameters.

Parameters	Description	Value
L_{ch}	Physical channel length	32 nm
L_{geff}	Mean free path in the intrinsic CNT channel	100 nm
L_{ss}	Length of doped CNT source-side extension region	32 nm
L_{dd}	Length of doped CNT drain-side extension region	32 nm
K_{gate}	The dielectric constant of high-k top gate dielectric material	16
T_{ox}	The thickness of high-k top gate dielectric material	4 nm
C_{sub}	The coupling capacitance between the channel region and the substrate	40 pF/m
Efi	The Fermi level of the doped S/D tube	6 eV

PDP is the main parameter for comparing the efficiency of different designs. The reason behind such an alternative is that this standard sets a compromise between power consumption and delay. The time that it takes the input to reach 50% of power supply voltage is considered as the delay parameter until the output reaches the same voltage. Rising and falling propagation delays are separately calculated for C_{out} and sum outputs, and the maximum value is regarded as the delay parameter. All possible states of the input passes to the circuit are implemented in order to calculate circuit delay. The delay of all outputs is considered for each pass and, finally, the maximum delay is reported as circuit delay. Power consumption is the average power that is computed during all the transistors. PDP is obtained according to Eq. (8), which is the multiplication of the

maximum delay and the average power consumption.

$$PDP = Max(\text{Delay}) \times Avg(\text{Power Consumption}) \tag{8}$$

Figure 11 shows the required test pattern and output waveforms for the proposed full adder cell with a power supply of 0.65 V, frequency of 250 MHz, room temperature, and load capacitance of 2.1 fF. It indicates that the outputs are true and have full swing. Simulation results are illustrated in Table 4. The simulation results for different power supplies (0.5 V, 0.65 V, and 0.8 V) were obtained with a capacitance of 2.1 fF and room temperature conditions. The obtained results suggest that the proposed design leads to an improvement over the others by shortening the data path. For example, if a 0.65 V power supply is used, the proposed design will be 74%, 72%, 69%, 61%, and 49% faster than CLRCLFA, CNPTLFA, CNFETFA-2, CNFETFA-1, and MBFA, respectively. The PDP of the proposed design is 71%, 64%, 39%, 26%, and 6% lower than CNFETFA-1, CLRCLFA, CNPTLFA, CNFETFA-2, and MBFA, respectively.

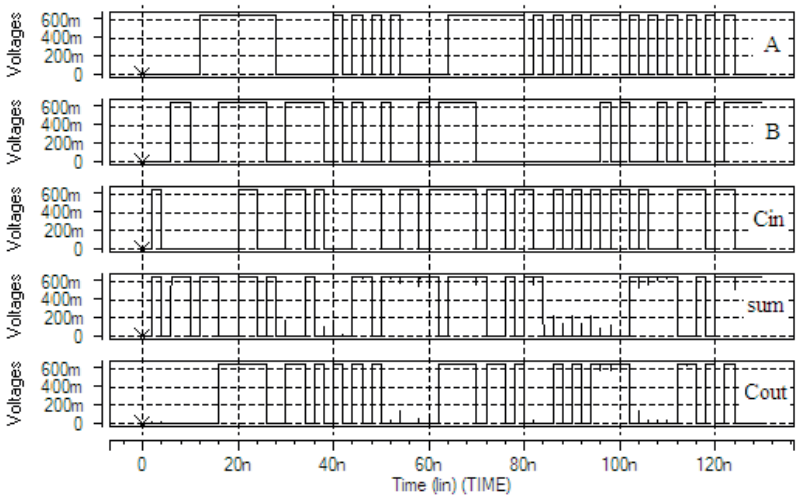

Figure 11. Test pattern and output waveforms for proposed full adder cell.

The ability of the truth operation to function at different frequencies is a recent requirement of digital systems. Thus, the proposed and other designs were simulated at different frequencies. The results of these simulations are depicted in Figure 12. These results were obtained with 0.65-V power supply, room temperature, 2.1-fF load capacitor, and the specified range of frequencies. According to this diagram, it is evident that PDP is lower in the proposed full adder compared to the other designs.

The driving capability is the speed with which a circuit can charge or discharge circuit output. This circuit becomes more significant when it is exposed to high output capacity. In this state, it should have enough power to drive other circuits. Thereby, different circuits are evaluated in the presence of different load capacitors. The results of these simulations are shown in Figure 13. These results were obtained with a 0.65-V power supply at 250-MHz frequency, room temperature, and the specified range of load capacitors. As shown in Figure 13, the proposed design is of acceptable efficiency in different output charges compared to the other designs.

Since temperature noise negatively affects the efficiency of the designed circuits, it is one of the main concerns for circuit designers. Different circuits were simulated at different temperatures. The results of these simulations are shown in Figure 14. These results were obtained at 0.65-V power supply, 250-MHZ frequency,

Table 4. Simulation results of the full adder cells.

PDP ($\times 10^{-18}$ J)	Power ($\times 10^{-7}$ W)	Delay ($\times 10^{-12}$ s)	Full adder cells
V_{DD} = 0.8 V			
5.9021	2.9411	20.068	MBFA
19.078	8.5307	22.365	CNFETFA-1
6.7341	2.2308	30.187	CNPTLFA
6.6094	2.3924	27.627	CNFETFA-2
15.292	4.3524	35.136	CLRCLFA
5.8224	5.3246	10.935	Proposed FA
V_{DD} = 0.65 V			
5.3070	2.1981	24.144	MBFA
17.383	5.4456	31.922	CNFETFA-1
8.2330	1.8334	44.906	CNPTLFA
6.7527	1.6912	39.929	CNFETFA-2
14.076	2.9016	48.514	CLRCLFA
4.9618	4.0568	12.231	Proposed FA
V_{DD} = 0.5 V			
6.4250	1.7092	37.591	MBFA
17.028	3.5680	47.725	CNFETFA-1
10.151	1.5158	66.974	CNPTLFA
8.1358	1.5891	51.198	CNFETFA-2
11.028	1.9294	57.160	CLRCLFA
6.7262	3.2197	20.891	Proposed FA

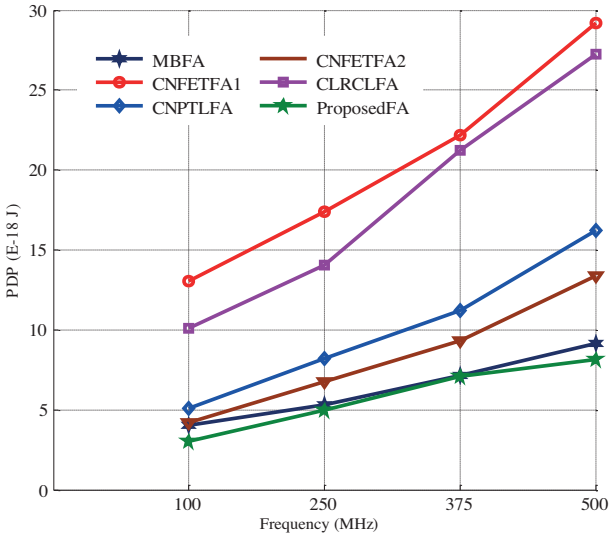

Figure 12. PDP of full adders with respect to different frequencies.

2.1-fF load capacitor, and the specified range of temperatures. According to the results, it is evident that the performance of the proposed circuit is acceptable at different temperatures.

The PDP of the proposed design is lower than that of the other designs in different simulations due to full swing outputs, lack of capacitors, and the use of transistors with normal threshold voltages.

Different circuits should be able to perform in larger circuits with a higher efficiency. Also, it is preferable to compare full adder cells that are in fact adders with each other. Therefore, 4-bit RCA and 8-bit RCA circuits

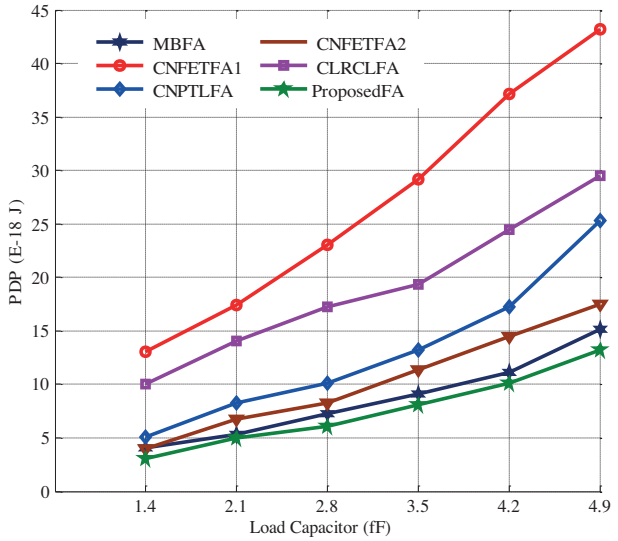

Figure 13. PDP of full adders with respect to load capacitors.

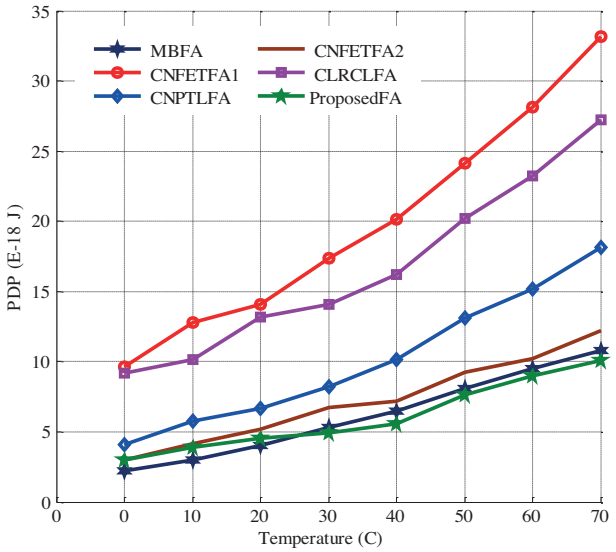

Figure 14. PDP of full adders with respect to different temperatures.

were simulated based on the proposed full adder cells and other full adder cells. The results of these simulations are depicted in Tables 5 and 6. According to the results, the proposed design leads to a considerable improvement over other designs because of the shortening of the data path.

Table 5. Simulation results of 4-bit adders.

PDP ($\times 10^{-18}$ J)	Power ($\times 10^{-7}$ W)	Delay ($\times 10^{-12}$ s)	4-bit RCAs
42.312	4.9251	85.912	MBFA
181.24	17.396	104.19	CNFETFA-1
48.978	4.1952	116.75	CNPTLFA
31.700	3.4297	92.428	CNFETFA-2
214.21	13.927	153.81	CLRCLFA
18.632	8.9951	20.713	Proposed FA

Table 6. Simulation results of 8-bit adders.

PDP ($\times 10^{-18}$ J)	Power ($\times 10^{-7}$ W)	Delay ($\times 10^{-12}$ s)	8-bit RCAs
358.98	13.973	256.91	MBFA
948.92	29.168	325.33	CNFETFA-1
1034.7	11.813	875.96	CNPTLFA
151.02	7.9138	190.84	CNFETFA-2
785.43	28.428	276.29	CLRCLFA
67.803	16.363	41.438	Proposed FA

6. Conclusion

A full adder cell based on CNFET technology is proposed. This cell can work in a wide range of frequencies, load capacitors, and temperatures. The main advantage of the proposed full adder is the significant reduction of data path delay in large adder circuits.

For example, the 8-bit RCA based on the proposed design is 95%, 87%, 85%, 83%, and 78% faster than 8-bit RCAs based on CNPTLFA, CNFETFA-1, CLRCLFA, MBFA, and CNFETFA-2, respectively, and the PDP of the 8-bit RCA based on the proposed design is 93%, 92%, 91%, 81%, and 55% lower than that of the CNPTLFA, CNFETFA-1, CLRCLFA, MBFA, and CNFETFA-2, respectively. Accordingly, the proposed design can be utilized in several applications, especially in arithmetic circuits for high-speed circuits.

References

[1] Uyemura J. CMOS Logic Circuit Design. 1st ed. Dordrecht, the Netherlands: Kluwer Academic Publishers, 2001.

[2] Rabaey JM, Chandrakasan A, Nikolic B. Digital Integrated Circuits: A Design Perspective. 2nd ed. Englewood Cliffs, NJ, USA: Prentice Hall, 2002.

[3] Mirzaee RF, Moaiyeri MH, Navi K. High speed NP-CMOS and multi-output dynamic full adder cells. International Journal of Electrical, Computer and Systems Engineering 2010; 4: 304-310.

[4] Tans SJ, Verschueren ARM, Dekker C. Room-temperature transistor based on a single carbon nanotube. Nature 1998; 393: 49-52.

[5] O'Connor I, Liu J, Gaffiot F, Pregaldiny F, Lallement C, Maneux C, Goguet J, Fregonese S, Zimmer T, Anghel L. CNTFET modeling and reconfigurable logic-circuit design. IEEE T Circuits-I 2007; 54: 2365-2379.

[6] Raychowdhury A, Roy K. Carbon nanotube-based voltage-mode multiple-valued logic design. IEEE T Nanotechnol 2005; 4: 168-179.

[7] Moaiyeri MH, Chavoshisani R, Jalali A, Navi K, Hashemipour O. High performance mixed-mode universal min-max circuits for nanotechnology. Circuits Syst Signal Process 2012; 31: 465-488.

[8] Navi K, Hossein Sajedi H, Faghih Mirzaee R, Moaiyeri MH, Jalali A, Kavehei O. High-speed full adder based on minority function and bridge style for nanoscale. Integration 2011; 44: 155-162.

[9] Reshadinezhad MR, Moaiyeri MH, Navi K. An energy-efficient full adder cell using cnfet technology. IEICE T Electron 2012; 4: 744-751.

[10] Moayeri MH, Faghih Mirzaee M, Navi K, Momeni A. Design and analysis of high-performance CNFET-based full adder. Int J Electron 2012; 99: 113-130.

[11] Ghadiry MH, Abd Manaf A, Ahmadi MT, Sadeghi H, Senejani N. Design and analysis of a new carbon nanotube full adder cell. J Nanomater 2011; 2011: 906237.

[12] Lin JF, Hwang YT, Sheu MH, Ho C. A novel high speed and energy efficient 10 transistor Full adder design. IEEE T Circuits-I 2007; 54: 1050-1059.

[13] Deng J, Wong HSP. A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application—Part I: Model of the intrinsic channel region. IEEE T Electron Dev 2007; 54: 3184-3194.

[14] Deng J, Wong HSP. A compact SPICE model for carbon nanotube field-effect transistors including nonidealities and its application—Part II: Full device model and circuit performance benchmarking. IEEE T Electron Dev 2007; 54: 3195-3205.